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Paid
NP
(14)

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

POLYSTAK, INC.,

Plaintiff,

v.

ENTORIAN TECHNOLOGIES L.P.,

Defendant.

Case No. CV 12-01048 MEJ

COMPLAINT FOR DECLARATORY RELIEF

DEMAND FOR JURY TRIAL

Plaintiff Polystak, Inc. ("Polystak") hereby demands a jury trial and alleges as follows:

NATURE OF THE ACTION

1. This is an action for a declaratory judgment of noninfringement and invalidity of United States Patent No. 5,420,751 (the "'751 Patent" or "Patent-in-Suit").

THE PARTIES

2. Plaintiff Polystak is a corporation organized and existing under the laws of the state of California, with a principal place of business at 2186 Paragon Drive, San Jose, California.

3. On information and belief, Defendant Entorian Technologies L.P. ("Entorian") is a limited partnership organized and existing under the laws of the state of Texas, with a principal place of business at 4030 West Braker Lane, Austin, Texas, and on information and belief, affiliated with Entorian Technologies, Inc., a corporation organized and existing under the laws of the state of Delaware.

JURISDICTION AND VENUE

4. This action arises under the patent laws of the United States, Title 35 of the United States Code, § 1 *et seq.* and under the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202. This case presents an actual, substantial, and continuing justiciable controversy under Article III of the United States Constitution and serves a useful purpose in clarifying and settling the legal rights at issue.

5. This Court has subject matter jurisdiction over this case pursuant to 28 U.S.C. §§ 1331, 1338(a), 2201, and 35 U.S.C. § 1 *et seq.*

6. This Court has personal jurisdiction over Entorian. On information and belief, Entorian has its principal place of business in Texas, but conducts business in this judicial district and elsewhere in the state of California. Entorian has established minimum contacts with this forum and the exercise of jurisdiction over Entorian would not offend the traditional notions of fair play and substantial justice.

7. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 and 1400. Entorian resides in this judicial district because it is subject to personal jurisdiction in this judicial district.

INTRADISTRICT ASSIGNMENT

8. Under Civil Local Rules 3-2(c) and 3-5, this action, being a declaratory judgment action based on patent claims, is appropriate for assignment on a district-wide basis.

PATENT-IN-SUIT

9. U.S. Patent No. 5,420,751, which issued on May 30, 1995 and expires on May 30, 2012, is entitled "Ultra High Density Modular Integrated Circuit Package." The '751 Patent is directed to a "modular integrated circuit package," e.g., memory stacks. A copy of the '751 Patent is attached hereto as Exhibit A.

10. The '751 Patent was the first to issue in a family of patents that include U.S. Patent No. 6,025,642, entitled "Ultra High Density Integrated Circuit Packages" ("'642 Patent") and U.S. Patent No. 5,446,620, also entitled "Ultra High Density Integrated Circuit Packages" ("'620 Patent") (collectively, "Related Patents"). The '642 Patent issued on February 15, 2000 and expired on August 1, 2010. The '620 Patent issued on August 29, 1995 and expires on August 29, 2012.

11. According to assignment records at the United States Patent and Trademark Office, Entorian is the record owner of the '751 Patent and its Related Patents.

12. Entorian's affiliated entity, Entorian Technologies, Inc., has also asserted ownership and/or control of the '751 Patent and its Related Patents, including the right to sue and grant licenses.

ENTORIAN'S ACCUSATION OF INFRINGEMENT OF THE PATENT-IN-SUIT

13. Polystak designs, manufactures, and sells memory module components among other products using a patented, proprietary "Direct Stacking Technology."

14. Fusion-io, Inc. ("Fusion") designs, manufactures, and sells certain memory platforms, such as solid-state drives ("SSD"), among other products and is a customer of

Polystak. Fusion SSD products incorporate a variety of discrete components, including memory module components, which Fusion purchases from Polystak.

15. In a letter dated April 22, 2011 from Entorian to Fusion, Entorian alleged that the memory module components in the Fusion 640GB ioDrive product infringed the Patent-in-Suit: "It has come to our attention that Fusion io makes and sells solid state drives that infringe U.S. Patents owned by Entorian. For example, your 640GB IODRIVE product FS1-003-641-CS-0001 appears to include 24 memory stacks. These stacks are made from two packaged TSOP devices whose respective leads are connected as claimed, for example, in Entorian's U.S. Pat. No. 5,420,751. We hereby notify you that your 640GB IODRIVE infringes U.S. Pat. No. 5,420,751 under Title 35 § 271 of the U.S. Code. Subject to further investigation, we believe that your 640GB IODRIVE likely infringes U.S. Pat. No. 6,025,642." Entorian demanded that Fusion cease this alleged infringement and threatened to "pursue all available legal remedies." A copy of Entorian's April 22, 2011 letter is attached hereto as Exhibit B.

16. In a letter dated May 18, 2011 from Fusion to Entorian, Fusion requested that Entorian provide details of its allegations, including identification of the specific patent claims and the products that allegedly infringe. A copy of the May 18, 2011 letter is attached hereto as Exhibit C.

17. In a letter dated May 19, 2011 from Fusion to Polystak, Fusion notified Polystak of Entorian's infringement allegations against the Polystak memory module components and Fusion's intent to seek indemnity from Polystak pursuant to Section 15 of the FUSION-IO, INC. PURCHASE ORDER TERMS AND CONDITIONS. A copy of the May 19, 2011 letter is attached hereto as Exhibit D and the FUSION-IO, INC. PURCHASE ORDER TERMS AND CONDITIONS is attached hereto as Exhibit E.

18. In a letter dated May 31, 2011 from Entorian to Fusion, Entorian specifically identified Claim 13 of the '751 Patent, listed out each element and alleged that each element was met by the "modules of leaded ICs," i.e., the memory module components, in Fusion's 640GB ioDrive. Again, Entorian demanded that Fusion take a license and threatened "to assert a more

aggressive range of legal remedies." A copy of the May 31, 2011 letter is attached hereto as Exhibit F.

19. In July 2011, pursuant to its indemnity obligation to Fusion, Polystak directly contacted Entorian. Polystak informed Entorian that Polystak was the real party in interest because Polystak supplied the memory module components for the Fusion product FS1-003-641-CS-0001 that were accused by Entorian in its April 22, 2011 letter and Polystak owed an indemnity obligation to Fusion. Entorian demanded that Polystak take a license to Entorian's patents, including specifically the '751 Patent.

20. Polystak and Entorian were unable to resolve their dispute. The last communication between Polystak and Entorian took place in or around July 25, 2011. After that date, Entorian did not contact Polystak or Fusion again.

21. On February 7, 2012, roughly three months before the '751 Patent is set to expire and nearly a year after first contacting Fusion and Polystak, Entorian filed a lawsuit against Fusion in the United States District Court, District of Utah, Central Division, Case No. 2:12-cv-158, captioned as *Entorian Technologies L.P. v. Fusion-io, Inc.* ("Utah Lawsuit"). A copy of the complaint filed in the Utah Lawsuit is attached hereto as Exhibit G.

22. In the Utah Lawsuit, Entorian alleged, "Fusion is and has been manufacturing, using, selling, and offering to sell solid state drives within the United States, and importing solid state drives into the United States, including without limitation solid state drives having the designation FS1-003-641-CS-0001, each comprising one or more memory stacks (the "Accused Products")." Entorian named only one product in the Utah Lawsuit – the same product it identified in its April 22, 2011 letter, which incorporates the Polystak memory module component accused of infringement by Entorian.

23. At the time of filing the Utah Lawsuit, Entorian was fully informed and aware that Polystak is the real party in interest for its infringement allegations.

24. On February 15, 2012, Fusion sought indemnification from and tendered defense of the Utah Lawsuit to Polystak. A copy of the February 15, 2012 letter is attached hereto as Exhibit H.

FIRST CLAIM FOR RELIEF

(Declaratory Judgment of Noninfringement of the '751 Patent)

25. Polystak realleges and incorporates by reference Paragraphs 1 through 24 as if fully set forth herein.

26. This is an action for declaratory judgment of noninfringement of any valid and enforceable claims of the '751 Patent.

27. Entorian has accused Polystak memory module components of infringing at least the '751 Patent, asserted that a license to the '751 Patent is required, and threatened to resolve the matter through litigation.

28. Entorian filed an actual suit against Fusion, a customer of Polystak, alleging that Polystak memory module components incorporated into the Fusion "ioDrive" product infringe the '751 Patent.

29. Polystak denies infringement, whether direct or indirect, literal or by equivalents, of any valid and enforceable claim of the '751 Patent and denies that it is required to license the '751 Patent.

30. Entorian's filing of the Utah Lawsuit has triggered Polystak's indemnity obligation to Fusion.

31. Entorian's allegations and Polystak's denials and indemnity obligations give rise to an immediate and substantial controversy regarding the alleged infringement of the '751 Patent.

32. An actual and justiciable controversy exists as to whether the '751 Patent is infringed by Polystak.

33. A judicial declaration is necessary and appropriate to ascertain Polystak's rights regarding the '751 Patent.

34. Polystak accordingly requests a judicial determination of its rights, duties, and obligations with regard to the '751 Patent.

SECOND CLAIM FOR RELIEF

(Declaratory Judgment of Invalidity of the '751 Patent)

35. Polystak realleges and incorporates by reference Paragraphs 1 through 34 as if fully set forth herein.

36. This is an action for declaratory judgment of invalidity of any and all claims of the '751 Patent.

37. Entorian has accused Polystak memory module components of infringing at least the '751 Patent, asserted that a license to the '751 Patent is required, and threatened to resolve the matter through litigation.

38. Entorian filed an actual suit against Fusion, a customer of Polystak, alleging that Polystak memory module components incorporated into the Fusion "ioDrive" product infringe the '751 Patent.

39. Polystak denies infringement, whether direct or indirect, literal or by equivalents, of any valid and enforceable claim of the '751 Patent and denies that it is required to license the '751 Patent.

40. Entorian's filing of the Utah Lawsuit has triggered Polystak's indemnity obligation to Fusion.

41. The claims of the '751 Patent are invalid because they fail to comply with the conditions and requirements for patentability set forth in 35 U.S.C. § 1 *et seq.*, including but not limited to 35 U.S.C. §§ 101, 102, 103, and 112.

42. Therefore, an immediate and substantial controversy exists regarding the validity of the '751 Patent.

43. An actual and justiciable controversy exists as to whether the '751 Patent is valid.

44. A judicial declaration is necessary and appropriate to ascertain Polystak's rights regarding the '751 Patent.

45. Polystak accordingly requests a judicial determination of its rights, duties, and obligations with regard to the '751 Patent.

PRAYER FOR RELIEF

WHEREFORE, Polystak respectfully requests that judgment be entered in its favor and prays the Court to grant the following relief:

A. A declaration that Polystak's products have not and do not infringe, either directly or indirectly, literally or by equivalents, any valid and enforceable claim of the Patent-in-Suit;

B. A declaration that the Patent-in-Suit is invalid;

C. An order enjoining Entorian, its officers, directors, agents, counsel, and employees, and all other persons in active concert or participation with the foregoing, from alleging infringement or instituting any action for infringement of the Patent-in-Suit against Polystak and/or any of Polystak's customers for the use or sale of Polystak's products;

D. An order declaring that Polystak is the prevailing party and that this is an exceptional case under 35 U.S.C. § 285;

E. That Polystak be awarded its reasonable attorneys fees, expenses, and costs in relation to this action; and

F. Such other relief as this Court may deem just and proper.

DATED: March 1, 2012

By: _____

Adrian M. Pruetz
Avraham Schwartz
GLASER WEIL FINK JACOBS HOWARD AVCHEN & SHAPIRO LLP

Andrew Choung
ECHELON LAW GROUP, PC

Attorneys for Plaintiff
Polystak, Inc.

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b) and the Northern District of California Local Rule 3-6(a), Polystak respectfully requests a jury trial on all issues triable thereby.

DATED: March 1, 2012

By: 

Adrian M. Pruetz
Avraham Schwartz
GLASER WEIL FINK JACOBS HOWARD AVCHEN & SHAPIRO LLP

Andrew Choung
ECHELON LAW GROUP, PC

Attorneys for Plaintiff
Polystak, Inc.

EXHIBIT A

US005420751A

United States Patent [19]

Burns

[11] Patent Number: 5,420,751

[45] Date of Patent: May 30, 1995

[54] **ULTRA HIGH DENSITY MODULAR INTEGRATED CIRCUIT PACKAGE**

[75] Inventor: **Carmen D. Burns**, Austin, Tex.

[73] Assignee: **Staktek Corporation**, Austin, Tex.

[21] Appl. No.: **133,397**

[22] Filed: **Oct. 8, 1993**

Related U.S. Application Data

[62] Division of Ser. No. 561,417, Aug. 1, 1990.

[51] **Int. Cl.**[6] **H05K 7/20**

[52] **U.S. Cl.** **361/707**; 174/16.3; 165/80.3; 165/185; 257/719; 361/690; 361/715; 361/717; 361/719; 361/790

[58] **Field of Search** 174/16.3; 165/80.3, 165/80.2, 185; 257/718–719, 726–727, 686; 361/690, 704, 707–713, 714, 717–719, 723, 730, 735, 744, 790

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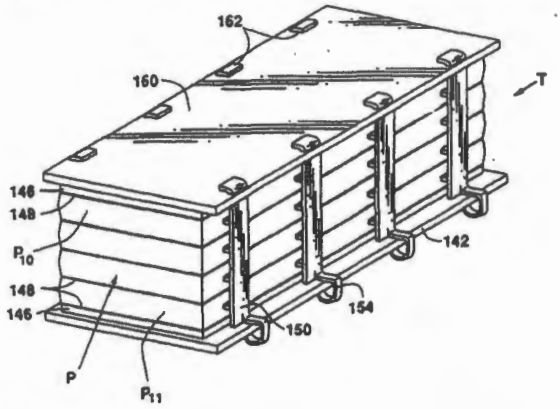
Primary Examiner—Gregory D. Thompson

Attorney, Agent, or Firm—Fulbright & Jaworski

[57] **ABSTRACT**

A multiple-element modular package is provided which includes a plurality of level-one packages in horizontal or vertical stacked configuration.

32 Claims, 15 Drawing Sheets



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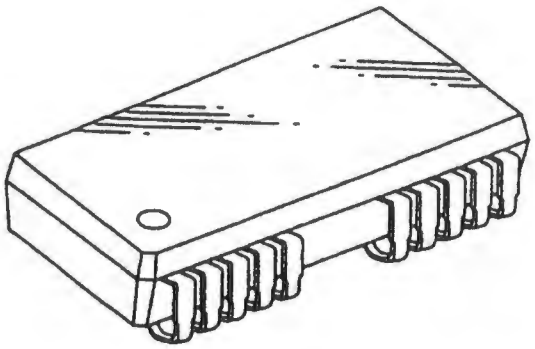

Fig. 1
(PRIOR ART)

Fig. 2
(PRIOR ART)

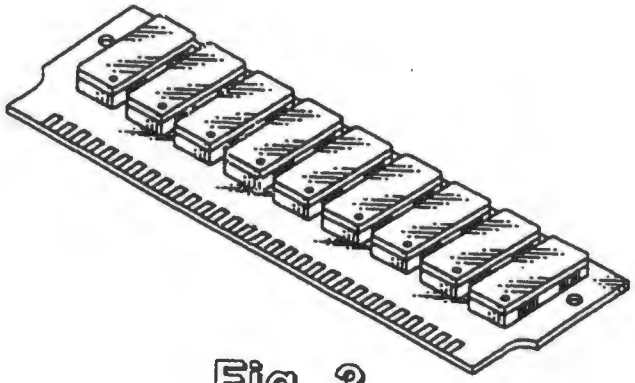

Fig. 3
(PRIOR ART)

Fig. 4

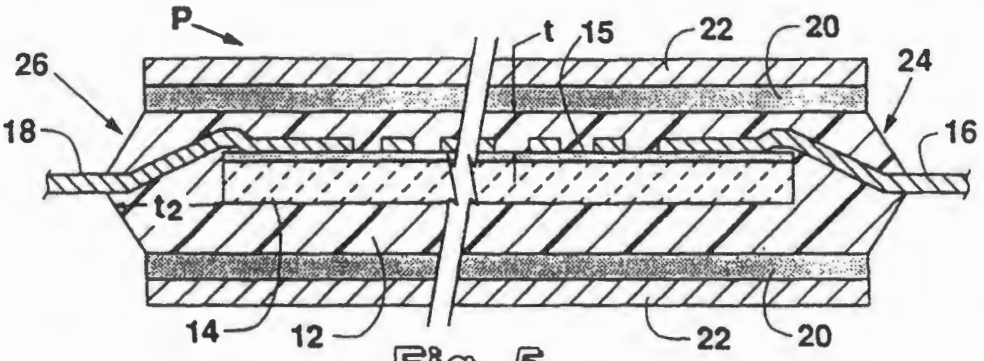

Fig. 5

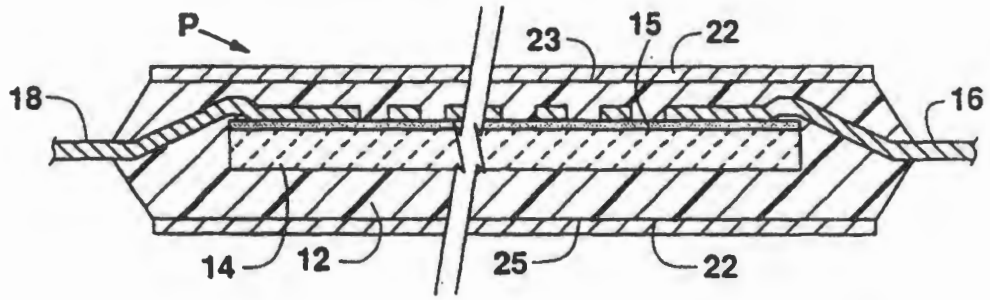

Fig. 6

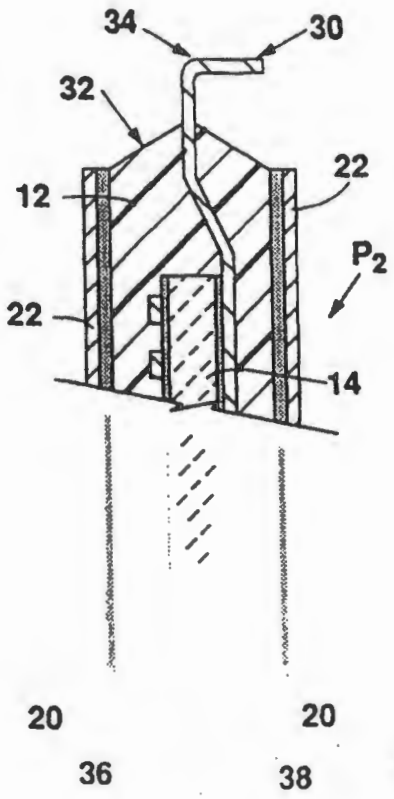

Fig. 7

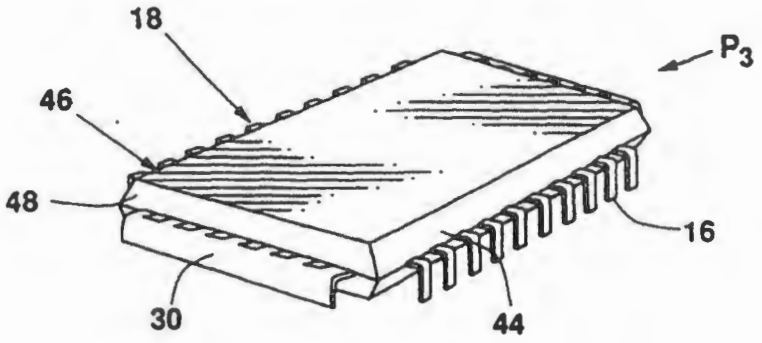

Fig. 8

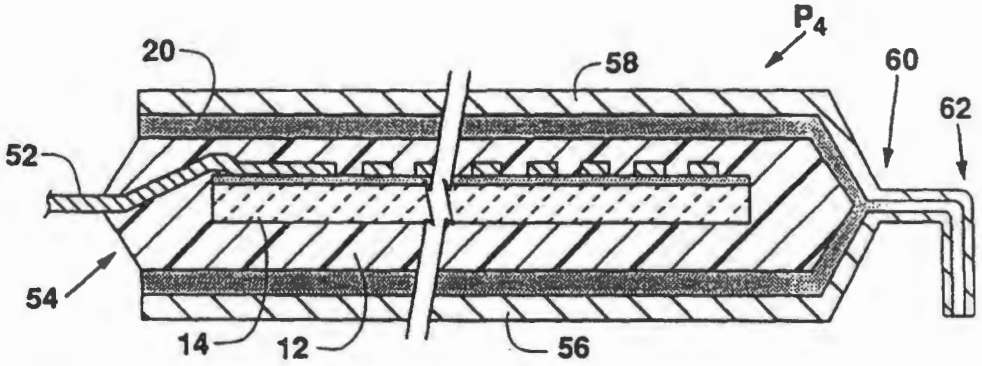

Fig. 9

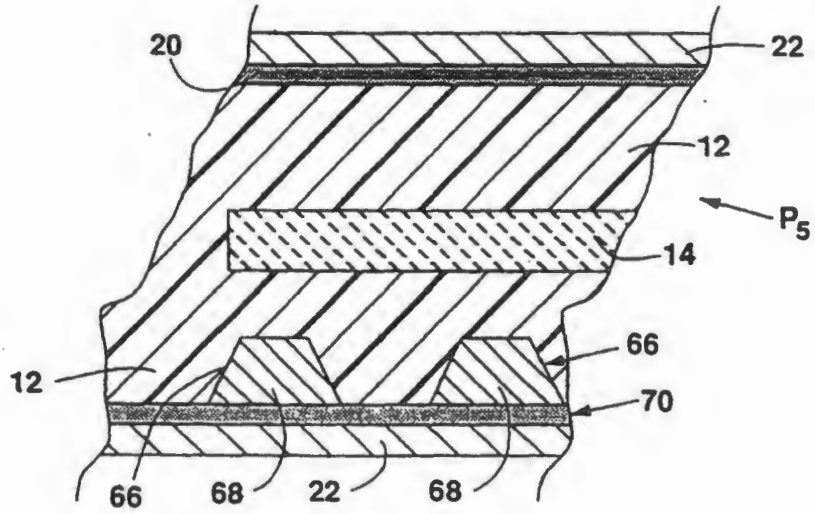

Fig. 10

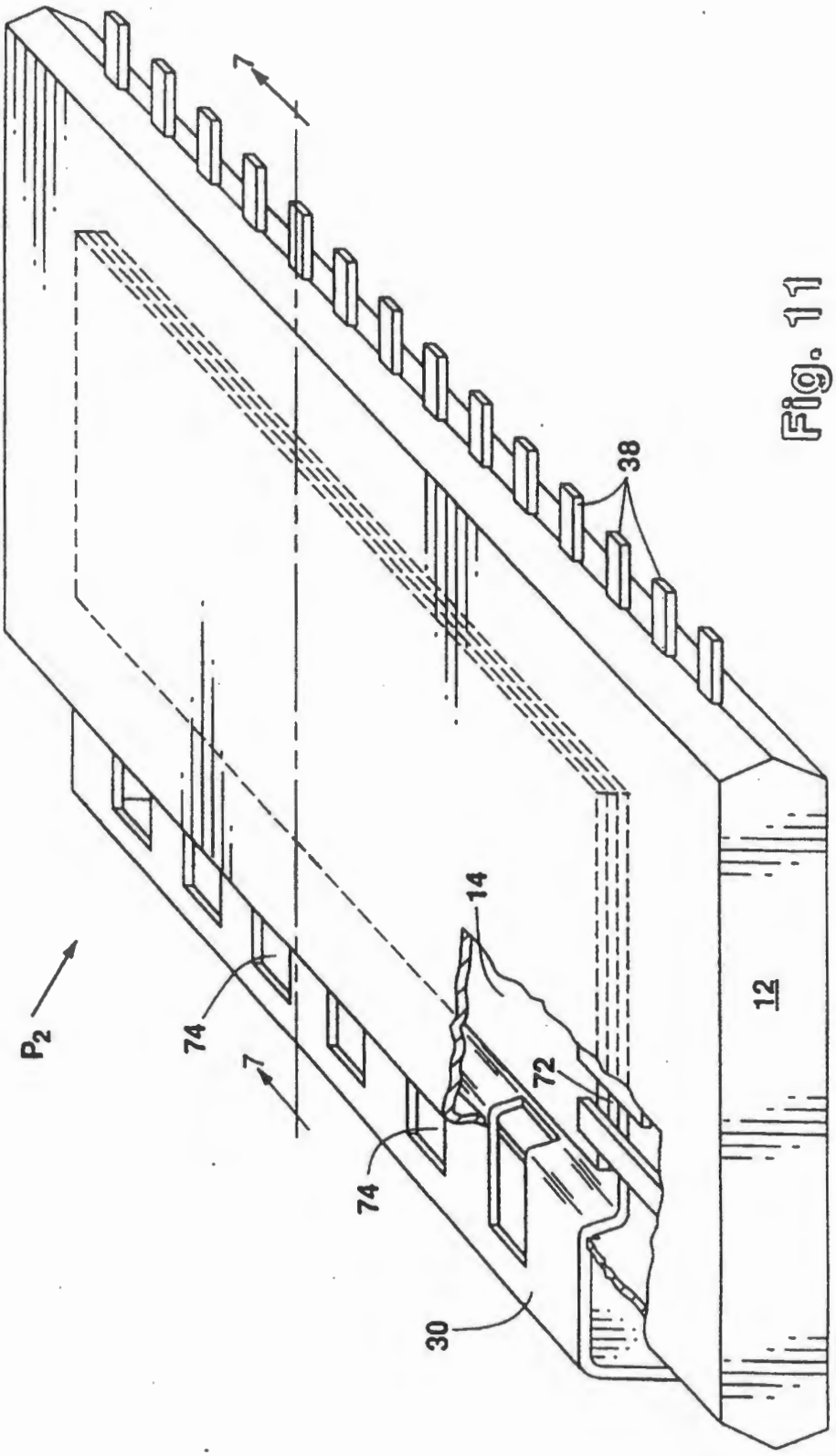

Fig. 11

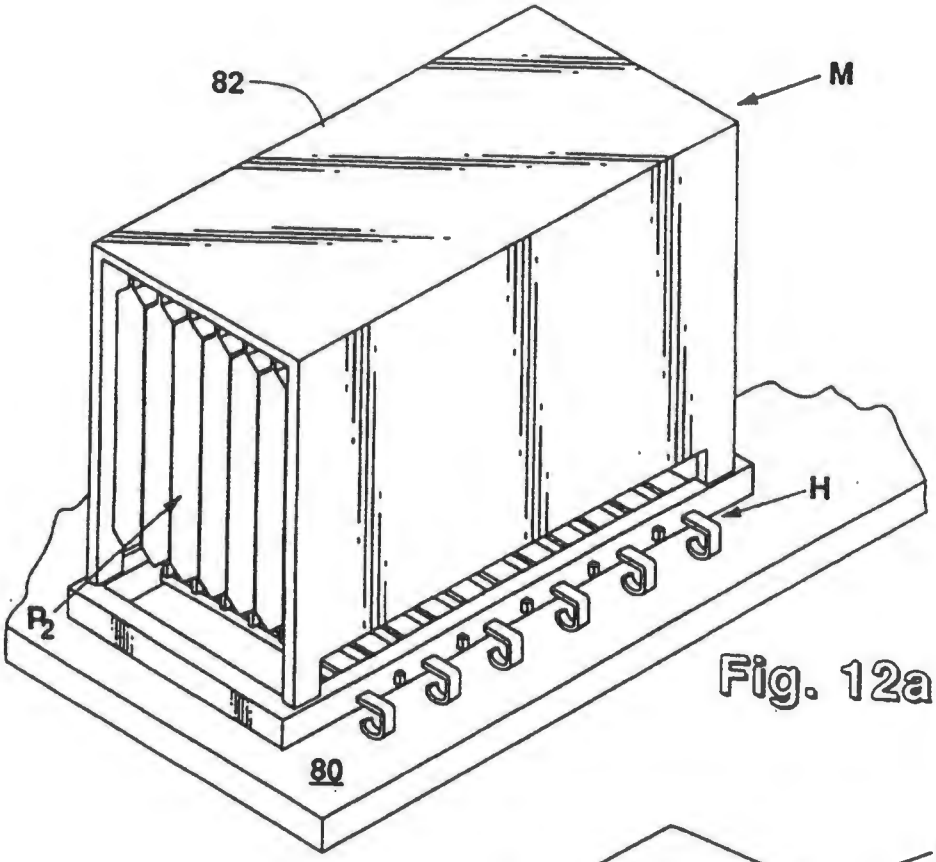

Fig. 12a

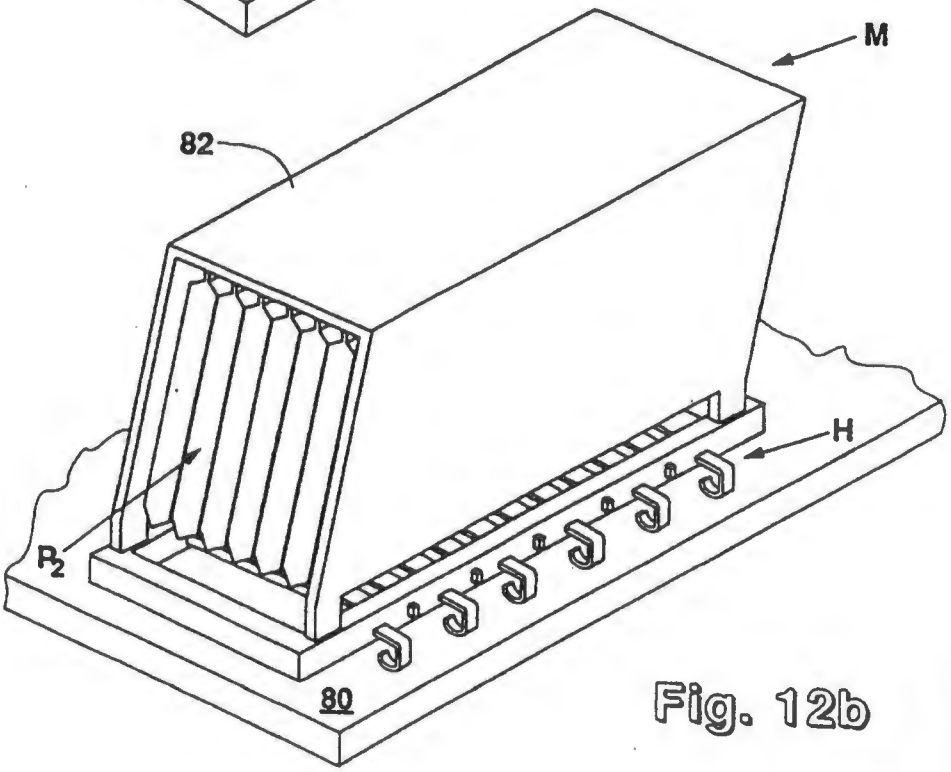

Fig. 12b

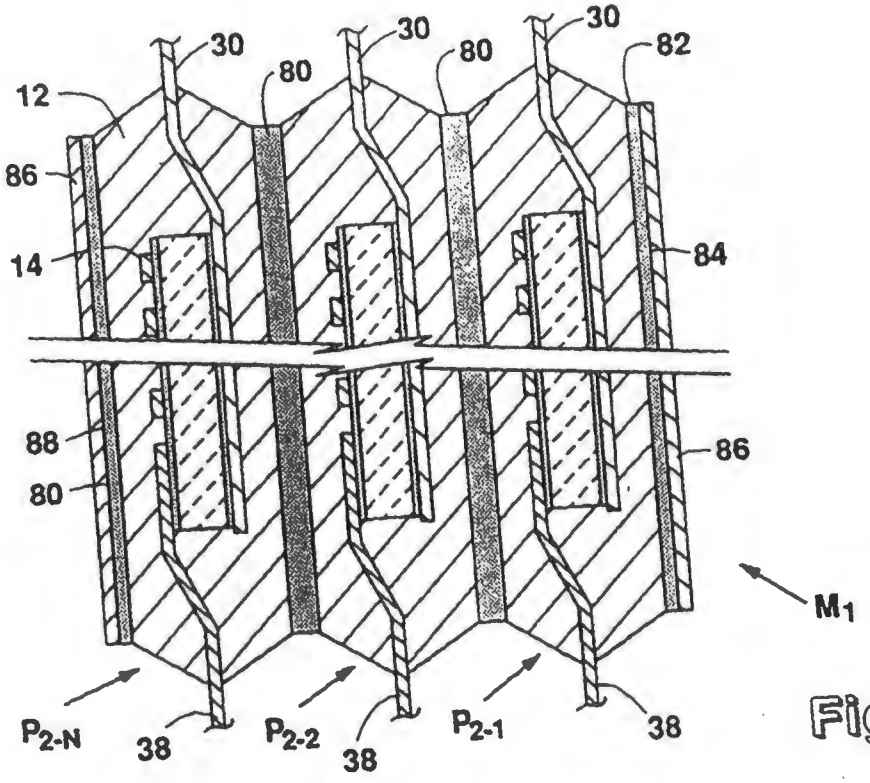
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Fig. 13

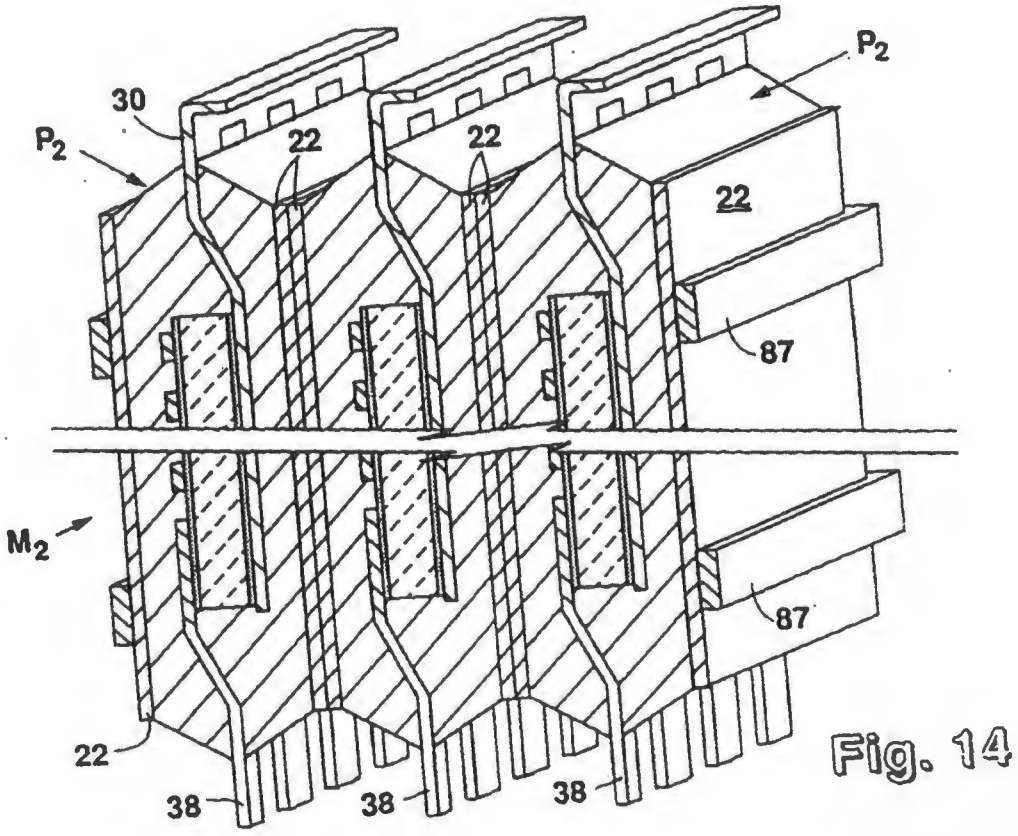
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Fig. 14

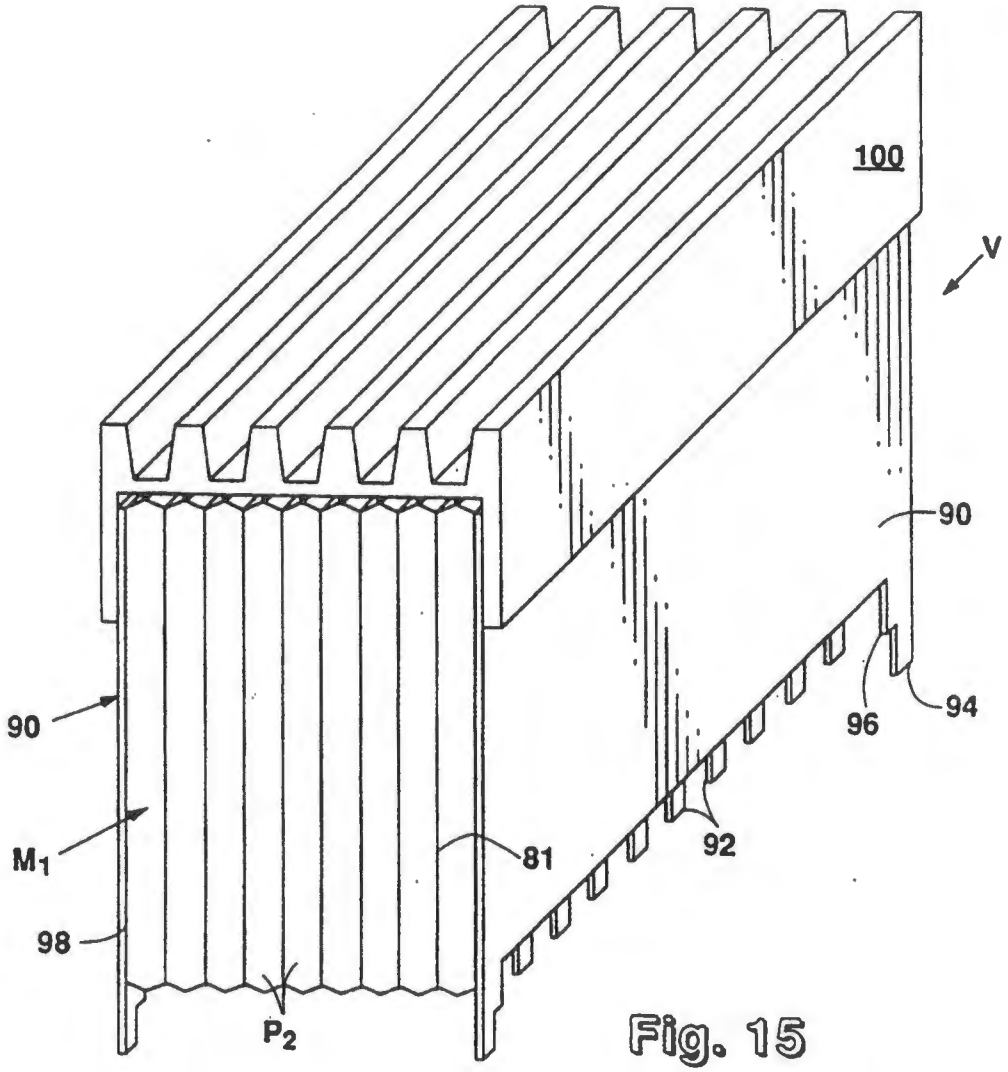


Fig. 15

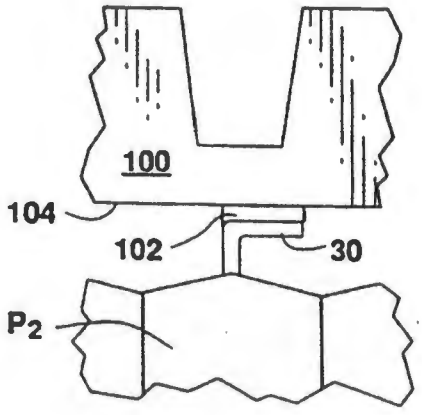


Fig. 15a

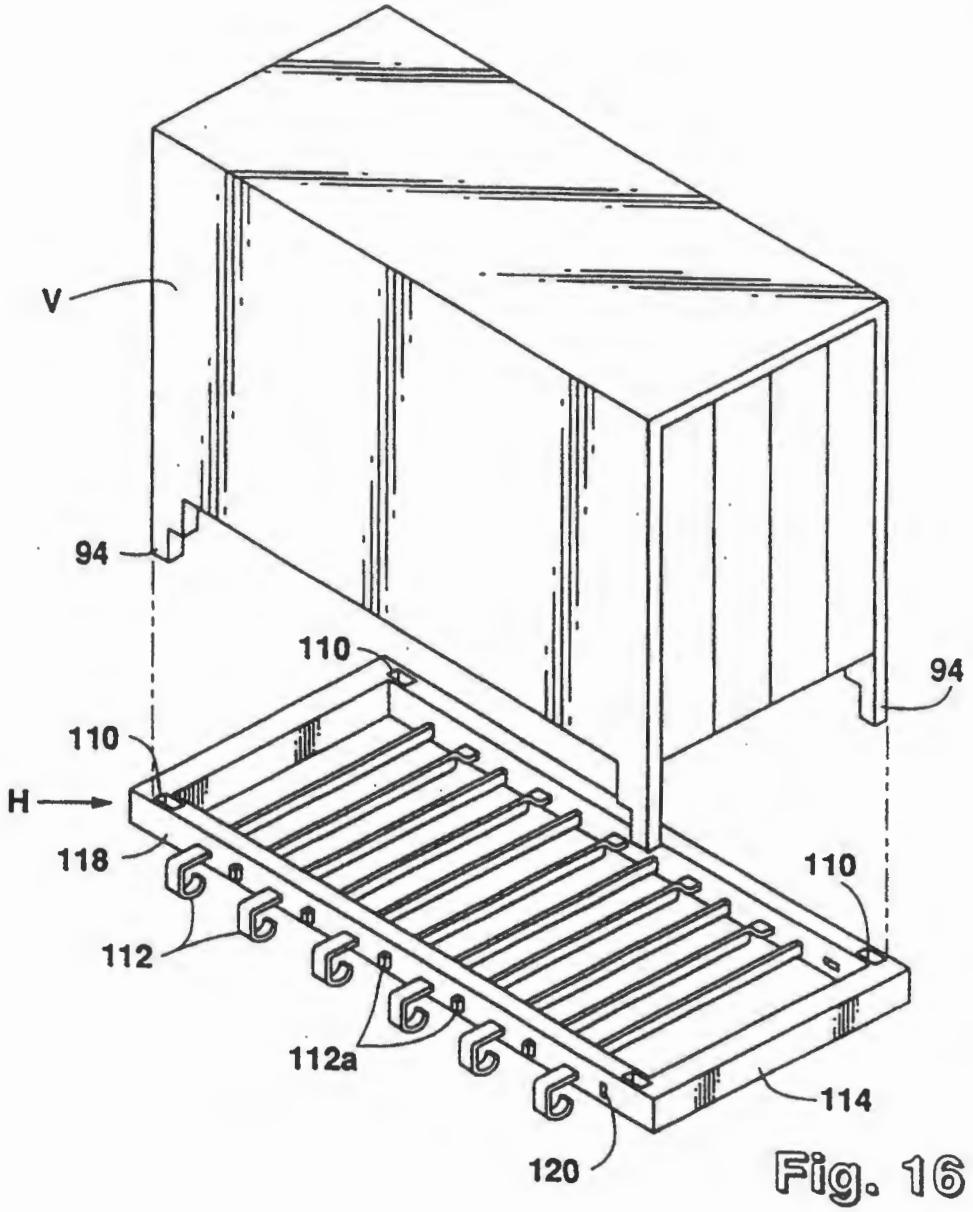


Fig. 16

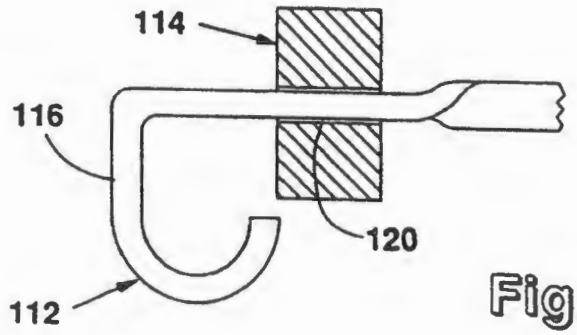


Fig. 16a

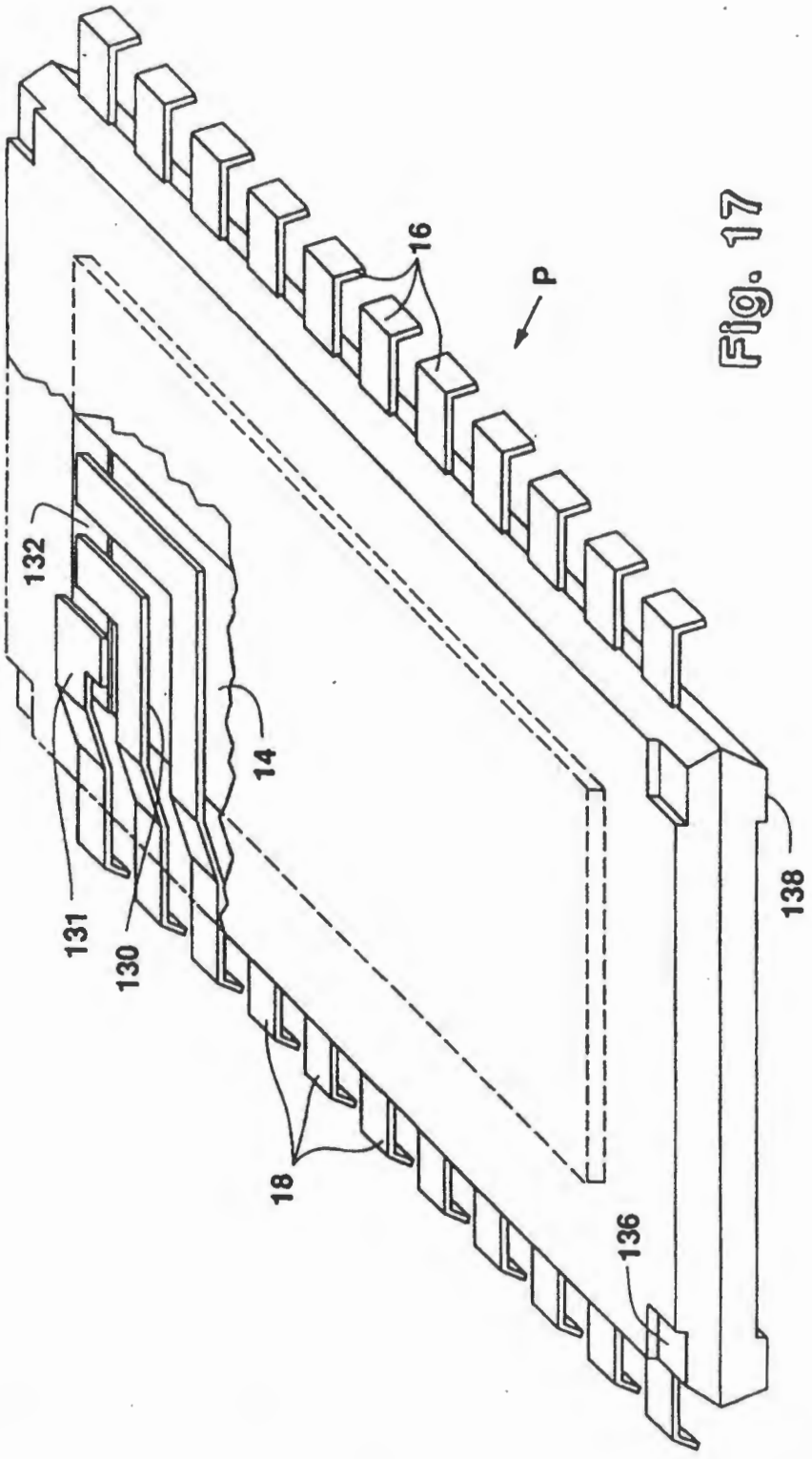


Fig. 17

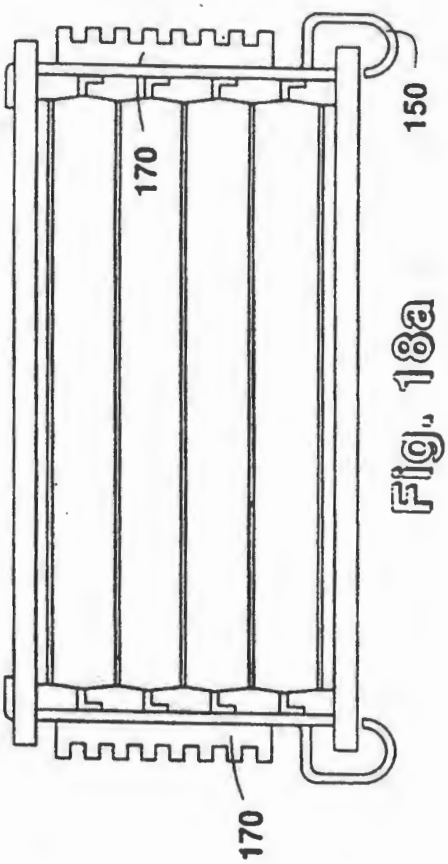


Fig. 18a

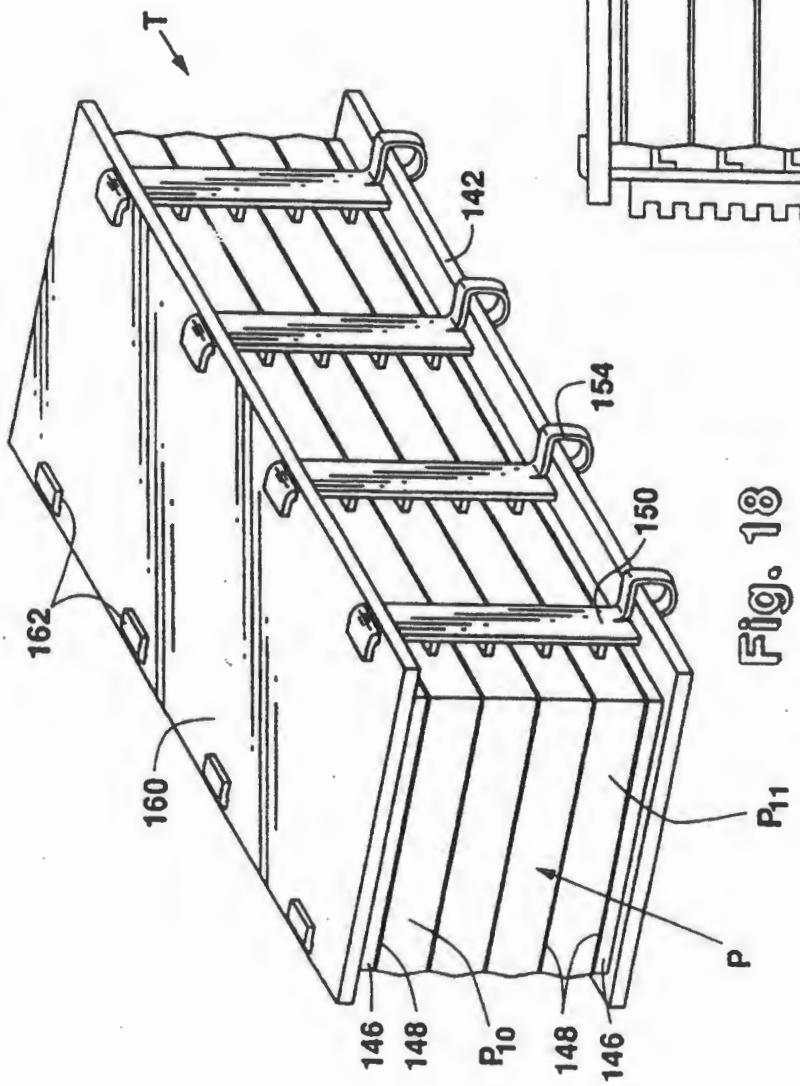


Fig. 18

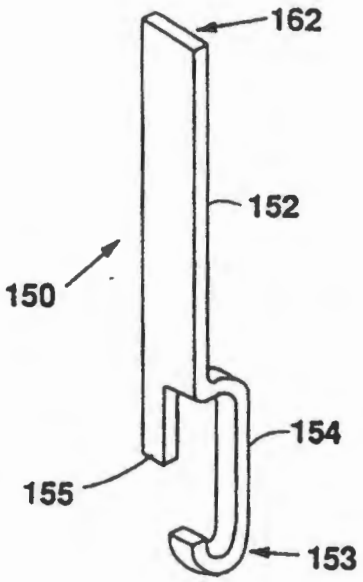


Fig. 19a

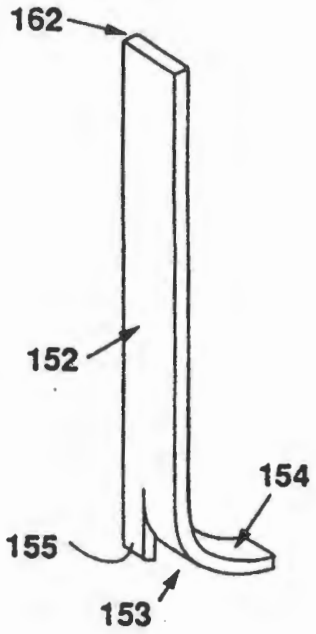


Fig. 19b

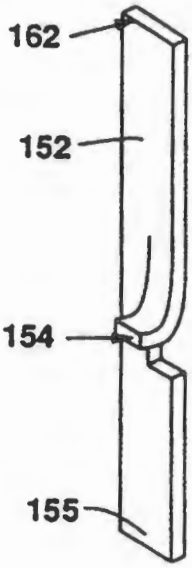


Fig. 19c

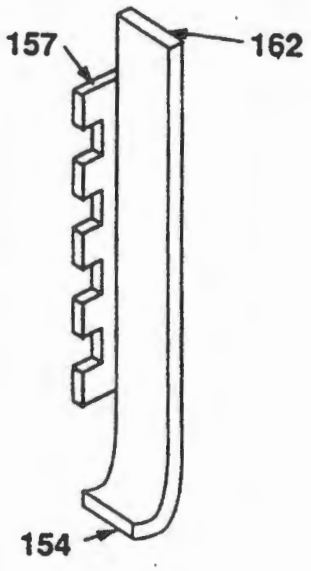
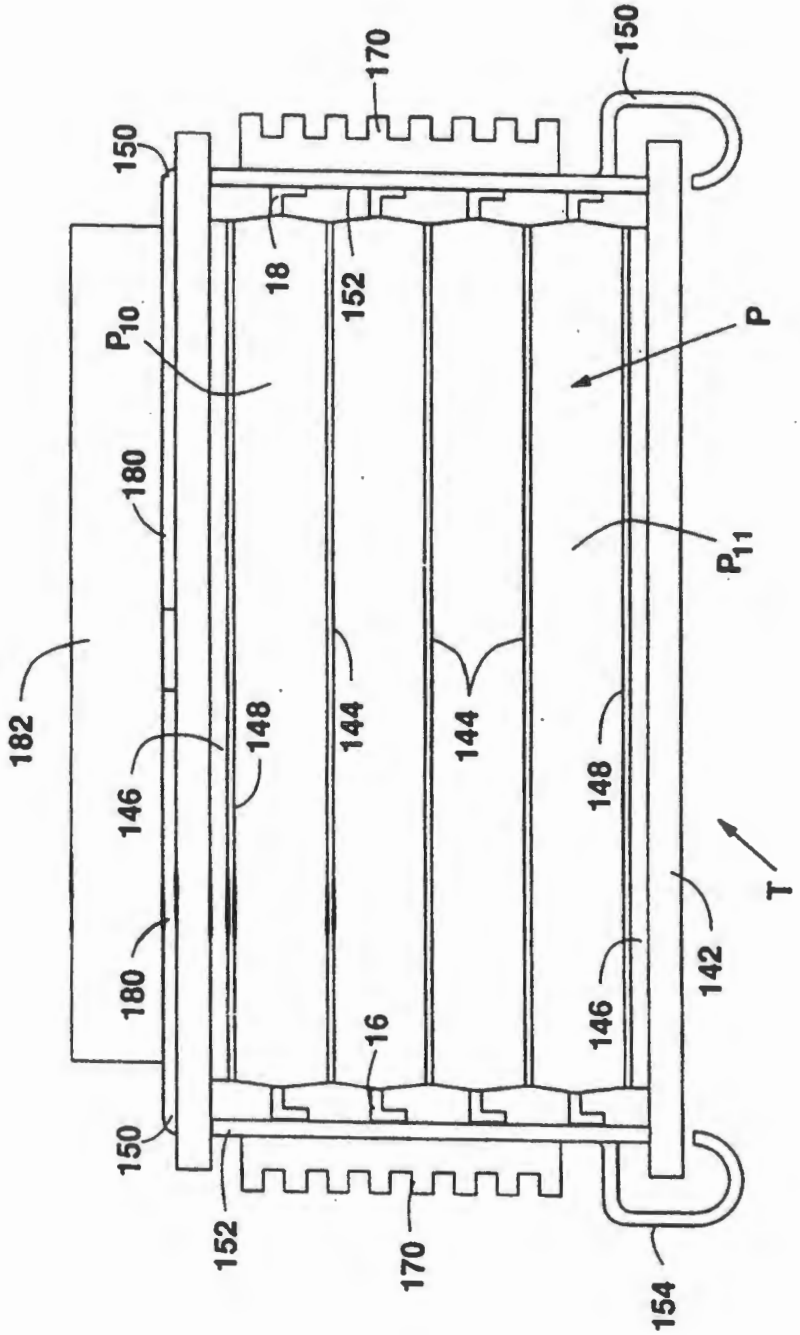


Fig. 19d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150
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18
152
P_{10}
P
180
P_{11}
182
148
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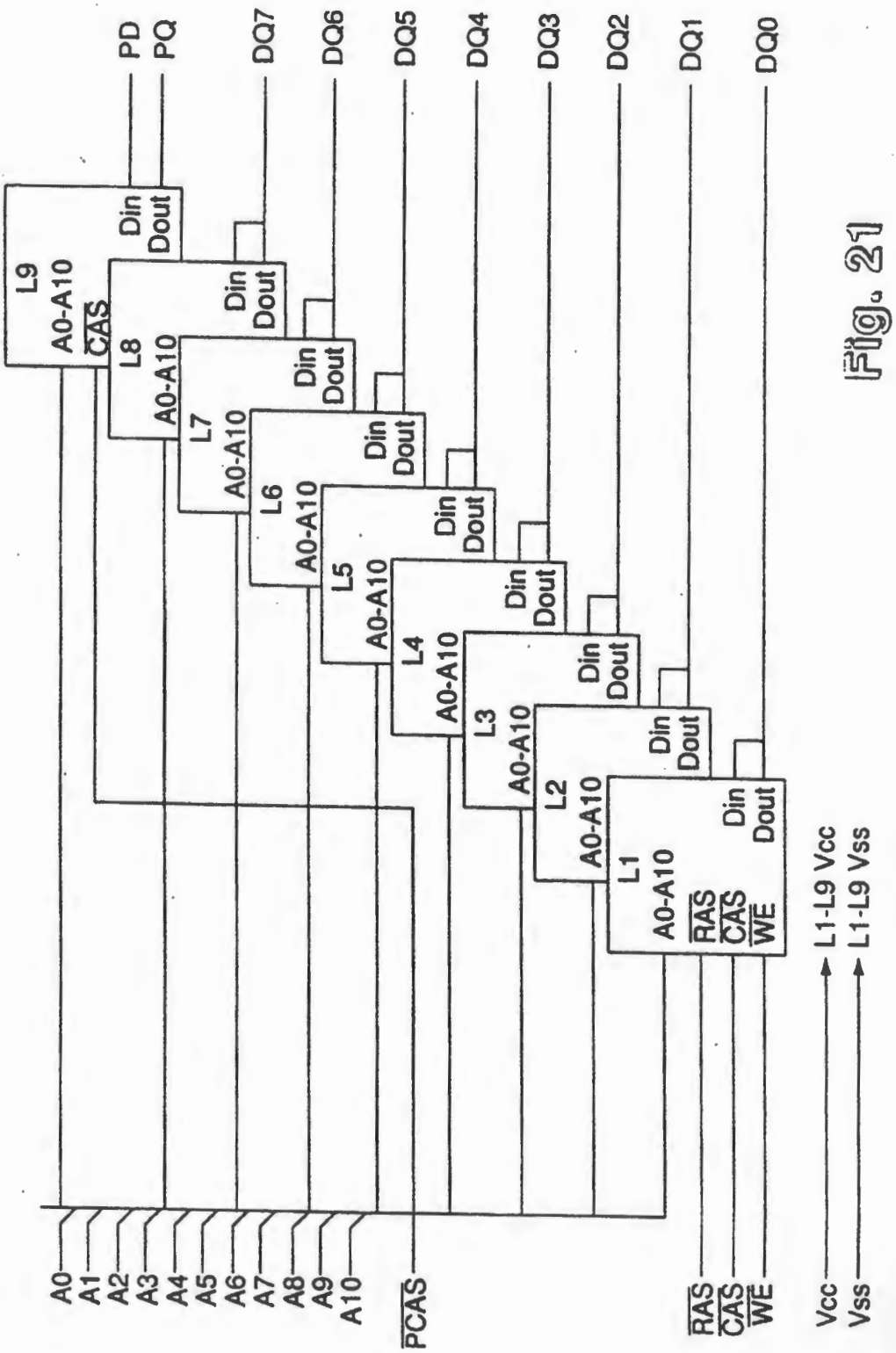
170
154

Fig. 20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L3
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RAS
CAS
WE
Din
Dout
A0
A1
A2
A3
A4
A5
A6
A7
A8
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PCAS
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CAS
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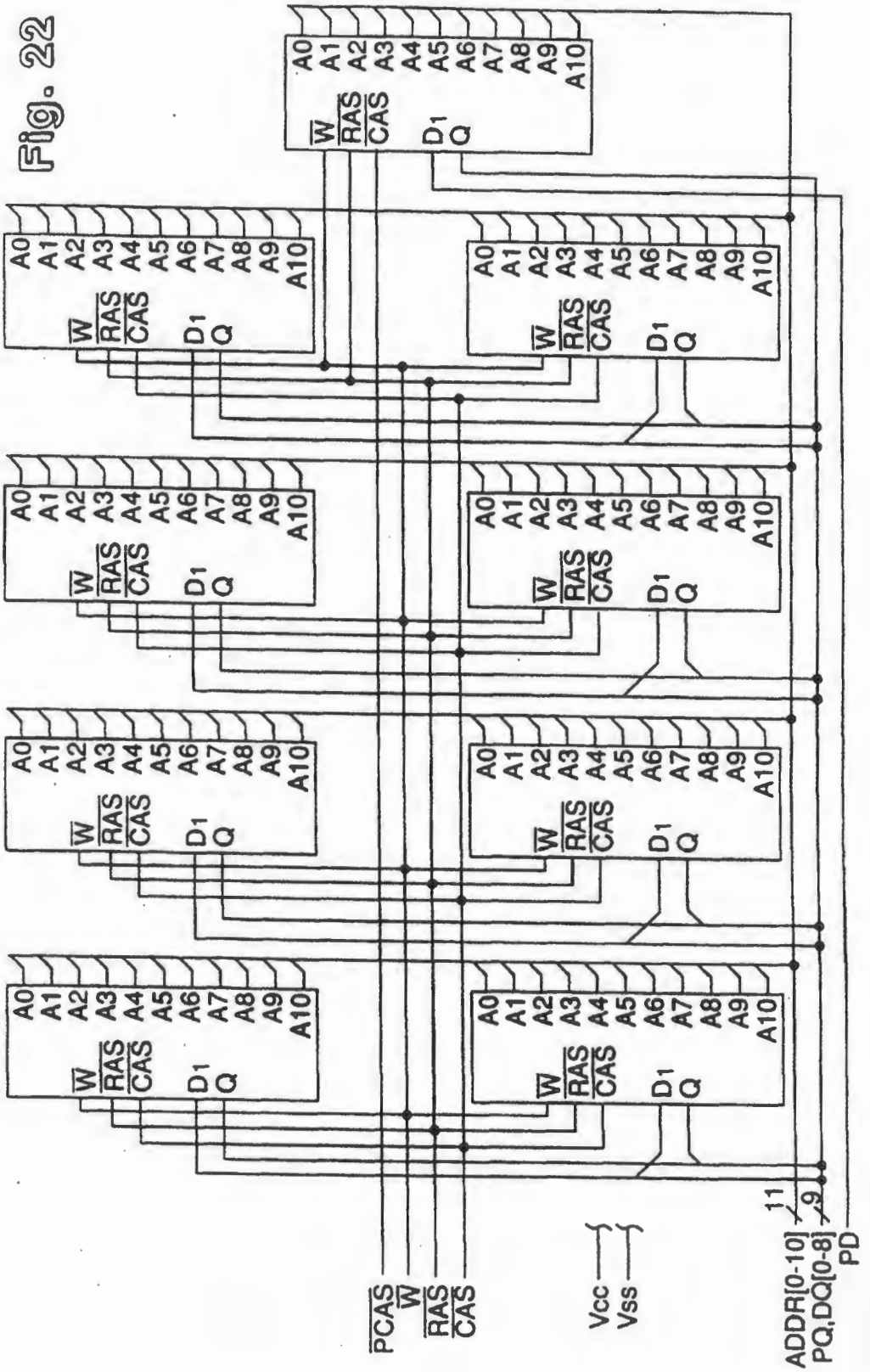
Vcc
Vss
L1-L9 Vcc
L1-L9 Vss

Fig. 21

Fig. 22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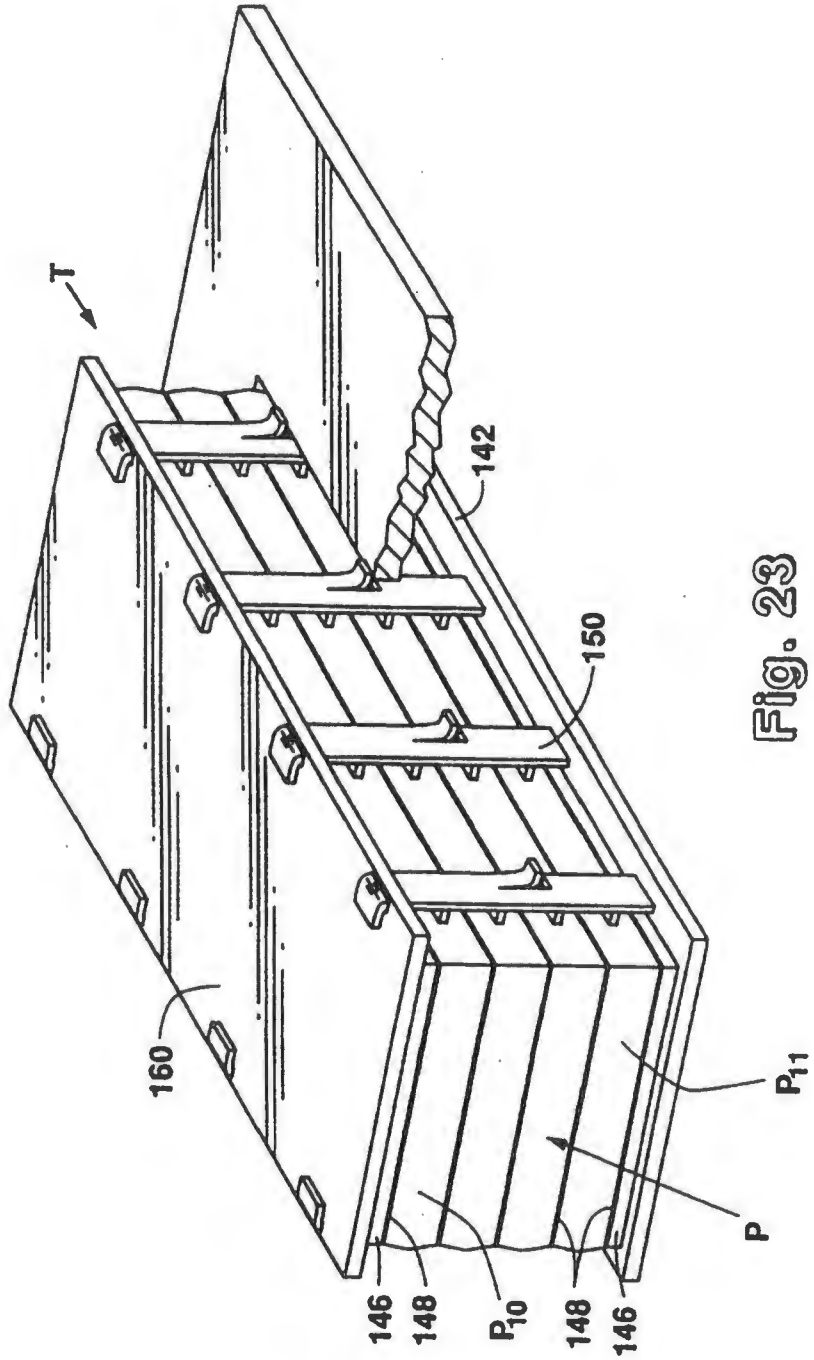

Fig. 23

ULTRA HIGH DENSITY MODULAR INTEGRATED CIRCUIT PACKAGE

This application is a divisional of application Ser. No. 07/561,417, filed Aug. 1, 1990, pending.

1. Field of Invention

This invention relates to a method and apparatus for achieving ultra high density integrated circuit packages incorporation a plurality of ultra-thin molded integrated circuit packages stacked and interconnected into an ultra-high density three-dimensional module.

2. Discussion of the Related Art

Packaging techniques for integrated circuits have been developed in the past in an attempt to satisfy demands for miniaturization in the semiconductor industry. Improved methods for miniaturization of integrated circuits enabling the integration of millions of circuit elements into single integrated silicon embodied circuits, or chips, have resulted in increased emphasis on methods to package these circuits in space efficient, yet reliable and mass producible packages.

The introduction of highly sophisticated integrated circuit microprocessors led to the rapid development of complex personal computers and other common bus systems utilizing a variety of integrated circuit elements such as memory devices (DRAMS, SRAMS), programmable logic arrays (PLAs), microprocessors (CPUs), coprocessors, and other related integrated circuit elements which had to be assembled, mounted and interconnected into as compact, yet reliable packages as feasible to satisfy the industry demands for miniaturization.

Other key considerations in developing packaging for such circuits have been the cost of manufacture, the reliability of the packaged device, heat transfer, moisture penetration, standardization of mounting and interconnect methods, and the ability to test and control the quality of the packaged devices.

In the past, one area of concentration for high density packaging has been memory devices such as SRAMS and, DRAMS prior systems typically utilized a transfer molded plastic encasement surrounding the integrated circuit and having one of a variety of pin-out or mounting and interconnect schemes. The older M-DIP (Dual-In-Line-Plastic) provides a relatively flat, molded package having dual parallel rows of leads extending from the bottom for through-hole connection and mounting to an underlying printed circuit board. These packages provided 100 mil spacing between leads.

A more dense package was the 100-mil SIP (Single-In-Line-Plastic) which was assembled on edge with two rows of 100-mil staggered leads extending from the bottom edge for through-hole assembly. Another popular prior art package is the PLCC (Plastic Leaded Chip Carrier) SOJ (Small Outline J-leaded) molded package with twenty surface-mount designed J-leads (length 0.67", width 0.34", height 0.14"). This prior art package is illustrated schematically in FIG. 1 and shown at approximate actual size in FIG. 2.

In order to obtain more density and provide lower cost socketability (i.e. removable mounting) and to allow for after-market sale of additional memory units the SIMM (Single-In-Line Memory Module) was developed. This package is schematically illustrated in FIG. 3. In this package typically nine one-megabyte or four-megabyte DRAMS are surface mounted into a socket which is in turn edge-mounted on a large printed

circuit board containing additional sockets or components. While this design provided some increase in density, it had the drawback of providing a module extending from one-half to nearly two inches vertically above the printed circuit board.

Newer, higher density versions of the SIMM design with even small versions of the DRAM-plastic package have been developed. These thinner versions of SOJ DRAMS are one-half the thickness (having a plastic packaging thickness of about 70 mils) of standard SOJ designs, and have been mounted on both sides of printed circuit boards. Even smaller TSOP packages have been developed experimentally with a plastic thickness of one millimeter and lower profile gull-wing leads for surface mounting. FIGS. 1–3 illustrate typical embodiments of some of these prior art packages. Based on experience with those prior art designs, for reasons of reliability related to moisture penetration and mechanical integrity the industry has adopted a standard thickness for plastic packaging of approximately one millimeter (40 mils), or approximately 10.5 mils on each side of a 19 mil thick integrated circuit element.

In contrast to such prior art systems, the packaging method of the present invention provides a reliable, cost efficient, easily manufacturable package with a plurality of ultra thin level-one package elements assembled in an integrated module or level-two package which can be mounted to a printed circuit board directly or via an underlying socket or header.

SUMMARY OF THE INVENTION

The present invention provides a level-one packaging method which enables the level-one elements to be packaged in transfer molded casing approximately 7 mils or less thick, encompassing an integrated circuit die element approximately eight to sixteen mils thick to produce a reliable level-one package less than thirty-two mils thick. These level-one units are then bound together mechanically or using an epoxy adhesive approximately one mil thick, with the outer surfaces of the outside level-one units having a thin metal foil adhered thereto or deposited using known semiconductor manufacturing methods such as vacuum deposition, sputtering or the like.

This packaging technique provides a high density module or level-two package with improved moisture resistance, and the lamination of multiple level-one elements together provides adequate structural rigidity to prevent intolerable flexing of the internal integrated circuit elements. Using the packaging technique of the present invention ultra dense reliable packages such as the nine megabyte DRAM shown at approximate actual size in FIG. 4 can be achieved.

In one form of a preferred embodiment, the level-one elements are configured with a single row of leads in either gull-wing or J-lead form for circuit board mounting and interconnect extending from one edge only,and having a heat sink conductive element which comprises a 2 oz. copper foil substrate in full surface contact with the internal integrated circuit die extending from the edge opposite the leads. The level-one elements are laminated together in a vertical array contained within a mounting package which includes metal side plates and a top heat sink element. The vertically extending metal side plates are provided with mounting tangs for attachment to a printed circuit board. Alternatively the level-one units can be laminated together at an angle to reduce overall height. Furthermore, the package can be

mounted to a rail header which in turn is mounted to the printed circuit board with J-leads or gull-wing leads for surface mounting. This latter embodiment provides visible solder connections for inspection.

A horizontally stacked module is also provided as an alternative form of the preferred embodiment, which utilizes similar level-one packages laminated together in a horizontal, module or level-two package. In this embodiment electrical interconnection and thermal conduction are provided by an array of vertically oriented conductive rails aligned with the vertical columns of leads, and extending from the top to the bottom of the stack. These rails can be configured with SMT gull-wing leads or J-leads for the package. Significant advantages are realized by incorporating an electrical signal bus and integral heat sink in the vertical rails which also provide structural integrity for the horizontal module. In all embodiments provision can be made for decoupling capacitors, control circuitry, self-contained power supplies as elements in the stack and configured with external heat sinking.

The computer systems of today and tomorrow are being designed with ever increasing clock rates. With the clock rates of personal computers approaching 50 MH_2, a single cycle memory access must be accomplished in 20 nano seconds (ns). If a static ram in a cache memory application has a 15 ns access time capability, only 5 ns is left to accommodate any gate and/or propagation delays to meet a single cycle memory access. A fast memory driver chip typically has a 3 ns gate delay, leaving 2 ns overhead. In a standard memory array assembled two dimensionally across an FR-4 type printed circuit board (PCB), the propagation delay could be larger than 2 ns and force a two cycle, 40 ns access, thus greatly affecting the overall system performance. The three-dimensional modular approach described herein provides for significantly shorter, lower impedance and reactance, routing paths to the memory arrays, and the potential to support a single-cycle access.

A unique feature of the horizontally oriented level-two module or package is the relatively large cross-sectional area of the rails connecting the leads of the level-one packages. These rails act as excellent low impedance buses for both electrical current flow and thermal heat transfer. The low electrical impedance provides for less ground bounce, less signal distortion, and improved signal integrity. The low thermal resistance allows for improved heat transfer from the die interior, which provides increased reliability and longer operating life for some embodiments, and in ultra-high density embodiments provides a package that can be adequately heat compensated with conventional convection techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1–3 illustrate prior art packaging for integrated circuits;

FIG. 4 is a schematic illustration of a modular package of the present invention shown at approximate actual size;

FIG. 5 illustrates the level-one design of the present invention in schematic cross-section;

FIG. 6 illustrates an alternative embodiment of the level-one package of the present invention in schematic cross-section;

FIG. 7 illustrates a vertically oriented embodiment a level-one package according to the present invention in schematic cross-section;

FIG. 8 illustrates a horizontal stack embodiment of a level-one package of the present invention having an integral heat sink;

FIG. 9 illustrates in schematic cross-section an alternate vertical embodiment of a level-one package according to the present invention;

FIG. 10 illustrates in partial cross-section an alternative embodiment of a level-one package according to the present invention which includes integral heat transfer elements formed in the package casing;

FIG. 11 is an isometric illustration of a vertically oriented level-one package according to the present invention;

FIGS. 12*a, b* illustrate vertically oriented modular level-two packages according to the present invention;

FIG. 13 illustrates an alternative vertically oriented embodiment of a portion of a modular or level-two package according to the present invention;

FIG. 14 illustrates an alternative embodiment of a portion of a modular or level-two package according to the present invention;

FIG. 15 illustrates a modular level-two vertically oriented package including a plurality of level-one packages and an external heat sink; p FIG. 15*a* illustrates assembly details of the package illustrated in FIG. 15;

FIG. 16 illustrates an alternative method and apparatus for assembling a modular, vertically oriented level-two package to a printed circuit board;

FIG. 16*a* illustrates assembly details for the package shown in FIG. 16;

FIG. 17. is an isometric illustration with a partial cut-out view of a horizontally oriented level-one package according to the present invention;

FIG. 18 is an isometric view of a horizontally oriented modular level-two package according to the present invention;

FIG. 18*a* is an alternative view of the embodiment illustrated in FIG. 18;

FIGS. 19*a, b, c* and d are isometric views of alternative embodiments of conductive rails used in horizontally oriented embodiments illustrated in FIG. 18;

FIG. 20 illustrates an alternative embodiment of a horizontally oriented modular or level-two package according to the present invention;

FIG. 21 is a schematic illustration of one method for electrical signal busing of the level-one packages in a modular, level-two package according to the present invention;

FIG. 22 is a schematic illustration of electrical signal busing for a four megabyte plus parity DRAM module;

FIG. 23 is an isometric view of a alternative embodiment of a level-two package according to the present invention adapted for mounting within an orifice formed in a printed circuit board.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A better understanding of the present invention can be had when the following detailed description is read with reference to the drawings wherein common elements are designated with like numbers or letters. Referring now to FIG. 5, a typical level-one package is illustrated in cross-section. Package P comprises a transfer molded casing 12 surrounding the integrated

circuit die 14, which is provided with an array of leads 16 and 18 for circuit interconnection. The level-one package P is formed using conventional, proven manufacturing techniques such as transfer molding and automated tape bonding, or low-profile ribbon or wire bonding to a lead frame, yet achieves substantial reduction in thickness without sacrificing circuit integrity.

Package P includes a silicon integrated circuit die element 14 having a nominal thickness of from about eight to about sixteen-inils. Die 14 is provided with an array of conductive leads 16 and 18 for circuit interconnect which are attached to die 14 in the manner described above. Leads 16, 18 are laid over a semiconductor grade epoxy insulating layer 15 which covers die 14 in a conventional manner. It should also be noted that in some of the drawings leads 16, 18 are illustrated as being connected at or near the edge of die 14 for clarity, whereas in automated bonding the connection pattern is more complex. It should be noted that the present invention is not limited to embodiments having leads exiting at two sides and can be readily fabricated to accommodate single or four sided lead configuration, in either J-lead, gull-wing or other surface mount technology (SMT) lead configurations.

Die 14 is encased in a transfer molded case 12 which may be formed of any suitable commercially available high-temperature semiconductor grade thermosetting plastic such as a filled NOVOLAC material. The casing material should be selected for high temperature, tolerance, moisture control, mechanical rigidity, and chemical and therman compatibility with the silicon die 14. In the preferred embodiment, casing 12 is made of a semiconductor grade, low stress, filled, transfer molding compound including a NOVOLAC-type epoxy.

For reasons explained below, case 12 is formed so as to have a thickness t of approximately five to seven mils. In one embodiment, after case 12 is formed, a layer of moisture resistant, high glass transition temperature epoxy 20 is applied over the upper and lower surfaces of case 12. Epoxy 20 should be selected to be suitable for curing at approximately 150° C. and endure 250° C. in subsequent manufacturing steps without reflowing. Epoxy layer 20 is applied in a thickness of one-half to one mil, and is preferably applied in a preformed film or B-stage form. A suitable epoxy is an acrylic NOVOLAC-type epoxy with plasticizers.

After the application of the epoxy layer 20, the package P is provided with an outer metal foil layer 22 applied over the B-stage epoxy 20. Alternatively, the epoxy layer 20 can be applied to foil 22 and both layers applied to the casing at once. Foil 22 can be aluminum or copper or other suitable metallic foils approximately one-half to one mil thick. The completed level-one package P is therefore approximately forty-five percent to eighty percent of the thickness of prior art packages. In the package of the present invention, the epoxy and foil laminations prevent moisture penetration, and in some applications provide sufficient structural rigidity so as to allow construction of an ultra-thin package while still preventing undesirable flexing of the die 14. Protection against moisture penetration is achieved because moisture can only penetrate from lead edges 24 and 26 and the distance t_2 from edges 24 and 26 to die 14 is greater than twenty-five mils.

Referring now to FIG. 6, an alternative embodiment of a level-one package P is schematically illustrated in cross-section. In this embodiment, package P includes a die 14 surrounded by a transfer molded casing 12 Of the type previously described. Leads 16 and 18 are tape or ribbon bonded to die 14 in the conventional manner. This embodiment does not include an epoxy layer 20 as in the previous embodiment, but instead only includes a thin (one-half to ten microns thick) metal foil lamination 22 formed of aluminum or copper foil adhered, vacuum deposited, or otherwise applied on surfaces 23 and 25 of casing 12.

Referring now to FIG. 7, a vertical stack embodiment of a level-one package P_2 is illustrated in schematic cross-section. Embodiment P_2 is configured to have an integral full-surface contact conductive heat sink element 30 mounted to one surface of die 14, Element 30 is formed of aluminum or copper 1.4 mil to 2.8 mil thick which is surface-mounted to die 14 using a semiconductor grade, metal-filled heat conductive epoxy layer 15. Element 30 extends from one end 32 of package P_2 and is bent to form a heat sink end 34 shaped to dissipate heat by convection or to be attached to a larger heat sink element (not shown) it should be noted that end 34 of heat sink 30, as well as other lead type extensions from the level-one packages should be formed of flexible material and extend far enough from the package to avoid unduly stressing the package or the die connection when the package is mounted to external electrical or mechanical supports. Extension of seven to eight mils in addition-to any connection length required is sufficient for these purposes.. In this embodiment all leads 38 extends from edge 36 of package. P_2. While in FIG. 7 package P_2 includes a transfer molded casing 12, an epoxy lamination layer 20 and foil lamination layers 22 as in the previous embodiment shown in FIG. 5, this integral heat sink embodiment could be just as readily formed without epoxy layer 20 as illustrated in FIG. 6.

Referring now to FIG. 8, a horizontal stack embodiment P_3 is illustrated in schematic isometric form. In this embodiment, leads 16 and 18 extend from sides 44 and 46 and are attached to die 14 (not shown) in the manner described above. Heat sink element 30 is surfaced mounted to die 14 in the manner described above with reference to FIG. 7, and brought out of end 48 of package P_3 for independent heat dissipation or for attachment to a larger heat sink element. Alternatively, in either the vertical embodiment P_2 or horizontal embodiment P_3 heat transfer can be achieved without element 30. In these embodiments, heat is transferred from die 14 through casing 12, epoxy layer 20 and foil layer (FIGS. 5 and 6).

Yet another alternative, level-one embodiment is illustrated in FIG. 9. In this embodiment (shown in vertical stack configuration) all circuit leads 52 extend from end 54 of package P_4. Package P_4 includes casing 12, die 14, and optional epoxy layer 20 as in previous embodiments. In package P_4 foil layers 56 and 58 wrap around end 60 of package P_4 and are joined together to form a heat sink element similar to element 30 of FIG. 7. Foil layers 56 and 58 are epoxy-bonded to package P_4 and to each other at end 62 using-a one half. mil epoxy layer of the type previously described.

Further improvement in heat transfer from die can be achieved in the manner illustrated in FIG. 10. In a this embodiment, package P_5 includes a die 14, case 12, optional epoxy upper layer 20 and foil layers 22 as previously described. To achieve greater heat transfer from die 14, cavities 66 are formed in case 12 and filled with thermally conductive epoxy material 68. Below that, an epoxy adhesive layer 70 is formed about one-

half mil thick to which foil layer 22 is adhered. This enhanced heat transfer embodiment may be incorporated into any of the previously described embodiments.

Referring now to FIG. 11, the preferred level-one vertical stack embodiment of package P_2 (FIG. 7) is shown in schematic isometric form with partial cutaway views. In this drawing, heat sink element 30 is formed as a conductive sheet, surface mounted to die 14 via a layer of metal-filled, semiconductor grade heat transfer epoxy 72. Element 30 is formed having a plurality of slots 74 cut from element 30 prior to fabrication of package P_2. While not shown in precise scale, slots 74 are formed so as to relieve stress in transfer molding casing 12. In this manner, casing 12 is formed around leads 38 and through slots 74 of heat sink element 30.

Level Two Packaging

Another aspect of the present invention relates to the manner in which level-one packages, in either vertical or horizontal configuration can be assembled into a multi-element, modular level-two package or stack for mounting to an underlying printed circuit board.

Referring now to FIG. 12, various vertical stack embodiments are schematically illustrated. In FIG. 12*a*, a level-two package M is formed of a plurality of vertically oriented level one packages P_2 and mounted to an underlying printed circuit board 800. The details of the assembly and mounting of package M are described below. An alternate embodiment which reduces the overall height of package M is illustrated in FIG. 12*b*. In this embodiment, package M and the constituent level-one packages P_2 are inclined at an angle to reduce overall package height. In both of these embodiments, package M includes a metal or otherwise heat conductive and electrically insulated outer casing 82 formed of a continuous sheet of metal approximately six mils thick.

Referring now to FIG. 13, an alternate embodiment of a portion of a vertical stack assembly of package M is illustrated. A plurality of level-one packages P_2 are assembled by applying epoxy bond 80 between each element P_2. It should be noted that while only three elements P_2 are illustrated for clarity, a typical package M would include eight or nine level-one elements P_2. Each element P_2 includes a die 14, a case 12, lead elements 38 and heat sink elements 30 as previously described.

In this embodiment, each element P_2 is individually manufactured and tested without applying exterior epoxy layer 20 or foil layer 22 (FIG. 7). Thereafter, on a first element $P_{2\text{-}1}$ (FIG. 13) an epoxy layer 82, similar to layer 20 described above, is applied to one surface of a conductive foil layer 86, and the combined lamination of layers 82 and 86 is adhered surface 84. After testing element $P_{2\text{-}1}$, a second layer of epoxy 80 is applied to the second, opposite side-of element $P_{2\text{-}1}$, and a second level-one package $P_{2\text{-}2}$ is attached to package $P_{2\text{-}1}$. Thereafter, the combined element formed of packages $P_{2\text{-}1}$ and $P_{2\text{-}2}$ is tested. Further elements $P_{2\text{-}3}$, through $P_{2\text{-}7}$ for example, are similarly assembled. The last element $P_{2\text{-}N}$ is adhered to the preceding element in the same manner. An epoxy layer 80 and a conductive foil layer 86 is then applied to the outside surface 88 of the last element $P_{2\text{-}N}$ to complete the assembly. The assembled level-two unit M_1 (FIG. 13) thereby includes a number of level-one elements bonded together in laminated fashion, having conductive foil layers applied to the .exterior flat surfaces of the outside elements in the stack. This lamination provides improved resistance to moisture penetration and enhances the structural rigidity of the package as a whole enabling thinner individual circuit elements P_2 to be used without sacrificing circuit integrity.

Alternatively, a plurality of level-one elements P_2 can be mechanically bound together rather than epoxy bonded. Referring now to FIG. 14, each element P_2 is provided with only exterior foil layers 22. The individual packages P_2 are mechanically bound together with any suitable means such as a tie 87 or a housing 82 as shown in FIGS. 12*a* or 15 surrounding the package M_2.

Assembled stacks M_1 or M_2 may be mounted in an exterior package V as illustrated in FIG. 15. Package V includes an exterior casing 90 which is a metal formed shield which may be in two pieces (FIG. 15) or may be a single piece traversing over the top of stack M_1 (numeral 82, FIG. 12*a*). Casing 90 is formed of sheet metal approximately six mils thick. Casing 90 also includes at each of the four corners of package V a printed circuit board mounting tab or locating pin 94 having an expanded portion midway on its length to from a height setting tab 96 to position package V above an underlying printed circuit board or header as described below.

In this embodiment, the individual level-one elements P_2 are either epoxy bonded together with a one mil thick epoxy layer 81 or mechanically bound together as previously described. Stack M_1 or M_2 may be adhered to casing 90 with an approximately one mil thick epoxy bond between outside surfaces of the stack M_1 or M_2 and interior surfaces of casing 90, or mechanically attached using any suitable clamping method.

Package V also includes a u-shaped heat sink element 100 formed of heat conductive material and shaped to fit snugly over the assembled stack M_1 and casing 90 so as to form an upper cap for package V. When affixed to package V heat sink 100 provides structural rigidity as well as heat transfer capability. Heat sink 100 is bonded to level-one heat sink elements 30 (FIG. 15*a*) via conductive epoxy bond 102. Prior to assembly, elements 30 of each element P_2 are uniformly bent to provide a relatively coplanar bonding surface for heat sink 100. The under surface 104 of heat sink 100 is coated with B-stage conductive epoxy and pushed onto the partially assembled package V so that surface 104 contacts each of the P_2 heat sink elements 30. Thereafter heat is applied to complete the bond 102.

Referring now to FIG. 16, the preferred method and apparatus for mounting package V to an underlying circuit board is illustrated. In this embodiment, package V is mounted to a preformed plastic non-conductive header H which is subsequently mounted to a printed circuit board to provide socket-type mounting. In this embodiment, package V is mounted to header H via mounting tabs 94 which fit into preformed holes 110 in header H.

Header H includes a rectangular frame 114 provided with a number of J-lead or gull-wing configured leads 112 which span the width of frame 114 and are uniformly spaced along two opposite sides of the perimeter of frame 114 consistent with industry standard spacing. Frame 114 is formed of high temperature plastic or transfer molding compound such as RYTON. Leads 112 extend from the perimeter of frame 114 as shown in detail in FIG. 16*a*. Leads 112 may be formed in conventional J-lead, gull-wing or other surface mount configuration as required. To provide dual-in-line lead configuration, alternating leads 112*a* (FIG. 16) are configured

to have the J-lead or terminal portion 116 on the opposite side of frame 114 as leads 112, with the non-terminal ends being flush with the exterior surface 118 of frame 114.

Leads 112, 112a are formed of approximately five-mil copper having a rectangular cross-section. Leads 112, 112*a* are mounted in frame 114 through preformed rectangular slots 120. The portion of leads 112, 112*a* within slots 120 are horizontally configured, and the portion within the interior of frame 114 are rotated or twisted ninety degrees to be vertically oriented (Fig. 16*a*). To facilitate mounting package V, leads 112, 112*a* are plated or solder-coated for subsequent attachment to individual leads 38 which are pre-treated with solder paste, just prior to assembly.

In assembly, stack V is mounted to header H by insertion of tabs 94 into holes 110. Tabs 94 are then bent or glued-to header H to temporarily hold stack V in place while leads. 38 are soldered to leads 112 / 112*a*. This configuration provides socket mounting-and visible solder connections for serviceability.

Horizontal Level-Two Packaging

Referring now to FIG. 17, the preferred embodiment of a horizontally oriented level-one package suitable for modular or level-two assembly is illustrated with a partial cut-out view of some interior details. The horizontal level-one package is preferred where overall height is a key consideration. In this embodiment, the level-one package P is constructed essentially as described above with reference to FIGS. 5 and 6 but may also include the integral heat sink element as shown in FIG. 8.

Package P is formed with a casing 12, optional epoxy layer 20 and aluminum foil layer 22 laminated above and below an integrated circuit die 14 (FIGS. 5–6). The cut-out (FIG. 18) shows typical interior details of such a package wherein leads 16 and 18 extend laterally from package P, and are bent downward at an angle less than ninety degrees to provide spring-loading which facilitates mounting as described below. Leads 16 and 18 are formed of copper approximately one and four-tenths to two and eight-tenths mils thick in a substantially rectangular cross-section and with adequate temper to provide a relatively flat, flexible connector. Leads 16 and 18 are bonded over die 14 with a two-mil semiconductor grade adhesive dielectric 130 using conventional automated tape bonding or low-profile ribbon or wire bonding techniques to a copper lead frame 131 to bond the leads to bonding pads 132 at-the perimeter of die 14. Leads 16, 18 are extended from package P and bent at their distal ends to provide flexibility for stress relief in mounting as described above. To facilitate stacking, each package P is formed having a nesting slot or detent 136 at each of four corners, such slots 136 being formed to receive a complimentary shaped nesting tab 138 formed at the lower surface at each of the four corners.

The individual level-one packages P are assembled in a horizontally oriented level-two package T in the manner illustrated in FIG. 18. Each package P is individually assembled and tested prior to assembly in horizontal stack package T. Package T is built upon a hard-anodized aluminum base 142 which alternatively can be formed of molded HYTON, or other suitable electrically insulating material. While FIG. 18 illustrates an assembly of four level-one packages for clarity, it should be noted that the typical package T would include eight or nine level-one packages. Furthermore, while some of the drawings illustrate a package P having only four leads 16, 18 per side for clarity, a typical package P would include many more (typically 28), depending upon the pin-out requirements of the particular integrated circuit being packaged.

Level-one packages P for assembly into multiple-unit level-two packages T are formed as described above. Each unit P includes a die 14, a case 12 a metallic foil lamination 22 and may include epoxy lamination layer 20 (FIGS. 5, 6). In those embodiments where each element P only includes an aluminum or copper foil lamination 22 (FIG. 6), the individual packages P are simply mechanically bound together by the structural members of package T (FIG. 18). Alternatively, each level-one package P can be adhered to the package P immediately above and below with a one-mil thick epoxy adhesive 148, and only upper and lower level-one packages P_{10} and P_{11} are provided with a metal foil lamination 146 over an adhesive layer 148 at the upper and lower surfaces of P_{10} and P_{11}, respectively. In this embodiment, each of leads 16, 18 (FIG. 17) is formed of copper to provide spring-like resiliency, and extended from package P to allow stress relief.

Referring now to FIG. 18, package T includes base 142, level-one packages P stacked above base 142, electrically and thermally conductive external rails 150 electrically and thermally coupled to leads 16 and 18, and a cap member 160. Cap member 160 and base member 142 must be electrically isolated from rails 150 and preferably should be formed of thermally conductive material. In addition to non-conducting plastics such as RYTON, cap 160 and base 142 can be formed of heat conductive materials such as plastic coated aluminum or preferably hardanodized aluminum without coating.

Cap 160 includes a plurality of slots 161 formed to be aligned with upper portions 162 of rails 150. Once the stack of packages P are assembled, cap 160 is adhered to the upper surface of package P_{10}, with upper portions 162 of rails 150 extending through slots 161 and being bent over to clamp rails 150 to cap 160.

Referring to FIG. 23, an alternative embodiment of a level-two package T is illustrated. This embodiment is adapted for mounting within an orifice formed in a printed circuit board, whereby the level-two package T is mounted to the printed circuit board with circuit board mounting portion 154(FIG. 19*c*) formed on the intermediate portion of rail 150.

Rails 150 include a lower portion 152 (FIG. 19*a,d*) which further includes base mounting tab 155 and a circuit board mounting portion 154 configured in either J-lead (FIG. 19*a*) or gull-wing configuration (FIGS. 19*b,c*). Additionally, rails 150 can include an integral heat sink flange 157 (FIG. 19*d*) for improved heat dissipation.

Assembly of level-two package T can be in one of two formats. In the first format, all of the required. level-one packages P are horizontally stacked above base. 142 and adhered or bound to one another first, and thereafter assembly continues with the provision of a plurality of vertically oriented lead rail elements 150. Rail elements 150 are formed of conductive resilient material such as 110 alloy copper having a cross-sectional thickness in the range of four to eight-mils. Each rail element (FIG. 19*a–d*) comprises alomer portion 152 and a lower J-lead, butt-lead or gull-wing configured SMT circuit board mounting portion 154.

Alternatively, in the preferred embodiment, assembly and testing are conducted level by level, with each level-one package P being assembled, tested, mounted

on the stack, with leads 16, 18 soldered to the corresponding rails 150, and re-tested before a subsequent level-one package P is added to the stack. This methodology insures that all level-one elements are functional before subsequent elements are added to the stack to avoid waste.

Where the level-one packages are to be mounted in the stack without adhesive bonding between level-one elements, the following procedure is utilized:

1. Assemble (including integrated circuit burn-in) and fully test a plurality of level-one packages, sorting level-one packages by speed or signal response time to ensure speed uniformity in level-two modules;
2. Preassemble the module header and rails;
3. Designate selected level-one packages for assembly into a particular module by level in the stack, cutting off unused leads for each respective level-one. package;
4. Place the lowest level-one package in position on the header, solder the leads 16,18 in place to the rails 150, using a laser or a hot bar to solder leads simultaneously;
5. Test the assembly for satisfactory electrical performance; remove and replace bad level-one package;
6. Repeat steps 4 and 5 for the remaining level-one packages for the module;
7. Mount the upper cap 160, and secure the connection between cap 160 and rails 150; and
8. Electrically test the entire assembled module.

Where adhesive bonding between level-one packages is to be used, the following procedure is utilized:

1. Assemble (including integrated circuit burn-in) and fully test a plurality of level-one packages, sorting level-one packages by speed or signal response time to ensure speed uniformity in level-two modules;
2. Preassemble the module header and rails;
3. Designate selected level-one packages for assembly into a particular module by level in the stack, cutting off unused leads for each respective level-one package;
4. Place the lowest level-one package in position on the header, solder the leads 16, 18 in place to the rails 150, using a laser or a hot bar to solder leads simultaneously;
5. Test the assembly for satisfactory electrical performance; remove and replace bad level-one package;
6. Place a B-stage epoxy lamination even the upper surface of the lowest level-one package previously mounted in the header;
7. Place a temporary teflon spacing lamination (2 mils thick) over the adhesive, B-stage epoxy lamination;
8. Mount the next level-one package over the teflon spacer and bond leads 16, 18 to rails 150;
9. Test the assembly for electrical performance;
10. Remove the teflon spacer if performance is satisfactory;
11. Heat laminate the adhesive bond between level-one packages to an intermediate bonding stage;
12. Repeat steps 6–10 until all level-one packages for the module are assembled;
13. Install a cap 160 over upper level-one package and secure to rails 150;
14. Complete the cure of the bonding adhesive between layers;
15. Test the entire module for electrical performance.

In either case, once the stack of level-one packages is completed and all leads 16, 18 have been solder connected to rails 150, a cap 160 formed of high temperature material, such as anodized aluminum, is mounted to the upper surface of the topmost level-one package P_{10} Cap 160 is formed having a plurality of slots 161 to receive the upper ends 162 (FIG. 19*a*) of rails 150.

After cap 160 is affixed, heat sinks may be attached to the package T in one of several alternative embodiments. In a first embodiment (FIG. 18*a*), heat sink elements 170 are mounted to the exterior surface of portions 152 of-rails 150 by means providing for electrical insulation but thermal conductance. One method is to bond heat sinks 170 to rails 150 using a two-mil thick high temperature epoxy adhesive. Alternatively, a two-mil thick beryllium oxide pad can be interposed between heat sinks 170 and rails 150 and adhered to sinks 17 and rails 150 with a suitable high temperature adhesive. Such heat sinks are preferably formed of anodized aluminum. Alternatively, heat is dissipated via the rails 150 without additional external heat sinks, or via integral heat sink flanges providing increased surface area for rails 150 such as the embodiment shown in FIG. 19*d*.

Where the stack is assembled without adhesive bonding (either horizontally or vertically) between the level-one elements and the elements are subsequently soldered to the rails simultaneously in one reflow process the following procedure is utilized:

1. Assemble (including integrated circuit burn-in) and fully test a plurality of level-one packages, sorting level-one packages by speed or signal response time to ensure speed uniformity in level-two modules;
2. Preassemble the module header and rails;
3. Designate selected level-one packages for assembly into a particular module by level in the stack, cutting off unused leads for each respective level-one package;
4. Place solder paste on all level-one leads
5. Place the header assembly into a temporary fixture and assemble all level-one packages into the rail/-header assembly;
6. Attach the top cap and a remove the assembly from the fixture;
7. Reflow solder all the level-one leads to the header rails in one reflow process;
8. Test entire stack;
9. If defective, remove the cap, desolder and remove the level-one package from the header assembly, replace the defective unit(s) and rework the assembly (stages 1 and 8).

With the foregoing assembly complete, heat is conducted from the level-one packages P via leads 16, 18 to rails 150 and thereafter dissipated in heat sinks 170. If a horizontal levelsone package with integral heat sink elements 30 is employed (FIG. 8), an additional set of rails 150 on a third side of package T are soldered to elements 30 in the same manner as described above, and an additional heat sink 170 can be attached.

An alternative embodiment of package T is disclosed in FIG. 20. In this embodiment, each of rails 150 are formed including an upper, horizontally oriented extension 180 which extends through cap 160 and traverses slightly less than half way across the width of cap 160 so as to be in surface contact with the upper surface of cap 160. An additional heat sink 182 is affixed to extensions 180 of rails 150 using a heat conductive adhesive. In this manner, heat from level-one packages P is conducted

through leads 16 and 18 to rails 150 and dissipated in heat sinks 170 and 182.

A major advantage of the invention is in the resulting efficiency and flexibility for thermal management of the module. At a fifty percent duty cycle a nine-high-module (four magabytes by one by nine) needs to dissipate up to 2.5 watts and a θJC of less than 20° C./Watt is desirable. The various embodiments of the level-one packages of the present invention provide an extremely efficient 2° C. to 5° C./watt θJC, and the modular package may be designed to provide a 15° C. to 20° C./watt θJC. This design thus permits the utilization of conventional air-cooling convection and conduction through the leads 16, 18 to rails 150 and heat sinks or a combination of these methods, as distinguished from more complicated and expensive cooling techniques.

The level-two modular construction is especially useful to provide a multiple element memory array. An example of this array-would be a four megabit by one by nine array to form a four megabyte plus panty DRAM module. This module would be a single package replacement for a four megabyte plus panty SIMM card. Each individual element P of the module will have twenty-eight leads where only eighteen of the twenty-eight leads require connection to the bus rails 150. The leads not requiring a connection for each element P are severed from the device flush to the package P. The tape lead frame, which provides the internal, level-one die to lead connections, provides for a common data-in, data-out bus. This bus will connect to eight pins on the package. Only one of the eight pins will be used for each level of the total module, with the other seven leads severed. This provides a common lead frame which could be used by the eight memory layers providing the data bits for the memory module. The parity bit memory layer requires a separate lead frame. The data-in and data-out pin are separated and the CAS input signal must be separated from the common CAS bus of the eight memory bits. A schematic illustrating an example of the manner of electrical interconnection is provided in FIG. 21.

Other options are available for various configurations static rams could be packaged-in a four high module to provide either a four, sixteen, or thirty-two bit wide array. DRAMS could also be packaged in four or five high stacks to accommodate those areas where product height is a concern. The five-high stack could be settled as a standard height, with a common header for the stack. For the four-high stack a "dummy" spacer layer will be added to maintain the product standard size.

Total pin count of the modules determines the lead spacing, stack height, and bus widths. Those modules with lead counts below thirty pins could be assembled with standard 50-mil lead spacing. Larger lead count devices will be set on 25-mil centers. The stack height and bus widths (data and address buses) are indirectly related. Higher stacks naturally make the data buses wider and provide for larger pin counts. FIG. 21 provides an exemplary four megabyte plus panty DRAM configuration. The following table represents examples of configurations, pin counts, data widths and product types:

Product	Chip	Total Memory	Configuration	Pin Count	Output Word Length
DRAM	1 Meg	9 M Bit	1M × 1 × 9	26	8 B, +1 Par.
DRAM	1 Meg	9 M Bit	256K × 4 × 0	52	32 B, +4 Par.
DRAM	4 Meg	36 M Bit	1M × 4 × 9	53	32 B, +4 Par.
DRAM	4 Meg	36 M Bit	4M × 1 × 9	28	8 B, +1 Par.
SRAM	256K	2 M Bit	256K × 1 × 8	30	8 B
SRAM	256K	1 M Bit	256K × 1 × 4	26	4 B
SRAM	256K	2 M Bit	64K × 4 × 8	52	32 B
SRAM	256K	1 M Bit	64K × 4 × 8	36	16 B
SRAM	1 Meg	8 M Bit	256K × 4 × 8	55	32 B
SRAM	1 Meg	4 M Bit	256K × 4 × 4	39	16 B

For those (× 1) memory chips with separate Din, Dout lines, the Din and Dout lines are tied together. The parity Din and Dout are not tied together.

The foregoing description provides details of preferred embodiments of an ultra-thin level-one integrated circuit package and a method of assembling level-one packages into a high density level-two package. The laminated structure of the level-one packages provides moisture protection and structural resistance to flexing to enable an ultra-thin package to be constructed without loss of circuit integrity. The level-two package provides high density, and thermal and environmental control in an easily manufactured package.

The foregoing disclosure and description of the invention are illustrative and explanatory of the preferred embodiments, and changes in the size, shape, materials and individual components, circuit elements, connection and construction may be made without departing from the spirit of the invention.

What is claimed is:

1. A modular integrated circuit package comprising:

a plurality of individual integrated circuit packages, each comprising:

an integrated circuit element, said integrated circuit element comprising an integrated electrical circuit and having a plurality of electrical interconnect leads extending therefrom;

a transfer-molded plastic casing surrounding said integrated circuit element, said casing having an upper surface, a lower surface and a perimeter wall;

a first metal foil lamination applied to said upper surface of said casing;

a second metal foil lamination applied to said lower surface of said casing;

a planar heat sink element in surface contact with a surface of said integrated circuit element, said heat sink further being formed and mounted so as to extend through a portion of said casing wall;

wherein said leads from said integrated circuit element extend through a portion of said perimeter wall of said casing; and wherein said plurality of integrated circuit packages are bound together in a vertically oriented assembly, having their said leads extending below the assembly and their heat sink elements extending above the assembly; and a

housing surrounding said assembly, said housing having a first side member and a second side member and a top, said side members and said

2. The package of claim 1, wherein said side members are substantially rectangular and further comprise a mounting means for mounting said package to an underlying circuit board.

3. The package of claim 2, wherein said mounting means comprises a plurality of mounting tangs formed in the lower edge of said side members and adapted to be received in a portion of an underlying circuit board.

4. The package of claim 1, wherein said housing top comprises a thermally conductive heat sink element adapted to be in thermal contact with said heat sink elements of said plurality of individual integrated circuit packages.

5. The package of claim 1, further comprising a circuit board mounting header, said header comprising a rectangular frame adapted for mounting with the lower extremities of said housing.

6. The package of claim 5, wherein said header further comprises a plurality of electrically conductive rails extending from one side of said frame to an opposite, parallel side, said rails being arranged in a parallel spacing arrangement coinciding with the spacing and arrangement of said electrical interconnect leads extending from said assembly and adapted for electrical connection to said leads.

7. The package of claim 6, wherein said rails further comprise a circuit board interconnection portion extending from the perimeter of said header frame and adapted for electrical interconnection to the underlying circuit board.

8. A modular integrated circuit package comprising:

a plurality of individual level-one integrated circuit packages, each comprising:

an integrated circuit element, said circuit element comprising an integrated electrical circuit having a plurality of electrical interconnect leads extending therefrom;

a transfer-molded plastic casing surrounding said integrated circuit element, said casing having an upper surface, a lower surface and a perimeter wall; and

wherein said integrated circuit leads extend from said integrated circuit element through a portion of said perimeter wall of said casing;

said plurality of level-one packages being assembled in a stacked configuration so that upper and lower surfaces of adjacent level-one packages are parallel to one another to form an assembly with a plurality of intermediate level-one packages flanked by two exterior level-one packages;

a high-temperature moisture-resistant adhesive bond layer formed between intermediate level-one packages;

a metallic foil lamination applied to the exterior surface of each of said exterior level-one packages.

9. The package of claim 8, wherein each of said level-one packages further comprises an integral planar heat sink element, said planar heat sink element in surface contact with one side of said integrated circuit element and extending from said integrated circuit element through a portion of said casing wall.

10. The package of claim 9, further comprising an assembly housing for housing said assembly of level-one packages, said housing including a top member and two side members; said top member being adjacent said heat sink elements of said level-one packages, and said side members being adjacent said exterior surface of said exterior level-one packages.

11. The package of claim 10, wherein said housing top member comprises a heat sink member having a substantially planar lower surface mounted in heat exchange relationship with said plurality of heat sink elements of said level-one packages.

12. The package of claim 8, wherein said level-one packages are horizontally oriented forming a vertical stack wherein said exterior level-one packages are at the upper and lower extremes of the stack.

13. A modular integrated circuit package comprising:

a plurality of level-one integrated circuit packages, each comprising:

an integrated circuit element, said integrated circuit element comprising an integrated circuit having a plurality of electrical interconnect leads extending therefrom;

an external electrically insulating casing surrounding said integrated circuit element, said casing having an upper surface, a lower surface and

a perimeter wall; and wherein leads extend from said integrated circuit element through a portion of said perimeter wall of said casing;

said level-one packages being horizontally oriented in a vertically aligned stacked configuration so that said leads from said level-one packages are aligned in an array of vertical columns;

a plurality of vertically oriented, thermally and electrically conductive rails mounted adjacent to said vertical columns of said leads; said rails being electrically and thermally coupled to said columns of leads.

14. The package of claim 13, wherein said rails each comprise a thermally and electrically conductive strip, each having an upper portion, an intermediate portion and a lower portion; and wherein said intermediate portion is adapted for electrical and thermal coupling to said leads.

15. The package of claim 14, wherein said rails include a circuit board interconnected portion adapted for mounting to an electrical circuit board.

16. The package of claim 14, further comprising:

a substantially planar, horizontally oriented top member, said top member overlaying said upper surface of the uppermost level-one package, and wherein said top member includes means for coupling to said upper portion of said rails.

17. The package of claim 16, wherein said top member is formed of thermally conductive material.

18. The package of claim 16, wherein said top member is formed of metal coated with electrically insulated material.

19. The package of claim 16, wherein said top member is formed of anodized aluminum.

20. The package of claim 16, wherein said rail coupling means comprises a plurality of slots formed to be aligned with said upper portion of said rails, said slots being adapted to receive said upper portion of said rails.

21. The package of claim 14, further comprising a substantially planar, electrically insulated base member underlying said lower surface of the bottom most level-one package.

22. The package of claim 21, wherein said base member is formed of anodized aluminum.

23. The package of claim 21, wherein said base member further comprises means for mounting said rails.

24. The package of claim 23, wherein each of said lower portions of said rails comprises a base mounting portion and a circuit board interconnection portion, and said rail mounting means comprises a plurality of slots formed in said base member so as to be aligned with said base mounting portion of said rails.

25. The package of claim 15, wherein said circuit board interconnection portion of said rails is formed in a J-lead configuration.

26. The package of claim 15, wherein said circuit board interconnection portion of said rails is formed in a gull-wing configuration.

27. The package of claim 15, wherein said circuit board interconnection portion is formed in said intermediate portion of said rails.

28. The package of claim 14, wherein said rails include an integral heat-sink portion.

29. The package of claim 14, further comprising a heat sink element mounted to said intermediate portion of said rails.

30. The package of claim 16, wherein said upper portions of said rails extend to overlay a portion of said top member, and wherein said module further comprises a heat sink element mounted over said top member and thermally coupled to said upper portion of said rails.

31. The package of claim 13, wherein said stack of level-one packages comprises a plurality of intermediate level-one packages, and an upper and lower level-one package, said module further comprising a moisture resistant, high-temperature adhesive bond layer formed between intermediate level-one packages.

32. The package of claim 31, further comprising:

a first metallic foil lamination applied to the upper surface of said upper level-one package; and a second metallic foil lamination applied to the lower surface of said lower level-one package. top being formed of thermally conductive, rigid material.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,420,751

DATED : May 30, 1995

INVENTOR(S) : Carmen D. Burns

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings: Figure 22:

Control input "PQDQ[0-8]" is changed to -- DQ[0-7] --.

The connection between the Q input to the RAM which connects to the PCAS input control line and control input DQ[0-7] has been eliminated.

Newly added control input PQ has been connected to the Q input of the RAM which connects to the PCAS input control line.

The bit number indicator on the DQ[0-7] input line has been changed from "9" to -- 8 --.

Column 1, line 10, delete "incorporation" and insert therefor -- incorporating -- .
Column 1, line 42, delete "and," and insert therefor -- and -- .
Column 2, line 7, delete "small" and insert therefor -- smaller -- .
Column 4, line 1, after "embodiment" add -- of -- .
Column 6, line 29, delete "extends" and insert therefor -- extend -- .
Column 6, line 28, delete "purposes.." and insert therefor -- purposes. -- .
Column 6, line 29, delete "package." and insert therefor -- package --.
Column 6, line 59, delete "using-a one half." and insert therefor -- using a one half -- .
Column 6, line 62, delete "In a this" and insert therefor -- In this -- .
Column 8, line 22, delete "from" and insert therefor -- form -- .
Column 9, line 19, delete "leads. 38" and insert therefor -- leads 38 -- .

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,420,751
DATED : May 30, 1995
INVENTOR(S) : Carmen D. Burns

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, line 47, delete (FIG. 19a,d) and insert therefor -- (FIG. 19a-d) -- .
Column 10, line 63, delete "alomer" and insert therefor -- a lower -- .
Column 13, line 56, after "configurations" insert -- . -- .
Column 13, line 57, delete "static" and insert therefor -- Static --.
Column 14, line 12, delete "256K x 4 x 0" and insert therefor -- 256K x 4 x 9 -- .
Column 14, line 23, delete "Din. Dout" and insert therefor -- Din, Dout -- .

Column 15, line 3, after "said" insert -- top being formed of thermally conductive, rigid material. -- .
Column 18, line 20-21, delete "top being formed of thermally conductive, rigid material."

Signed and Sealed this

Nineteenth Day of December, 1995

Attest:

BRUCE LEHMAN

Attesting Officer *Commissioner of Patents and Trademarks*

Fig. 22

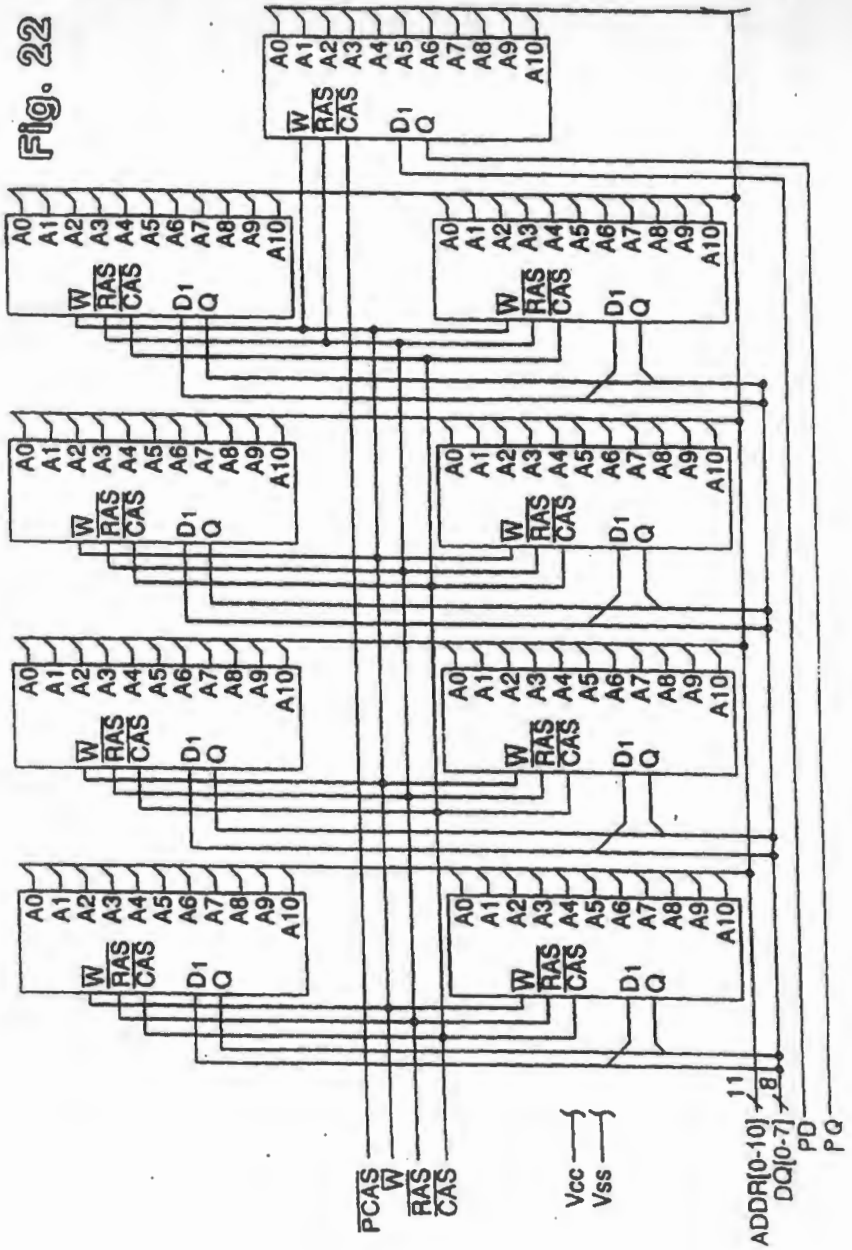
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
W
RAS
CAS
D1
Q
PCAS
W
RAS
CAS
Vcc
Vss
11
8
ADDR[0-10]
DQ[0-7]
PD
PQ

EXHIBIT B

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J. Scott Denko
Direct Dial: (512)-906-2076
Email: denko@dcllegal.com

April 22, 2011

Shawn Lindquist
Chief Legal Officer
Fusion-IO
2855 E. Cottonwood Parkway, Suite 100
Salt Lake City, UT 84121

Via Federal Express

RE: Patent Infringement

Dear Mr. Lindquist:

This law firm represents Entorian Technologies Inc. ("Entorian") of Austin, Texas. It has come to our attention that Fusion io makes and sells solid state drives that infringe U.S. Patents owned by Entorian. For example, your 640GB IODRIVE product FS1-003-641-CS-0001[1] appears to include 24 memory stacks. These stacks are made from two packaged TSOP devices whose respective leads are connected as claimed, for example, in Entorian's U.S. Pat. No. 5,420,751.

We hereby notify you that your 640GB IODRIVE infringes U.S. Pat. No. 5,420,751 under Title 35 § 271 of the U.S. Code. Subject to further investigation, we believe that your 640GB IODRIVE likely infringes U.S. Pat. No. 6,025,642. Copies of these patents are enclosed. We are continuing our investigation and expect to find that a variety of your solid state drives exhibit the same features that compel us to conclude that your 640GB IODRIVE is an infringement.

Your infringement of Entorian patents must stop immediately. Entorian stands ready to discuss this matter including licensing its patent portfolio, but if we do not hear from you by May 20, 2011, we will pursue all available legal remedies.

Sincerely,

J. Scott Denko

[1] Also known as part #A4144511. It includes a PC board marked with "Fusion-io EP001193-000_6."

EXHIBIT C

May 18, 2011

J. Scott Denko
Denko Coburn & Lauff LLP
816 Congress Avenue, Suite 1205
Austin, Texas 78701

Re: April 22, 2011 Letter from Entorian Technologies Inc.

Dear Mr. Denko:

Thank you for your letter of April 22, 2011 regarding United States Patent Nos. 5,420,751 and 6,025,642. We have reviewed the letter and the attached copies of the patents. Unfortunately, the information in your letter was insufficient for us to understand the nature of Entorian Technologies Inc. ("*Entorian*") infringement allegations against our products. *For example*, your letter does not provide an identification of the specific patent claims that you believe are infringed by the 640GB IO Drive product. Also, your letter does not include any claim charts or engineering analysis showing how our products allegedly use the unidentified claims of the Entorian patents.

Fusion-io is a private company and does not have a large legal staff. As such, it would be very helpful if you could provide more information so that we could better understand why you allege that our products infringe Entorian patents. Fusion-io has always believed in respecting the intellectual property rights of companies.

Sincerely,

Shawn J. Lindquist

Shawn J. Lindquist
Chief Legal Officer
Fusion-io, Inc.

EXHIBIT D

FUSION-IO

May 19, 2011

Polystack, Inc.
2186 Paragon Drive
San Jose, CA 95131
Attn: Terry Chung, General Manager

Re: Entorian Technologies, Inc. ("Entorian") Infringement Allegations against Products Supplied by Polystak, Inc. ("Polystak")

Ladies and Gentlemen:

Fusion-io has received a letter from Entorian, dated April 22, 2011, that alleges that memory stacks that Fusion-io purchases from Polystack, Inc. ("Polystack") infringe United States Patent Nos. 5,420,751 ("'751 Patent") and 6,025,642 ("'642 Patent"). A copy of the April 22, 2011 Entorian letter and the two patents are enclosed with this letter. The April 22, 2011 letter does not identify the specific patent claims in the '751 and '642 Patents that are allegedly infringed by the Polystack memory stacks supplied to Fusion-io. To date, Entorian has not initiated any legal action against Fusion-io with respect to the patents identified in the April 22, 2011 letter.

Pursuant to the section 15 (Indemnification) of "FUSION-IO, INC. PURCHASE ORDER TERMS AND CONDITIONS," Fusion-io is providing Polystack with notice that it may seek indemnification from Polystack for any patent action brought by Entorian with respect to the memory stacks that the company supplies to Fusion-io. For reference, a copy of Fusion-io's standard purchase order terms and conditions are enclosed with this letter.

Fusion-io greatly values its strong partnership with Polystack and looks forward to working with the company in the future and to resolve the issues set forth in the letter.

Sincerely,

Shawn J. Lindquist

Shawn J. Lindquist
Chief Legal Officer
Fusion-io, Inc.

cc: David A. Flynn, CEO, Fusion-io, Inc.
Dennis P. Wolf, CFO, Fusion-io, Inc.
Larry W. Sonsini, Esq., Wilson Sonsini Goodrich & Rosati, P.C.
James C. Yoon, Esq., Wilson Sonsini Goodrich & Rosati, P.C.

EXHIBIT E

FUSION-IO, INC.
PURCHASE ORDER TERMS AND CONDITIONS

PLEASE READ THE REVERSE SIDE CAREFULLY. BY SHIPPING THE GOODS SPECIFIED IN THE PURCHASE ORDER OR BY PERFORMING THE WORK DESCRIBED IN THE PURCHASE ORDER, SELLER AGREES TO THE SPECIFICATIONS, TERMS AND CONDITIONS OF PURCHASE SET FORTH IN THESE TERMS AND CONDITIONS AND ON ANY SHEETS OF ADDITIONAL SPECIFICATIONS, TERMS, AND CONDITIONS ATTACHED HERETO. FUSION-IO HEREBY OBJECTS TO ANY DIFFERENT OR ADDITIONAL TERMS IN SELLER'S ACCEPTANCE OF THIS OFFER.

1. PRICES AND TAXES
The acceptance of this purchase order constitutes a warranty that the prices to be charged for articles or services ordered ("Products") do not exceed the lowest price charged to any other customer for similar quantities and delivery requirements. Unless otherwise specified, the prices set forth in this purchase order include all packaging, transportation and shipping charges and all applicable federal, state and local taxes. All personal property taxes assessable upon the goods prior to receipt by Fusion-io will be borne by Seller.

2. INVOICES
Seller will submit invoices in duplicate showing the following information: purchase order number, item number, description of item, size of item, quantity of item, unit prices, each applicable tax, extended totals and any other information specified elsewhere herein. A bill of lading or express receipt must accompany each invoice. Payment of invoice will not constitute acceptance of goods and will be subject to adjustment for errors, shortages, defects in the goods or other failure of Seller to meet the requirements of this purchase order. Unless otherwise agreed by the parties in writing, if goods are shipped to Fusion-io in installments, Fusion-io will not be required to pay Seller for the goods until after the last installment of goods has been received by Fusion-io. Fusion-io may at any time set off any amount owed by Fusion-io to Seller against any amount owed by Seller or any of its affiliated companies to Fusion-io.

3. DISCOUNTS
Time in connection with any discount offered by Seller will be computed from the latest of (a) the scheduled delivery date, (b) the date of actual delivery or (c) the date an acceptable invoice is received. For the purpose of earning the discount, payment will be deemed to have been made on the date of mailing of Fusion-io's check.

4. OVERSHIPMENTS
Fusion-io will pay only for maximum quantities ordered. Overshipments will be held by Fusion-io at Seller's risk and expense for a reasonable time awaiting shipping instructions. Return shipping charges for excess quantities will be at Seller's expense.

5. PACKING AND SHIPMENT
Unless otherwise specified, when the price of this purchase order is based on the weight of the ordered goods, such price is to cover only the net weight of material ordered, and no charges will be allowed for packing, handling, transportation, storage or other packing requirements. Unless otherwise provided for in the purchase order, Fusion-io will not be responsible for any charges relating to packaging of the goods. Unless otherwise specified, Seller will package and pack all goods in a manner that is (a) in accordance with good commercial practice, (b) acceptable to common carriers for shipment at the lowest rate for the particular goods, (c) in accordance with I.C.C. regulations, and (d) adequate to insure safe arrival of the goods at the named destination. Seller will mark all containers with necessary lifting, handling, and shipping information and with purchase order numbers, date of shipment and the names of the consignee and consignor. An itemized packing list must accompany each shipment. No partial or complete delivery will be made prior to the due date or dates shown unless Fusion-io has given prior written consent.

6. F.O.B. POINT
Unless otherwise specifically provided on the face of this purchase order, the products ordered hereunder will be delivered F.O.B. named port of destination.

7. WARRANTY
(a) Seller warrants that all goods delivered will (i) be free from defects in workmanship, material, and manufacture; (ii) comply with the requirements of this purchase order, including any drawings or specifications incorporated herein or samples furnished by Seller; (iii) where design is Seller's responsibility, be free from defects in design and (iv) be in compliance with all applicable laws and regulations. Seller further warrants that all goods purchased hereunder will be of merchantable quality and will be fit for the purposes intended by Fusion-io to the extent disclosed to Fusion-io. The foregoing warranties constitute conditions to this purchase order. They are in addition to all other warranties, whether express or implied, and will survive any delivery, inspection, acceptance or payment by Fusion-io. All warranties run to the benefit of Fusion-io and its resellers and customers.
(b) Fusion-io's approval of Seller's materials or design will not relieve Seller of any warranties.
(c) If any goods delivered do not meet the warranties specified herein or otherwise applicable, Fusion-io may, at its option, (i) require Seller to correct any defective or nonconforming goods by repair or replacement at no cost to Fusion-io; (ii) return such defective or nonconforming goods to Seller at Seller's expense and recover from Seller the order price thereof or (iii) correct the defective or nonconforming goods itself and charge Seller with the cost of such correction.

8. INSPECTION AND ACCEPTANCE
Notwithstanding any prior inspection or payments, all goods will be subject to final inspection and acceptance at Fusion-io's plant within a reasonable time after delivery. Fusion-io may run tests to determine whether the goods conform to the requirements of this purchase order. In case any item is defective in material or workmanship, or otherwise not in conformity with the requirements of this purchase order, Fusion-io will have the right to reject it, to require its correction or to accept it with an adjustment in price. Any item that has been rejected or required to be corrected must be replaced or corrected by and at the expense of Seller promptly after notice. If, after being requested by Fusion-io, Seller fails to promptly replace or correct any defective item, then Fusion-io may (a) by contract or otherwise, replace or correct such item and charge to Seller the cost occasioned thereby, (b) without further notice, cancel this purchase order for default in accordance with Section 10 below or (c) require an appropriate reduction in price.

9. CHANGE ORDERS
(a) The Fusion-io may at any time, by a written order, suspend performance hereunder, increase or decrease the ordered quantities, change the due date or make changes in any one or more of the following:
(i) applicable drawings, designs or specifications;
(ii) method of shipment or packing; or
(iii) place of delivery.
(b) If the change causes an increase in the cost or the time required by Seller for performance of this purchase order and Seller so notifies Fusion-io, then an equitable adjustment will be made in the order price or delivery schedule or both, and the purchase order will be modified accordingly in writing. No claim by Seller for such an adjustment will be valid unless asserted within 20 days from the date of receipt by Seller of the notification of change; provided, however, that such period may be extended upon the written approval of Fusion-io.
(c) Nothing in this Section 9 is intended to excuse Seller from proceeding with this purchase order as changed or amended.

10. CANCELLATION FOR DEFAULT
(a) It is understood and agreed that time is of the essence for this purchase order because the goods or services ordered herein are needed for products of Fusion-io that have a very short, carefully timed market life; failure of Seller to deliver on the due date could cause Fusion-io's products to be unmarketable. Fusion-io may, by written notice, cancel this purchase order in whole or in part if, in Fusion-io's good-faith opinion, Seller has failed to (i) make delivery of the items or to perform the services within the time specified herein, or any extension thereof by written change order or

amendment; (ii) replace or correct defective items in accordance with the provisions of Sections 7 or 8 above; (iii) perform any of the other provisions of this purchase order or (iv) has so failed to make progress under this purchase order as to endanger performance in accordance with its terms.

(b) If this purchase order is canceled for Seller's default, Fusion-io may procure, upon such terms and in such manner as Fusion-io may deem appropriate, goods or services similar or substantially similar to those canceled. Seller will then be liable to Fusion-io for any excess costs occasioned thereby.

(c) If all or a portion of this purchase order is canceled for Seller's default, Fusion-io may require Seller to transfer title and to deliver to Fusion-io, in the manner and to the extent directed by Fusion-io, (i) all completed items not yet delivered and (ii) any partially completed items and materials that Seller has produced or acquired for the performance of the terminated portion. Seller will, upon direction of Fusion-io, protect and preserve the property listed in this paragraph that is in the possession of Seller. Payment for completed items delivered to and accepted by Fusion-io under this paragraph will be in an amount (not to exceed the contract price) agreed upon by Seller and Fusion-io; however, Seller's obligation to carry out Fusion-io's direction as to delivery, protection and preservation of the property will not be contingent upon prior agreement as to such amount.

(d) Nothing in this Section 10 is intended to excuse Seller from proceeding with any uncancelled portion of this purchase order.

11. TERMINATION FOR CONVENIENCE

(a) At any time for convenience, Fusion-io may terminate this purchase order, in whole or in part, by written notice.

(b) Upon such termination, Seller will, to the extent and at the times specified by Fusion-io, stop all work under this purchase order; place no further orders for materials to complete the work; assign to Fusion-io all Seller's interests under terminated subcontracts and orders; settle all claims thereunder after obtaining Fusion-io's approval; protect all property in which Fusion-io has or may acquire an interest; and transfer title and make delivery to Fusion-io of all articles, materials, work in process and other things held or acquired by Seller in connection with the terminated portion of this purchase order. Seller will proceed promptly to comply with Fusion-io's instructions respecting each of the foregoing without awaiting settlement or payment of its termination claim.

(c) Within six months after such termination, Seller may submit to Fusion-io its written claim for termination charges, in the form and with the certifications prescribed by Fusion-io. Failure to submit the claim within six months will constitute a waiver of all claims and a release of all Fusion-io's liability arising out of the termination.

(d) The parties may agree upon the amount to be paid Seller for such termination. If they fail to agree, Fusion-io will pay Seller the following amounts:

(i) The contract price for all items completed or services rendered in accordance with this purchase order for which payment has not been made.

(ii) The actual costs incurred by Seller which are properly allocable under recognized commercial accounting practices to the terminated portion of this purchase order, plus a fair and reasonable profit on such costs. If it appears that Seller would have sustained a loss on the order, no profit will be allowed and an adjustment will be made reducing the amount of the settlement to reflect the indicated rate of loss.

(iii) The reasonable costs incurred by Seller in making settlement hereunder and in protecting property in which Fusion-io has or may acquire an interest.

(e) Payments made under Sections 11(d)(i) and (ii) above may not exceed the aggregate price specified in this purchase order less payments otherwise made or to be made. Any amounts payable for property lost, damaged, stolen or destroyed prior to delivery to Fusion-io will be excluded from amounts otherwise payable to Seller under this Section 11.

12. RISK OF LOSS OR DAMAGE

Notwithstanding any prior inspections and irrespective of the F.O.B. point named herein, Seller will bear all risk of loss, damage or destruction to the ordered goods until final acceptance of the goods by Fusion-io at destination. Seller will bear the same risk with respect to any goods rejected by Fusion-io. Fusion-io, however, will be responsible for any loss occasioned by the gross negligence of its employees acting within the scope of their employment.

13. WAIVER

The failure of Fusion-io to enforce at any time any of the provisions of this purchase order, to exercise any election or option provided herein or to require at any time the performance by Seller of any of the provisions herein will not in any way be construed to be a waiver of such provisions.

14. REMEDIES

The remedies stated herein are in addition to all other remedies at law or in equity.

15. INDEMNIFICATION

(a) Seller agrees to indemnify Fusion-io, its agents, customers, successors, and assigns against any loss, damage and liability (including costs and expenses) for actual or alleged infringement of any patent, copyright, trademark or other third party right arising out of the use or sale of the goods by Fusion-io, its agents or customers; provided, however, that Fusion-io must notify Seller of any suit, claim or demand involving such infringement and permit Seller to defend against or settle the same. If any injunction is issued as the result of any such infringement, Seller agrees, at Fusion-io's option, to (i) refund to Fusion-io the amounts paid to Seller for the goods covered by the injunction or (ii) promptly furnish Fusion-io with acceptable and noninfringing goods.

(b) Seller agrees to indemnify Fusion-io against any and all liability and expense resulting from any alleged defect in the goods, whether latent or patent, including allegedly improper construction and design or from the failure of the goods to comply with specifications.

(c) Seller warrants that there are no liabilities for royalties, mechanics liens or other encumbrances on the goods supplied and agrees to indemnify Fusion-io against any such liabilities.

(d) The above indemnifications are in addition to all other rights of indemnification of Fusion-io against Seller.

16. NON-DISCLOSURE OF CONFIDENTIAL MATTER

Seller will not quote for sale to others, without Fusion-io's written authorization, any goods purchased under Fusion-io's specifications or drawings. All designs, tools, patterns, specifications, drawings, samples and other data, as well as materials and equipment, furnished by Fusion-io will be treated by Seller as confidential information, will remain Fusion-io's property and will be returned to Fusion-io on request. Unless otherwise agreed in writing, all special dies, tools, jigs, fixtures, equipment and patterns furnished by Fusion-io to Seller or specifically paid for by Fusion-io, will be the property of Fusion-io (and Seller hereby assigns to Fusion-io any of its right, title, or interest therein) and will be returned to Fusion-io in good condition upon Fusion-io's request.

17. ASSIGNMENTS

No right or obligation under this purchase order (including the right to receive monies due) may be assigned by Seller without the prior written consent of Fusion-io and any purported assignment without such consent will be void. Fusion-io may assign this purchase order at any time if such assignment is considered necessary by Fusion-io in connection with a sale of Fusion-io's assets or a transfer of its obligations.

18. NOTICE OF DELAYS

Whenever any event delays or threatens to delay the timely performance of this purchase order, Seller will immediately notify Fusion-io of such event and furnish all relevant details. Receipt by Fusion-io of such notice will not constitute a waiver of the due dates hereunder.

19. GOVERNMENT CONTRACTS

If this purchase order is issued for any purpose that is either directly or indirectly connected with the performance of a prime contract with the government or a subcontract thereunder, the terms that the Armed Services Procurement Regulation or other appropriate regulations require to be inserted in contracts or subcontracts will be deemed to apply to this purchase order.

20. APPLICABLE LAW

This purchase order will be governed by the laws of the State of Utah without reference to conflict of law principles. The federal and state courts located in Salt Lake County, Utah will have exclusive jurisdiction to adjudicate any dispute arising out of these terms and conditions of sale.

EXHIBIT F

DENKO COBURN & LAUFF LLP

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May 31, 2011

Shawn Lindquist
Chief Legal Officer
Fusion-IO
2855 E. Cottonwood Parkway, Suite 100
Salt Lake City, UT 84121

RE: Patent Infringement

Dear Mr. Lindquist:

Thank you for your letter of May 18, 2011 regarding US Pat. Nos. 5,420,751 (the '751 patent) and 6,025,642 (the '642 patent), collectively referred to as the "Patents". In this letter, we provide more detail concerning infringement of these Patents by the Fusion io 640GB IO Drive (the "Product").

We draw your attention to claim 13 of the '751 patent. Below we reproduce claim 13 and identify each limitation with a numerical marker (e.g., #X) for the convenience of the following discussion.

> 13. A modular integrated circuit package comprising:
>
> (#1) a plurality of level-one integrated circuit packages, each comprising:
>
> (#2) an integrated circuit element, said integrated circuit element comprising an integrated circuit having a plurality of electrical interconnect leads extending therefrom;
>
> (#3) an external electrically insulating casing surrounding said integrated circuit element, said casing having an upper surface, a lower surface and
>
> (#4) a perimeter wall; and wherein leads extend from said integrated circuit element through a portion of said perimeter wall of said casing;
>
> (#5) said level-one packages being horizontally oriented in a vertically aligned stacked configuration so that said leads from said level-one packages are aligned in an array of vertical columns;
>
> (#6) a plurality of vertically oriented, thermally and electrically conductive rails mounted adjacent to said vertical columns of said leads; said rails being electrically and thermally coupled to said columns of leads.

By its terms, claim 13 is directed to a module comprised from two (or more) (i.e., "a plurality") of leaded ICs (see limitation #1 of claim 13). Each of the leaded ICs has certain attributes as recited in limitations #2, #3, and #4 of claim 13. The modules found in the Product include two leaded ICs thus meeting limitation #1 of claim 13. Each of those constituent ICs meets the limitations of clauses #2, #3, and #4.

According to limitation #5 of claim 13, the constituent ICs are oriented horizontally in a vertically aligned configuration so that the leads are aligned in an array of vertical columns. In our examination of your Product, we find that the leads of the constituent ICs are aligned in an array of vertical columns. Thus, limitation #5 is met by the Product.

Limitation #6 of claim 13 recites, "a plurality of vertically oriented, thermally and electrically conductive rails mounted adjacent to said vertical columns of said leads; said rails being electrically and thermally coupled to said columns of leads." In your Product, a board bearing the rails is inserted between the leads of the constituent ICs and those rails are mounted adjacent to the vertical columns of leads. Keep in mind extra elements (i.e., the board that carries the rails) do not, as the case law says, "obviate" infringement. Consequently, limitation #6 is met and, therefore, all the limitations of the claim are found in the Product and the claim is infringed.

As an examination of the '642 patent will reveal in light of the above explanation, other claims are likely infringed. This exposition is merely an example of how one claim of the '751 patent is infringed by your Product. We expect that other products that you make, use, sell, import or offer for sale will be found to meet the limitations of at least claim 13. Consequently, we have to again urge you to contact us to arrange a license to this technology. If no progress on licensing is made by July 15, you will force us to assert a more aggressive range of legal remedies against Fusion IO.

Sincerely,

J. Scott Denko