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September 15, 2011

VIA HAND DELIVERY

PUBLIC VERSION

James R. Holbein
Secretary
U.S. International Trade Commission
500 E Street, S.W.
Washington, D.C. 20436

Re: In the Matter of Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software, Inv. No. 337-TA-724 -- Request for Confidential Treatment of Motion to Intervene and Terminate and Related Exhibits

Dear Secretary Holbein:

This firm represents Advanced Micro Devices, Inc. ("AMD"), and ATI Technologies ULC and ATI International SRL (collectively "ATI"), which are concurrently filing a motion to intervene and terminate the investigation pursuant to Commission Rules 210.19 and 210.21. In accordance with Commission Rules 201.6(b) and 210.5(e)(2), AMD and ATI request that confidential treatment be accorded the business information contained in the motion, memorandum of points and authorities, and accompanying exhibits. Pursuant to paragraphs 2 and 15 of the Protective Order (Order no. 1) issued in this investigation, AMD and ATI are suppliers of confidential business information and such information shall be treated in accordance with the terms of the Protective Order. AMD and ATI's motion and exhibits are clearly and prominently marked on their face with a notice of confidential business information in accordance with paragraph 2(a) of the Protective Order. AMD and ATI's confidential business information is in brackets, and a public version of AMD and ATI's motion is also being submitted pursuant to Commission Rule 201.6 and 201.8(d).

The information for which AMD and ATI seek confidential treatment is proprietary commercial information not otherwise publicly available. Specifically, the motion, memorandum of points and authorities, and accompanying exhibits contain proprietary commercial information concerning AMD and ATI's ownership of the asserted patents.

The information described above qualifies as confidential business information pursuant to Commission Rule 201.6(a) because:

1. it is not publicly available;

2. unauthorized disclosure of such information could cause substantial harm to the competitive position of AMD and ATI; and

3. the disclosure of which could impair the Commission's ability to obtain information necessary to perform its statutory function.

Please do not hesitate to contact me should you have any questions pertaining to this request.

Very truly yours,

Jeffrey D. Mills
Jeffrey M. Telep
Counsel for Advanced Micro Devices, Inc., ATI Technologies ULC and ATI International SRL

Enclosures

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of
CERTAIN DIGITAL IMAGING DEVICES AND RELATED SOFTWARE

Investigation No. 337-TA-724

ADVANCED MICRO DEVICES, INC., ATI TECHNOLOGIES ULC'S AND ATI INTERNATIONAL SRL'S MOTION TO INTERVENE FOR THE LIMITED PURPOSE OF RAISING A DISPOSITIVE JURISDICTIONAL ISSUE AND REQUESTING TERMINATION OF THIS INVESTIGATION

Pursuant to 19 C.F.R. §§ 210.19, Advanced Micro Devices, Inc. ("AMD"), ATI Technologies ULC and ATI International SRL (collectively, "ATI") respectfully move to intervene for the limited purpose of raising a dispositive jurisdiction issue and requesting that the United States International Trade Commission ("Commission") terminate this Investigation.

AMD and ATI seek to intervene in this Investigation on the side of respondents to raise one narrow issue not previously raised by the parties, but which goes to the heart of the Commission's jurisdiction. The Commission lacks jurisdiction over this Investigation because ATI owns the asserted patents and declines to participate as a complainant. *SiRF Tech., Inc. v. ITC*, 601 F.3d 1319, 1325–26 (Fed. Cir. 2010); *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, ITC LEXIS 455 Order No. 49, 2005 (ITC June 8, 2005); *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, 2007 ITC LEXIS 117, at *8–9 (ITC Feb. 6, 2007).

The prior owner of the asserted patents, SONICblue Incorporated ("SONICblue") assigned the patents to ATI [

]

SONICblue and ATI have recently executed and recorded an acknowledgment of this prior assignment of the asserted patents with the United States Patent and Trademark Office ("PTO"). Exs. 2, 25. ATI executed this acknowledgement on SONICblue's behalf pursuant to a power of attorney given to ATI to "take any and all reasonable action designed to vest more fully in ATI and the Purchasers the Acquired Assets" and to provide for ATI "the benefit, use, enjoyment and possession of such Acquired Assets." Ex. 1, ¶ 2.

Complainants S3 Graphics Co., Ltd. and S3 Graphics, Inc. (collectively "S3G") cannot supplant ATI's ownership of the asserted patents by pointing to a purported assignment effective November 14, 2006 or documents recorded May 7, 2002 and attached as Exhibit 5 to its Complaint ("May 7, 2002 Documents"). S3G did not even attempt to rely on the November 2006 assignment documents to establish ownership of the asserted patents. Ex. 4, Reel 026598 Frame 0180; Exs. 3, 5, 6. By November 2006, SONICblue had no rights in the asserted patents to assign to S3G because SONICblue had already transferred the asserted patents to ATI more than 5 years earlier. S3G, moreover, is not a bona fide purchaser without notice of the prior

transfer to ATI because S3G clearly had notice of SONICblue's FireGL Business and the sale of that entire business to ATI.

S3G's Complaint appears to rely solely on the May 7, 2002 Documents. Ex. 15, Reel 012852 Frame 0016-34. But these documents do not show an assignment of the asserted patents from SONICblue to S3G, and the documents were not included in any of the PTO assignment records for any of the asserted patents. Ex. 3–6. These documents obviously do not contain an assignment of the asserted patents to S3G because S3G would not have obtained an assignment from SONICblue in 2006 if the asserted patents had already been assigned. At most, the May 7, 2002 Documents reflect nothing more than an assignment of specific patents listed in "the attached Schedule A." None of the asserted patents, or even any of the pending patent applications that issued as asserted patents, is identified as being assigned or listed on Schedule A.

Even if the May 7, 2002 Documents effectively memorialized an earlier assignment to S3G, ATI would still own the asserted patents. ATI acquired any rights that may have been assigned to S3G [

] In addition, any earlier assignment reflected in the May 7, 2002 Documents is void because ATI is a subsequent purchaser for valuable consideration without notice of any prior assignment to S3G. [

I

Because ATI owns the patents and declines to participate as a complainant, the Commission has no jurisdiction over this Investigation. Accordingly, AMD and ATI should be granted leave to intervene, and the Commission should terminate this Investigation.

AMD and ATI submit the accompanying Memorandum of Points and Authorities in support of their Motion to Intervene for the Limited Purpose of Raising a Dispositive Jurisdictional Issue and Requesting Termination of this Investigation.

Counsel for AMD and ATI contacted S3G, Apple and Staff to inform them of AMD's and ATI's intention to move to intervene. Apple's counsel stated that Apple does not oppose the motion. S3G's counsel stated that S3G will review the written motion and memorandum in support thereof and then respond accordingly. Similarly, the Staff indicated stated that it would not take a position until it had reviewed the papers.

Dated: September 15, 2011

Respectfully submitted,

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Attorneys for Advanced Micro Devices, Inc., ATI Technologies ULC and ATI International SRL

United States International Trade Commission
Investigation No. 337-TA-724
In the Matter of Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software

CERTIFICATE OF SERVICE

The undersigned certifies that, on September 15, 2011, he caused the foregoing document to be served upon the following parties as indicated below:

The Honorable James R. Holbein Secretary U.S. International Trade Commission 500 E Street S.W., Room 112 Washington, D.C. 20436	☒ Original and Four Copies - Via Hand Delivery ☐ Via Electronic Filing
The Honorable E. James Gildea Administrative Law Judge U.S. International Trade Commission 500 E Street S.W., Suite 317-N Washington, D.C. 20436	Two Copies - Via Hand Delivery
Kecia J. Reynolds, Esq. Office of Unfair Import Investigations U.S. International Trade Commission 500 E Street, S.W., Suite 401-A Washington, D.C. 20436	☒ Via Hand Delivery ☐ Via First Class Mail ☐ Via Overnight Delivery ☐ Via Electronic Service
On Behalf of Complainant S3 Graphics Co. Ltd. and S3 Graphics, Inc.: Thomas L. Jarvis, Esq. Finnegan, Henerson, Farabow, Garrett & Dunner LLP 901 New York Ave., NW Washington, DC 20001	☒ Via Hand Delivery ☐ Via First Class Mail ☐ Via Overnight Delivery ☐ Via Electronic Service
On Behalf of Respondent Apple Inc.: Chris R. Ottenweller, Esq Orrick, Herrington & Sutliff LLP 1000 Marsh Road Menlo Park, CA 94025	☐ Via Hand Delivery ☐ Via First Class Mail ☒ Via Overnight Delivery ☐ Via Electronic Service
V. James Adduci, II Andrew F. Pratt Adduci, Mastriani & Schaumberg, L.L.P. 1200 Seventeenth Street, N.W., Fifth Floor Washington, DC 20036	☒ Via Hand Delivery ☐ Via First Class Mail ☐ Via Overnight Delivery ☐ Via Electronic Service

Dated: September 15, 2011

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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of

CERTAIN DIGITAL IMAGING DEVICES AND RELATED SOFTWARE

Investigation No. 337-TA-724

MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT OF ADVANCED MICRO DEVICES, INC., ATI TECHNOLOGIES ULC AND ATI INTERNATIONAL SRL'S MOTION TO INTERVENE FOR THE LIMITED PURPOSE OF RAISING A DISPOSITIVE JURISDICTIONAL ISSUE AND REQUESTING TERMINATION OF THIS INVESTIGATION

PUBLIC VERSION

TABLE OF CONTENTS

PUBLIC VERSION

TABLE OF AUTHORITIES

Page(s)

CASES AND ITC DECISIONS

STATUTES AND OTHER AUTHORITIES

Pursuant to 19 C.F.R. §§ 210.19, Advanced Micro Devices, Inc. ("AMD"), ATI Technologies ULC and ATI International SRL (collectively, "ATI") submit this memorandum in support of their motion to intervene for the limited purpose of raising a dispositive jurisdictional issue not previously raised by the parties to the Investigation, and requesting the United States International Trade Commission ("Commission") to terminate this Investigation.

I. INTRODUCTION

AMD and ATI seek to intervene in this Investigation on the side of respondents to raise one narrow issue not previously raised by the parties, but which goes to the heart of the Commission's jurisdiction. The Commission lacks jurisdiction over this Investigation because ATI owns the asserted patents and declines to participate as a complainant. *SiRF Tech., Inc. v. ITC*, 601 F.3d 1319, 1325–26 (Fed. Cir. 2010); *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, ITC LEXIS 455 Order No. 49, 2005 (ITC June 8, 2005); *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, 2007 ITC LEXIS 117, at *8–9 (ITC Feb. 6, 2007).

The prior owner of the asserted patents, SONICblue Incorporated ("SONICblue") assigned the patents to ATI [

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SONICblue and ATI have recently executed and recorded an acknowledgment of this prior assignment of the asserted patents with the United States Patent and Trademark Office ("PTO"). Exs. 2, 25. ATI executed this acknowledgement on SONICblue's behalf pursuant to a power of attorney given to ATI to "take any and all reasonable action designed to vest more fully in ATI and the Purchasers the Acquired Assets" and to provide for ATI "the benefit, use, enjoyment and possession of such Acquired Assets." Ex. 1, ¶ 2.

Complainants S3 Graphics Co., Ltd. and S3 Graphics, Inc. (collectively "S3G") cannot supplant ATI's ownership of the asserted patents by pointing to a purported assignment effective November 14, 2006 or documents recorded May 7, 2002 and attached as Exhibit 5 to its Complaint ("May 7, 2002 Documents"). S3G did not even attempt to rely on the November 2006 assignment documents to establish ownership of the asserted patents. Ex. 4, Reel 026598 Frame 0180; Exs. 3, 5, 6. By November 2006, SONICblue had no rights in the asserted patents to assign to S3G because SONICblue had already transferred the asserted patents to ATI more than 5 years earlier. S3G, moreover, is not a bona fide purchaser without notice of the prior transfer to ATI because S3G clearly had notice of SONICblue's FireGL Business and the sale of that entire business to ATI.

S3G's Complaint appears to rely solely on the May 7, 2002 Documents. Ex. 15, Reel 012852 Frame 0016-34. But these documents do not show an assignment of the asserted patents from SONICblue to S3G, and the documents were not included in any of the PTO assignment records for any of the asserted patents. Ex. 3–6. These documents obviously do not contain an assignment of the asserted patents to S3G because S3G would not have obtained an assignment from SONICblue in 2006 if the asserted patents had already been assigned. At most, the May 7, 2002 Documents reflect nothing more than an assignment of specific patents listed in

"the attached Schedule A." None of the asserted patents, or even any of the pending patent applications that issued as asserted patents, is identified as being assigned or listed on Schedule A.

Even if the May 7, 2002 Documents effectively memorialized an earlier assignment to S3G, ATI would still own the asserted patents. ATI acquired any rights that may have been assigned to S3G [

] In addition, any earlier assignment reflected in the May 7, 2002 Documents is void because ATI is a subsequent purchaser for valuable consideration without notice of any prior assignment to S3G. [

]

Because ATI owns the patents and declines to participate as a complainant, the Commission has no jurisdiction over this Investigation. Accordingly, AMD and ATI should be granted leave to intervene, and the Commission should terminate this Investigation.

II. BACKGROUND PERTINENT TO AMD AND ATI

A. This Investigation and S3G's Unsupported Allegations that it Owns the Asserted Patents.

S3G submitted its Complaint requesting institution of this Investigation on May 28, 2010. Doc. ID 426439. S3G's Complaint named only one respondent, Apple, Inc. AMD

and ATI were never a party to this Investigation. To the contrary, S3G repeatedly represented to ATI that their devices were not at issue. Ex. 17, Zimmerman Decl., ¶¶ 4, 6, 14.

S3G alleged that Apple has violated 19 U.S.C. §1337 by infringing four patents, U.S. Patent No. 6,658,146, U.S. Patent 6,683,978, U.S. Patent 6,775,417, and U.S. Patent 7,043,087 ("Asserted Patents"). Exs. 8–11. S3G's complaint summarily alleges that "S3 Graphics Co., Ltd., owns by assignment the entire right, title and interest in and to" each of the Asserted Patents. Ex. 14, Complaint at p. 6 ¶ 25, p. 8, ¶ 33, p. 11, ¶ 44, p. 12, ¶ 52. To support this conclusory allegation, S3G relied solely on the May 7, 2002 Documents submitted in Complaint Exhibit 5. Ex. 15. As described below, the May 7, 2002 Documents do not establish that S3G owns the Asserted Patents. *See* Part III.B.2 and III.B.3b.

Based on S3G's complaint, the Commission instituted this Investigation on June 25, 2010. *See* 75 Fed. Reg. 38118. On July 1, 2011, the Administrative Law Judge issued an Initial Determination finding a violation of Section 337 by certain Apple computers. Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond (public version posted Aug. 2, 2011, Doc. ID 455892) (hereafter "ID"). On September 2, 2011, the Commission issued a Notice indicating that the Commission intends to "review the final ID in its entirety." Doc. ID 458512 at p. 2. The Commission, however, should terminate this Investigation because ATI owns the Asserted Patents and declines to participate in this Investigation as a Complainant.

B. ATI Owns the Asserted Patents.

For the Commission's reference, the following table provides a timeline of the relevant events pertinent to ATI's ownership of the Asserted Patents:

Date	Event	Support
Feb. 1998	Named Inventors Zhou Hong, Konstantine I. Iourcha, and Krishna S. Nayak assign their rights to S3 Incorporated.	Ex. 4, Reel 026597 Frame 0409; Exs. 3, 5, 6
07/12/1999	The patent application that issues as U.S. Patent No. 6,658,146 ("'146 Patent") is filed with the PTO.	Ex. 8
11/17/1999	The patent application that issues as U.S. Patent No. 6,683,978 ("'978 Patent") is filed with the PTO.	Ex. 9
11/09/2000	S3 Incorporated changed its name to SONICblue Incorporated.	Ex. 4, Reel 026598 Frame 0136; Ex. 15, Reel 019744 Frame 0136
01/03/2001	SONICblue and VIA Technologies, Inc. ("VIA") form S3 Graphics Co., Ltd. as a joint venture to operate the "Graphics Chip Business." SONICblue owns at least 50% of S3G's voting common stock and its CEO is a founding member of S3G's board. The "Graphics Chip Business" does not include SONICblue's professional graphics products or FireGL Business.	Ex. 12
03/30/2001	[ ]	Ex. 7, § 2.01; Ex. 1
05/07/2002	The May 7, 2002 Documents are recorded in the PTO. The documents record an assignment of specific patents listed in "the Attached Schedule A" from SONICblue to S3 Graphics, Co., Ltd. The May 7, 2002 Documents are not listed in the PTO assignment records of any of the Asserted Patents. Schedule A does not list any of the Asserted Patents or the pending '146 and '978 Patent applications.	Ex. 15, Reel 012852 Frame 0016-34
03/21/2003	SONICblue Inc. files for bankruptcy protection.	Ex. 16, Section 1 ¶ 23

[1]

Date	Event	Support
10/25/2006	ATI Technologies Inc. changes its name to ATI Technologies ULC. AMD acquires ATI in 2006.	Ex. 20
10/31/2006	Settlement Agreement obligating SONICblue to assign intellectual property rights "in its possession" to S3 Graphics Co., Ltd.	Exs. 16, 19
11/14/2006	Effective Date of purported assignment of the Asserted Patents from SONICblue to S3 Graphics Co., Ltd.	Ex. 4, Reel 026598 Frame 0180 Exs. 3, 5, 6
05/28/2010	S3G files Complaint with the Commission alleging infringement of the Asserted Patents by respondent Apple, Inc.	Ex. 14
06/25/2010	The Commission commences Investigation 337-TA-724 based on S3G's Complaint.	75 Fed. Reg. 38118
07/15/2011	S3G records a purported assignment of the Asserted Patents from SONICblue to S3 Graphics Co., Ltd. The Assignment states "this assignment is effective November 14, 2006."	Exs. 3–6
09/13/2011	ATI records acknowledgment by SONICblue and ATI that SONICblue assigned the Asserted Patents to ATI on March 30, 2001. ATI executed the acknowledgement pursuant to a power of attorney SONICblue granted to ATI.	Exs. 2, 25 Exs. 1, ¶ 2

The PTO assignment records for the Asserted Patents reveal an assignment by the inventors to S3 Incorporated in February 1998. Exs. 3–6. They also reflect an assignment from S3 Incorporated to SONICblue in November 2000. *Id.* [

] Pursuant to a power of attorney given to ATI by SONICblue, ATI recently executed an acknowledgment by SONICblue of that prior assignment, which was recorded with the PTO. Exs. 2, 25. After SONICblue assigned the Asserted Patents to ATI, ATI Technologies, Inc. changed its name to ATI

Technologies ULC. Ex. 20. In 2006, AMD purchased ATI. ATI is now a wholly-owned subsidiary of AMD.

C. S3G's Unfounded Ownership Claims.

S3G's claim of ownership of the Asserted Patents rests on allegations that SONICblue assigned those patents to S3G, not ATI. AMD and ATI are aware of only two documents that S3G could claim to be an assignment of the Asserted Patents from SONICblue to S3G: the November 14, 2006 "assignment" recorded in the PTO on July 15, 2011, and the May 7, 2002 Documents. Neither impacts ATI's ownership of the Asserted Patents.

1. The November 14, 2006 "Assignment."

On November 14, 2006, SONICblue purported to assign the Asserted Patents to S3 Graphics Co., Ltd. This assignment was recorded only two months ago, and more than a year after the Commission instituted this Investigation. Exs. 3–6. S3G's Complaint did not rely on this purported assignment as a basis for claiming ownership of the Asserted Patents.

This assignment also proves that S3G did not own the Asserted Patents prior to November 14, 2006. As detailed below in Part III.B.2., SONICblue could not assign the Asserted Patents to S3G in November 2006 because it had already assigned them to ATI more than 5 years earlier. S3G had notice of the 2001 assignment to ATI at least because Mr. Ken Potashner was CEO of SONICblue as well as a director of S3G. S3G also shared the same business address with SONICblue, and SONICblue owned a majority of the voting common stock of S3G.

2. The May 7, 2002 Documents.

S3G's Complaint relies solely on the May 7, 2002 Documents contained in Complaint Exhibit 5 to allege ownership of the Asserted Patents. Ex. 15, Reel 012852 Frame 0016-0034. As discussed in detail in Part III.B.3b., the May 7, 2002 Documents are not listed in

the PTO assignment records for any of the Asserted Patents and do not identify the Asserted Patents by patent number or application number. To the contrary, the May 7, 2002 Documents reflect an assignment of other specific patents identified in "the attached Schedule A." *Id.* at Reel 012852 Frame 0016–21.

Even if the May 7, 2002 Documents sought to assign the Asserted Patents to S3G, they do not impact ATI's ownership rights because the documents were not recorded with the PTO until more than a year after their execution date. [

] Pursuant to 35 U.S.C. § 261, any earlier assignment reflected in the May 7, 2002 Documents is not effective against ATI.

III. ARGUMENT

A. AMD and ATI Should Be Granted Leave to Intervene to Seek Termination of This Investigation.

Under 19 CFR § 210.19, the Commission may grant a motion to intervene to the extent and upon such terms as may be proper under the circumstances. 19 CFR § 210.19. AMD and ATI's intervention is not only proper, but essential under the circumstances of this Investigation because ATI owns the Asserted Patents. Because ATI owns the Asserted Patents and declines to voluntarily participate in this Investigation as a Complainant, the Commission is without jurisdiction to continue this Investigation, and it should be terminated. *SiRF Tech., Inc. v. ITC*, 601 F.3d 1319, 1325–26 (Fed. Cir. 2010); *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, 2005 ITC LEXIS, 455, Order No. 49 (ITC June 8, 2005); *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, 2007 ITC LEXIS 117, at *8–9 (ITC Feb. 6, 2007).

The Commission applies "a strong presumption in favor of intervention" to allow third parties to intervene at any time and under appropriate circumstances. *Certain Garage Door Operators Including Components Thereof*, Inv. No. 337-TA-459, Order No. 5 at p. 3 (Oct. 1, 2001) ("Garage Door Operators"). The Commission follows the criteria for intervention set forth in Rule 24 of the Federal Rules of Civil Procedure. *See, e.g., Certain Baseband Processor Chips and Chipsets, Transmitter and Receiver (Radio) Chips, Power Control Chips, and Products Containing Same, Including Cellular Telephone Handsets*, Inv. No. 337-TA-543, Order No. 27, at p. 3 (n.4 with further cites) (February 15, 2006) ("Baseband Processor Chips").

Intervention is appropriate any time: (1) the proposed intervenor has an interest relating to the property that is the subject of the action; (2) the proposed intervenor is so situated that the disposition of the action may as a practical matter impair or impede its ability to protect that interest; (3) the proposed intervenor's interest is not adequately represented by the existing parties; and (4) the motion to intervene is timely. *See Garage Door Operators,* Inv. No. 337-TA-459, Order No. 5 at p. 3 (Oct. 1, 2001); *Baseband Processor Chips*, Inv. No. 337-TA-543, Order No. 27, at p. 3; *Certain Hardware Logic Emulation Systems and Components Thereof*, Inv. No. 337-TA-383, Order No. 30, at pp. 2, 8–9 (May 14, 1996) ("Hardware Logic Emulation Systems"). These four criteria are liberally construed, with all doubts resolved in favor of the proposed intervenors. *See Am. Renovation & Constr. Co v. United States*, 65 Fed. Cl. 254, 257 (Fed. Cl. 2005) (with further cites); *United States v. Union Elec. Co.*, 64 F.3d 1152, 1158 (8th Cir. 1995); *Elliott Indus. Ltd. P'ship v. BP Am. Prod. Co.*, 407 F.3d 1091, 1103 (10th Cir. 2005). In addition, all well-pleaded, non-conclusory allegations in a motion to intervene and supporting declarations are accepted as true, absent sham, frivolity, or other objections. *See Mendenhall v. M/V Toyota Maru No. 11,* 551 F.2d 55, 56 n.2 (5th Cir. 1977); *Reich v. ABC/York-Estes Corp.,*

64 F.3d 316, 321 (7th Cir. 1995); *Southwest Ctr. for Biological Diversity v. Berg*, 268 F.3d 810, 819-820 (9th Cir. 2001); *see also* 6 JAMES WM. MOORE, MOORE'S FEDERAL PRACTICE – CIVIL § 24.03 [5][a] (3d ed. 2011).

These four criteria all clearly favor intervention by AMD and ATI, particularly in view of the narrowly tailored, dispositive jurisdictional issue for which intervention is sought.

1. AMD and ATI Have an Interest in the Asserted Patents that May Be Impeded or Impaired in This Investigation.

AMD and ATI clearly meet the first two intervention criteria because (1) they have an interest relating to the property that is the subject of this Investigation, and (2) disposition of this Investigation may as a practical matter impair or impede their ability to protect that interest. The Commission permits intervention whenever the proposed intervenor's business or economic interests "could be affected by the Commission's final decision ... in [the] investigation." *Hardware Logic Emulation Systems*, Inv. No. 337-TA-383, Order No. 30 at p. 8 (May 14, 1996); *Garage Door Operators*, Inv. No. 337-TA-459, Comm'n Order at p. 4 (Jan. 7, 2002); *see also Isr. Bio-Eng'g Project v. Amgen Inc.*, 401 F.3d 1299, 1306 (Fed. Cir. 2005) (permitting intervention in patent infringement suit). That S3G's allegations of infringement and the Commission's final decision in this Investigation could impair or impede AMD and ATI's property rights as well as and their business or economic interests cannot be seriously disputed.

First, S3G's is attempting to usurp ATI's ownership rights in the Asserted Patents. As discussed in detail in Part III.B.2, ATI owns the Asserted Patents. S3G has alleged that AMD/ATI Graphics Processing Unit ("GPU") hardware products infringe the Asserted Patents but, as the owner of the patents, ATI is free to practice the claimed inventions. *Microsoft Corp. v. i4i Ltd. P'ship*, 131 S. Ct. 2238, 2242 (2011) ("Once issued, a patent grants certain exclusive

rights to its holder, including the exclusive right to use the invention during the patent's duration. To enforce that right, a patentee can bring a civil action for infringement . . .").

Second, as patent owner, ATI also has the right to exclude others from practicing the invention claimed in these patents. *See, e.g., Morrow v. Microsoft Corp.*, 499 F.3d 1332, 1339–40 (Fed. Cir. 2007). This right to exclude carries with it the right to choose to enforce or to not enforce the Asserted Patents against others, including the right to choose not to enforce the patents against respondent Apple in this Investigation. *See, e.g., Ortho Pharm. Corp. v. Genetics Inst.*, 52 F.3d 1026, 1031 (Fed. Cir. 1995) ("Hence the patent owner may freely license others, or may tolerate infringers . . ."); *W. Elec. Co.* v. *Pacent Reproducer Corp.*, 42 F.2d 116, 118 (2d Cir.), *cert. denied*, 282 U.S. 873 (1930) (same). In this Investigation, however, S3G has appropriated ATI's right to control whether to enforce the patents by asserting that Apple products infringe the Asserted Patents, and seeking to prevent their import and sale.

Third, the Commission's final decision in this Investigation could also impede and impair AMD and ATI's ability to sell AMD/ATI GPU hardware products. The ALJ's initial determination did not find that AMD/ATI's GPU products infringe the Asserted Patents. ID at p. 274. However, the Commission has decided to review the ALJ's initial determination in its entirety. Doc. ID 458512 at p. 2. The possibility that the Commission could exclude Apple products containing AMD/ATI products from being imported or sold suffices to establish that AMD and ATI have substantial interests at stake in the Investigation. *See, e.g., Hardware Logic Emulation Systems*, Inv. No. 337-TA-383, Order No. 30 at p. 8 (May 14, 1996) (Movant was permitted to intervene because "the Movant could be affected by the Commission's final decision on permanent relief in this investigation."); *Garage Door Operators*, Inv. No. 337-TA-459, Comm'n Order at p. 3–4 (Jan. 7, 2002).

2. AMD and ATI's Interests Are Not Adequately Protected Because the Patent Ownership Issue Is Specific to AMD/ATI and Has Not Been Raised by the Existing Parties.

AMD and ATI clearly satisfy the third intervention criteria because AMD and ATI's interests are not adequately represented by the existing parties to this Investigation. This standard for intervention is "satisfied if the applicant shows that representation of his interest 'may be' inadequate; and the burden of making that showing should be treated as minimal." *Trbovich v. United Mine Workers of Am.*, 404 U.S. 528, 538 n.10 (1972). Clearly, the interests of AMD and ATI have not been adequately represented because none of the parties has understood that ATI owns the Asserted Patents. *Isr. Bio-Eng'g Project v. Amgen Inc.*, 401 F.3d 1299, 1306 (Fed. Cir. 2005) (reversing district court's denial of a motion to intervene where proposed intervenor seeks to raise two new bases for defeating the action, including a right to purchase the patented discoveries); *New Century Bank d/b/a Customers Bank v. Open Solutions, Inc.*, No. 10-6537, 2011 U.S. Dist. LEXIS 47340, at *6 (E.D. Pa. May 2, 2011) (permitting intervention where intervenor's argument, namely subject matter jurisdiction, was not previously litigated in the case); *see also Abbott Labs. v. Diamedix Corp.*, 47 F.3d 1128 (Fed. Cir. 1995) (reversing denial of motion to intervene where proposed intervenor retained rights in the asserted patent).

By raising the dispositive jurisdictional issue of patent ownership, AMD and ATI offer a necessary element to this Investigation which would otherwise be neglected, and a perspective which differs materially from that of the present parties. *See, e.g., Sagebrush Rebellion, Inc. v. Watt*, 713 F.2d 525, 528 (9th Cir. 1983) (allowing intervention where intervenor "offers a necessary element to the proceedings that would be neglected," *i.e.*, "a perspective that differs materially from that of the present parties to this litigation"); *Wilderness*

Soc'y v. United States Forest Serv., No. CV08-363-E-EJL, 2011 U.S. Dist. LEXIS 48835, at *8–9 (D. Idaho May 5, 2011).

In addition, AMD and ATI possess knowledge about the ownership of the Asserted Patents that Respondent Apple does not have. *Nat'l Farm Lines v. Interstate Commerce Comm'n*, 564 F.2d 381, 383 (9th Cir. 1977) (holding that the standard for intervention is met when the applicant for intervention possesses experience and knowledge that a party who would allegedly represent its interest does not have). As discussed below, ATI has unique knowledge about the details of the FireGL Business [

] Because Apple cannot adequately represent AMD and ATI on this issue, intervention is appropriate. *See, e.g., Hardware Logic Emulation Systems*, Inv. No. 337-TA-383, Order No. 30 at pp. 1–2, 8; *Isr. Bio-Eng'g Project*, 401 F.3d at 1306 (permitting intervention where arguments raised by intervenor are specific to the intervening party).

3. The Motion to Intervene Is Timely Because It Raises a Jurisdictional Issue That May Be Raised at Any Time.

AMD and ATI's motion to intervene is timely because it raises a dispositive jurisdictional issue. Because ATI owns the Asserted Patents and declines to participate in this Investigation as a Complainant, the Commission lacks jurisdiction to continue this Investigation, and the Investigation should be terminated. A motion to dismiss for lack of jurisdiction may be raised at any time. *Ins. Corp. of Ir., Ltd. v. Compagnie Des Bauxites De Guinee*, 456 U.S. 694, 702 (1982) (holding that "a party does not waive the requirement by failing to challenge jurisdiction early in the proceedings"); *Folden v. United States*, 379 F.3d 1344, 1354 (Fed. Cir. 2004) ("Subject-matter jurisdiction may be challenged at any time . . ."); *Elliott Indus. Ltd. P'ship v. BP Am. Prod. Co.*, 407 F.3d 1091, 1103–04 (10th Cir. 2005) (permitting intervention

on appeal to raise subject matter jurisdiction); *Duplan v. Harper*, 188 F.3d 1195, 1203 (10th Cir. 1999) (same).

Because the issue of the Commission's jurisdiction over an Investigation is one of "public importance," and intervenors' motion is narrowly confined to this important issue, it is timely. *New Century Bank d/b/a Customers Bank v. Open Solutions, Inc.*, No. 10-6537, 2011 U.S. Dist. LEXIS 47340, at *6–7 (E.D. Pa. May 2, 2011) (permitting interventor to raise issue of court's subject matter jurisdiction after case was fully litigated and final judgment on all counts entered); *see also Abbott Labs. v. Diamedix Corp.*, 47 F.3d 1128 (Fed. Cir. 1995) (reversing denial of motion to intervene where proposed intervenor owned the asserted patent). Indeed, the Commission has previously permitted the patent owner to intervene in an Investigation even after remand of a Commission final determination from the United States Court of Appeals for the Federal Circuit. *See Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, Doc. ID 44125 (July 8, 1997).

Although the motion is timely because it goes to the Commission's jurisdiction, AMD and ATI had good reason for not previously investigating this issue. AMD was not named as a respondent. Instead, S3G referred to AMD as a "licensee." Ex. 17, Zimmerman Decl. ¶¶ 3, 14, 16. During the Investigation, S3G repeatedly represented that AMD and ATI's products were not at issue in this Investigation. *Id.* at ¶¶ 4, 6, 14. This changed, however, when S3G accused the Apple computers of infringing based on AMD/ATI GPUs found in those computers. While the public version of the ALJ's ID issued August, 2, 2011 did not find that the AMD and ATI products infringe (ID at 272–74), the ID and Commission's Notice of September 2, 2011 heightened the risk that the Apple computers might be found to infringe based on the inclusion of AMD/ATI GPUs despite S3G's complaint representation that AMD/ATI was "licensed" and

repeated representations that AMD/ATI's products were not at issue. The ALJ's ID sanctioned Apple by drawing adverse inferences from the failure to disclose AMD's driver source code software, cracking the door open for S3G to seek from the Commission a broader sanction that could result in a finding that Apple computers containing AMD/ATI GPUs infringe. The Commission's notice of intent to review the ALJ's ID opened the door wider to that possibility by deciding to review the ID in its entirety.

At that point, AMD and ATI undertook a thorough assessment of the case and potential defenses, including an examination of the veracity and accuracy of S3G's statements to the Commission that it owned the patents and that AMD and ATI may have been licensed. This assessment led to an investigation of ATI's 2001 purchase of the FireGL Business, caused AMD and ATI to examine information relating to the FireGL Business it acquired over 10 years ago, and led AMD and ATI to recognize that ATI owned the Asserted Patents. Once AMD and ATI learned that ATI owned the Asserted Patents, AMD and ATI promptly sought to intervene.

B. The Commission Should Terminate this Investigation Because ATI Owns the Asserted Patents and the Commission Lacks Jurisdiction.

As detailed below, SONICblue clearly assigned the Asserted Patents to ATI on March 30, 2001 when ATI acquired SONICblue's FireGL Business. S3G has offered, and there is, no evidence of any alleged transfer of these Asserted Patents from SONICblue to S3G that could supplant ATI's ownership of the Asserted Patents.

1. This Investigation Cannot Proceed if S3G Does Not Own the Asserted Patents.

Standing to sue is a threshold jurisdictional issue in every ITC Investigation that is based on an assertion that private intellectual property rights have been infringed. *SiRF Tech.*, 601 F.3d at 1325–26; *Certain Catalyst Components & Catalysts for the Polymerization of Olefins,* Inv. No. 337-TA-307, 1990 ITC LEXIS 224, at *10, *16, *26–27, Order No. 23 (June

25, 1990) (hereafter "Catalyst Components"). The Commission has made clear that "infringement actions may only be brought by, or in the name of, all of the owners of the patent in suit or the exclusive licensee of all of the rights covered by the patent." *SiRF Tech., Inc.*, 601 F.3d at 1326 n.4, (*citing Catalyst Components*, 1990 ITC LEXIS 224, at *10, *16 (ITC June 25, 1990)). Commission Rule 210.12(a)(7) confirms that a complainant must demonstrate that it is the "owner" or "exclusive licensee" of the Asserted Patents. 19 CFR § 210.12(a)(7).

As complainant, S3G has the burden of establishing that it has standing. *SiRF Tech., Inc.*, 601 F.3d at 1327; *Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same*, Inv. No. 337-TA-605, 2008 ITC LEXIS 2267, at *22 (ITC Dec. 1, 2008). S3G cannot meet that burden because ATI owns the Asserted Patents.

2. ATI Owns the Asserted Patents.

ATI owns the Asserted Patents because SONICblue assigned these patents to ATI

[

] Under Delaware law, a court is "constrained" to effectuate the parties' intent "by a combination of the parties' words and the plain meaning of those words." *Lorillard Tobacco Co. v. Am. Legacy Found.*, 903 A.2d 728, 739 (Del. 2006); *Nw. Nat'l Ins. Co. v. Esmark, Inc.*, 672 A.2d 41, 43 (Del. 1996). "When the language of a . . . contract is clear and unequivocal, a party will be bound by its plain meaning because creating an ambiguity where none exists could, in effect, create a new contract with rights, liabilities and duties to which the parties had not assented. . . ." *Lorrillard,* 903 A.2d at 739. Moreover, "[a] contract is not rendered ambiguous simply because the parties do not agree upon its proper construction." *Id.*

"Ambiguity does not exist where a court can determine the meaning of a contract without any other guide than a knowledge of the simple facts on which, from the nature of language in general, its meaning depends. Courts will not torture contractual terms to impart ambiguity where ordinary meaning leaves no room for uncertainty." *Id. quoting Rhone-Poulenc Basic Chems. Co. v. Am. Motorists Ins. Co.,* 616 A.2d 1192, 1195–96 (Del. 1992).

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[2] See Ex. 7 at p. 1, initial paragraph "ASSET PURCHASE AGREEMENT, dated as of March 30, 2001, among SONICblue Incorporated, a Delaware corporation (the "Seller")...."

[

] "Where an agreement expressly identifies excluded assets, and then conveys 'all assets' except those so excluded, there is no room for a finding of ambiguity in its language." *Turner v. Officers, Directors & Employees of Mid Valley Bank*, 712 F. Supp. 1489; 1497 (E.D. Wa. 1988) (holding that all assets including intangible cause of action were assigned by purchase agreement); *see also EMD Crop Bioscience Inc. v. Becker Underwood, Inc.*, 750 F. Supp. 2d 1004, 1013 (W.D. Wis. 2010).

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] The patent applications that issued as U.S. Patent 6,658,146 and U.S. Patent 6,683,978 were being prosecuted in the PTO on March 30, 2001. Exs. 8, 9. According to PTO records, each of these patent applications was actively being prosecuted on behalf of SONICblue pursuant to a power of attorney granted by S3 Incorporated.[3] Exs. 21, 22. Patent applications are considered personal property, and "35 U.S.C. § 261 makes clear that an application for patent as well as the patent itself may be assigned." *Filmtec Corp. v. Allied-Signal Inc.*, 939 F.2d 1568, 1572 (Fed. Cir. 1991).

Although the patent applications that issued as U.S. Patents No. 6,775,417 (the "'417 Patent"), and U.S. Patent 7,043,087 (the "'087 Patent) had not been on file on March 30, 2001, [

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[3] S3 Incorporated became SONICblue Incorporated in November 2000. Exs. 3–6.

[application.] *See, e.g., Bd. of Trustees of the Leland Stanford Junior Univ. v. Roche Molecular Sys., Inc.*, 583 F.3d 832, 842 (Fed. Cir. 2009) and 487 F. Supp. 2d 1099, 1107 (N.D. Ca. 2007) (broad language in VCA Agreement assigning rights in "ideas, inventions and improvements … that relate in any manner to the actual or anticipated business" assigns right to subsequently applied for and issued patents); *Filmtec Corp. v. Allied-Signal Inc.*, 939 F.2d 1568, 1572 (Fed. Cir. 1991); *EMD Crop Bioscience Inc. v. Becker Underwood, Inc.*, 750 F. Supp. 2d 1004, 1013 (W.D. Wis. 2010). [

] The '417 Patent issued from a continuation-in-part of the '146 Patent application. ID p. 7, Ex. 10. The '087 Patent issued from a continuation of the '417 Patent application. ID p. 4, Ex. 11.[4]

The Asserted Patents were also used in, held for use in, and intended for use in the FireGL Business because several of the FireGL Products that ATI acquired, including, without limitation, the FireGL 2, 3 and 4 products, support S3TC Texture Compression. Ex. 26, Declaration of Kevin O'Neil. The United States Supreme Court has indicated that the term "use" has a very broad definition, and includes any way that an invention is put into practice. *Bauer & Cie v. O'Donnell*, 229 U.S. 1, 10–11 (1913) ("The right to use is a comprehensive term and embraces within its meaning the right to put into service any given invention."); *NTP, Inc. v. Research in Motion, Ltd.*, 418 F.3d 1282, 1316–17 (Fed. Cir. 2005) ("[T]he Supreme Court

[4] As discussed *infra* at Part III.B.3bii, the Asset Purchase Agreement and Bill of Sale and Assignment also transferred to ATI any rights in the Asserted Patents that may have been transferred to S3 Graphics Co., Ltd. prior to March 30, 2001. The Acquired Assets include all rights owned by the Seller [SONICblue] or "its Subsidiaries." S3 Graphics Co., Ltd. is a "Subsidiary" of SONICblue under the Asset Purchase Agreement.

stated that 'use' . . . is a 'comprehensive term and embraces within its meaning the right to put into service any given invention.' . . . The ordinary meaning of 'use' is to 'put into action or service.'"). In this Investigation, S3G has asserted that graphics products that support S3TC texture compression or decompression practice the inventions claimed in the Asserted Patents. ID at p. 272-74. [

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c) Other Provisions of the Asset Purchase Agreement Confirm that the Asserted Patents are "Acquired Assets" that SONICblue Assigned to ATI.

Other provisions of the Asset Purchase Agreement further confirm that the Asserted Patents were Acquired Assets that SONICblue assigned to ATI when it sold the "FireGL Business." [

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d) SONICblue and ATI Have Recently Executed an Acknowledgement of the March 30, 2001 Assignment of the Asserted Patents to ATI.

Finally, SONICblue and ATI recently confirmed in writing that SONICblue assigned the Asserted Patents to ATI on March 30, 2001. *See, e.g., Cadles of Grassy Meadows II, LLC v. Mackinnon,* No. 91-10432-WGY, 2010 U.S. Dist. LEXIS 22553, at *9–11 (D. Ma. March 11, 2010) (giving effect to acknowledgment of prior assignment executed in 2009 pursuant to power of attorney as evidence that certain interest had been assigned in 2006). On September 6, 2011, SONICblue and ATI executed an acknowledgment of the prior assignment and transfer of the Asserted Patents to ATI on March 30, 2001. That acknowledgment explicitly states:

> **NOW, THREFORE, TO ALL WHOM IT MAY CONCERN:**
>
> Be it known that for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the Assignor and Assignee agree that when Assignor sold, assigned, transferred, conveyed and delivered to Assignee all of the assets, properties, goodwill and business of every kind and description and wherever located, owned by the Assignor or its
>
> Subsidiaries or used or held for use by the Assignor or its Subsidiaries in the FireGL Business other than the Excluded Assets including, except for the Excluded Assets all right, title and interest in, to and under all other assets, rights and claims of every kind and nature used or intended to be used or held for use in the operation of the FireGL Business, pursuant to the Bill of Sale and Assignment on March 30, 2001, Assignor intended to sell, assign, transfer, convey and deliver, and did sell, assign, transfer, convey and set over to Assignee, Assignor's entire right, title and interest in and to all patents and patent applications owned by the Assignor or its Subsidiaries or used or intended to be used or held for use by the Assignor or its Subsidiaries in the FireGL Business, including but not limited to the patents and patent applications listed in Schedule 1, and any and all reissues, continuations, continuations-in-part, divisions, extensions, reexaminations and renewals of and substitutes for said applications and all rights therein provided by multinational treaties or conventions and all improvements to the inventions disclosed in each such registration, patent or application, and in, to and under any and all Letters Patent which may be granted on or as a result thereof in the United States and any and all other countries, and any reissue or reissues or extension or extensions of said Letters Patent; and does

Schedule 1

Application Serial No.	U.S. Patent No.
U.S. Ser. No. 09/351,930	U.S. 6,658,146
U.S. Ser. No. 09/442,114	U.S. 6,683,978
U.S. Ser. No. 10/052,613	U.S. 6,775,417
U.S. Ser. No. 10/893,084	U.S. 7,043,087

Ex. 2. ATI duly recorded this acknowledgement with the PTO on September 13, 2011. Ex. 25.

As in *Cadles*, ATI executed this acknowledgment on behalf of SONICblue pursuant to a power of attorney that SONICblue granted in the Bill of Sale and Assignment. Ex. 1, § 2. SONICblue appointed ATI, as well as its respective successors and assigns, the true and lawful attorney and attorneys of SONICblue "to take any and all reasonable action designed to vest more fully in ATI and the Purchasers the Acquired Assets hereby sold and assigned to ATI and the Purchasers or intended so to be and in order to provide for ATI and the Purchasers the benefit, use, enjoyment and possession of such Acquired Assets." Ex. 1, § 2. The powers of attorney granted by SONICblue "are coupled with an interest" and are "irrevocable by it or upon [SONICblue's] subsequent dissolution or in any manner or for any reason." *Id.*

3. S3G Cannot Supplant ATI's Ownership of the Asserted Patents.

S3G's claim that it owns the Asserted Patents rests on allegations that SONICblue assigned those patents to S3G, not ATI. AMD and ATI are aware of only two documents that S3G could claim to be an assignment of the Asserted Patents from SONICblue to S3G: the November 14, 2006 "assignment" recorded in the PTO on July 15, 2011 and the May 7, 2002 Documents recorded in the PTO and attached as Complaint Exhibit 5. Neither undermines ATI's ownership of the Asserted Patents.

a) The Purported November 14, 2006 Assignment from SONICblue Does Not Impact ATI's Ownership of the Asserted Patents.

The PTO Records reveal that just two months ago, and over a year after this Investigation commenced, S3G recorded a purported assignment of the Asserted Patents from SONICblue. Exs. 3–6. The document filed with the PTO indicates that "[t]his "assignment is effective November 14, 2006":

This assignment is effective November 14, 2006.

SONICblue Incorporated

Signed at San Jose, CA
This 15th **day of** January, **2007**

Ex. 4, Reel 026598 Frame 0180.

The November 14, 2006 assignment cannot operate to establish that S3G owns the Asserted Patents. SONICblue had no rights in the Asserted Patents to assign to S3G in 2006 because it had already assigned the Asserted Patents to ATI more than 5 years earlier. *See supra* Part III.B.2.; *see, e.g.*, *Six Wheel Corp. v. Sterling Motor Truck Co. of Ca.*, 50 F.2d 568, 570 (9th Cir. 1931) ("Obviously [the assignor] cannot assign more than he has..."); *see also EMD Crop Bioscience Inc. v. Becker Underwood, Inc.*, 750 F. Supp. 2d 1004, 1012 (W.D. Wis. 2010) ("[Section 261] does not address the legal validity of an assignment."); *TM Patents, L.P. v. Int'l Bus. Machs.*, 121 F. Supp. 2d 349, 365 (S.D.N.Y. 2000) ("Clearly, § 261 does not grant an assignee any title better than the assignor had.").

Nor can S3G rely on the provisions of 35 U.S.C. § 261 to negate ATI's ownership. Under § 261, "[a]n assignment, grant, or conveyance shall be void as against any subsequent purchaser or mortgagee for a valuable consideration, without notice, unless it is recorded in the Patent and Trademark Office within three months from its date or prior to the

date of such subsequent purchase or mortgage." 35 U.S.C. § 261. S3G cannot claim the benefit of § 261 because S3G is not a subsequent purchaser without notice of the prior assignment to ATI. A subsequent purchaser is on notice of a prior assignment when the purchaser has actual, constructive or inquiry notice of a prior assignment. *Bd. of Trustees of the Leland Stanford Junior Univ. v. Roche Molecular Sys., Inc.*, 583 F.3d 832, 843 (Fed. Cir. 2009) ("'Notice' under § 261 can include constructive or inquiry notice, in addition to actual notice.").

The evidence clearly demonstrates that S3G had actual notice, or at the very least constructive or inquiry notice, that SONICblue sold the entire FireGL Business to ATI before the November 14, 2006 "assignment." Public documents state that S3 Graphics Co., Ltd. was formed as a joint venture between SONICblue and VIA shortly before ATI acquired the FireGL Business. Ex. 12. SONICblue owned a majority of the voting common stock of S3G. Ex. 12, p. 16 (Joint Venture Agreement at § 2.4.1). SONICblue's CEO, Mr. Ken Potashner, was a founding director of S3G with a term that continued until 2003. Ex. 12, pp. 17 (§ 3.2), 26. Because Mr. Potashner was CEO of SONICblue as well as a director of S3G, S3G may have had actual notice. At the very least, S3G had constructive or inquiry notice that SONICblue had sold its entire FireGL Business in March 2001 to ATI.

For example, S3G clearly had notice through Mr. Potashner that SONICblue had sold its entire FireGL Business to ATI and that the S3G joint venture did not include any of the assets used in the FireGL Business. S3G clearly knew, at least through Mr. Potashner as well as through board members who had ties to VIA, that the "Graphic Chip Business" the S3G joint venture would operate did not include SONICblue's professional graphics products or FireGL business. The ARIA executed by SONICblue and VIA explicitly states that the "Graphic Chip Business" does not include "S3's professional graphics business (e.g., the FireGL graphics board

product line) which S3 conducts through its professional graphics divisions." Ex. 13, §1. S3G also knew, at least through Mr. Potashner, that SONICblue had sold its entire FireGL Business to ATI. *See, e.g., Thomas v. Tomco Acquisitions, Inc.*, 776 F. Supp. 431, 435–36 (E.D. Wis. 1991) (holding that assignee of patents was not a subsequent purchaser without notice under §261 because the purchase "wore two hats: he was president of Tomco when the patents were originally surrendered to Maryland National . . . as well as a 'subsequent purchaser' of the disputed patents from Tomco two years later . . ."); *Filmtec Corp. v. Allied-Signal Inc.*, 939 F.2d 1568, 1574 (Fed. Cir. 1991) ("Since Cadotte was one of the four founders of FilmTec, and the other founders and officers were also involved at MRI, FilmTec may well be deemed to have had actual notice of an assignment. Given the key roles that Cadotte and the others played both at MRI and later at FilmTec, at a minimum FilmTec might be said to be on inquiry notice of any possible rights in MRI or the Government as a result of Cadotte's work at MRI."). S3G clearly was not a bona fide purchase without notice of the assignment to ATI when it received the purported assignment from SONICblue effective November 14, 2006.

b) The May 7, 2002 Documents Cited in S3G's Complaint Do Not Affect ATI's Ownership of the Asserted Patents.

Tellingly, S3G does not rely on the November 2006 assignment that is actually reflected in the PTO assignment records of the Asserted Patents in its Complaint. Instead, to support its assertion that "S3 Graphics Co., Ltd., owns by assignment the entire right, title, and interest in and to" each particular patent, S3G relies solely on the May 7, 2002 Documents attached as Complaint Exhibit 5. Ex. 14, Complaint p. 6 ¶ 25, p. 8, ¶ 33, p. 11, ¶ 44, p. 12, ¶ 52; Ex. 15. As demonstrated below, the May 7, 2002 Documents have no impact ATI's ownership of the Asserted Patents.

i) The May 7, 2002 Documents Do Not Include an Assignment of the Asserted Patents to S3G.

The May 7, 2002 Documents do not include an assignment of any of the Asserted Patents. Ex. 15, Reel 012852 Frame 0016–34. Unlike the November 14, 2006 assignment, the May 7, 2002 Documents are not included in the PTO assignment records for any of the Asserted Patents. Exs. 3–6. These documents appear to include an assignment from SONICblue to S3 Graphics Co., Ltd. of specific patents identified in "the attached Schedule A":

05-16-2002

Form PTO-1595 (Rev. 03/01)
OMB No. 0651-0027 (exp. 5/31/2002)
Tab settings ⇨⇨⇨

102092001

U.S. DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):
SONICblue Incorporated
5-7-02

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

3. Nature of conveyance:
☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Other

Execution Date: January 3, 2001

2. Name and address of receiving party(ies)
Name: S3 Graphics Co., Ltd.
Internal Address:
Street Address: Charles Adams, Ritchie & Duckworth
Zephyr House, Mary Street, P.O. Box 709
Grand Cayman, British West Indies

Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or patent number(s):
If this document is being filed together with a new application, the execution date of the application is:
A. Patent Application No.(s)
B. Patent No.(s)
(Please see the attached Schedule A)

Additional numbers attached? ☒ Yes ☐ No

Ex. 15, Reel 012852 Frame 0016. This document, however, does not reflect an assignment of any of the Asserted Patents. Although Schedule A identifies U.S. Patent 5,956,431 and other patents that are not asserted in this Investigation, none of the Asserted Patents is listed. This document also contains a space to identify assigned patent applications, but no applications are listed even though the '146 and '987 Patent applications were on file and being prosecuted. In fact, none of the May 7, 2002 Documents indentifies any of the then-pending patent applications

for the '146 and '987 Patents by application number. *Id.* at Frame 0016–34.[5] The explicit reference to an assignment of particular patents in Schedule A, and the omission of any reference to any patent applications when two of the patent applications that issued as Asserted Patents were pending, is a clear indication that the May 7, 2002 Documents assigned only the patents identified in Schedule A and did not assign the Asserted Patents. 37 C.F.R. § 3.21 ("An assignment relating to a patent must identify the patent by the patent number. An assignment relating to a national patent application must identify the national patent application by the application number (consisting of the series code and the serial number, e.g., 07/123,456). . . .").

The November 14, 2006 assignment and other documents pertaining to that assignment confirm that the Asserted Patents were not transferred to S3G in 2001. The 2006 Assignment clearly states that "this assignment is effective" November 14, 2006. Ex. 4, Reel 026598 Frame 0179–88. SONICblue appears to have executed this "assignment" in response to an October 2006 Settlement Agreement between SONICblue, S3G, VIA and Intel Corp. to settle litigation Intel commenced to terminate a Patent Cross License Agreement with SONICblue. Ex. 16. The Settlement Agreement obligates SONICblue to "use its commercially reasonable best efforts to transfer" the "intellectual property related to or used in the Graphics Chip Business ***that currently remains in [SONICblue's] possession***, ... and was to be contributed pursuant to

[5] The other documents that appear to have been recorded on May 7, 2002 either confirm that the Asserted Patents were not assigned to S3G or appear entirely unrelated to the Asserted Patents. Ex. 15, Reel 012852 Frame 0022-0034. For example, one document purports to be an assignment by SONICblue to S3 Graphics Co., Ltd of "the inventions and patent applications and disclosures listed in Schedule 1 annexed hereto." *Id.* at Frame 0022. But in contrast to the attached Schedule A, no document identified as "Schedule 1" accompanies the submission. The document that follows this assignment appears to be an entirely unrelated assignment from some individuals to SONICblue's predecessor, S3 Incorporated.

the Amended and Restated Investment Agreement."[6] Ex. 16, Doc. 2158-3 (filed 2/16/2007), § 5 (emphasis added); Ex. 19. The Settlement Agreement further requires SONICblue to execute "transfer documents relating to all patents and patent applications listed on Schedule 1 to the Bill of Sale (as defined in the Amended and Restated Agreement), and patents, trademarks, copyrights, and other items listed in Schedule 3.14(a)(ii) to the Amended and Restated Investment Agreement." *Id.* at § 5a. The bankruptcy court authorized SONICblue to enter into the Settlement Agreement on October 31, 2006, including authorizing the execution of documentation reasonably necessary to transfer "the intellectual property related to or used in the Graphics Chip Business in SONICblue's possession to S3G Co. or its designee...." Ex. 19, at p. 5 line 27 to p. 6, line 3. SONICblue then executed the assignment effective November 14, 2006. Although AMD and ATI have not had access to either Schedule 1 or Schedule 3.14(a)(ii) referred to in the Settlement Agreement because S3G has designated them confidential, the Settlement Agreement, Court Order, and SONICblue's purported assignment of the Asserted Patents to S3G in 2006 indicate clearly that SONICblue had not previously assigned the Asserted Patents to S3G. S3G would have no reason to identify the Asserted Patents as intellectual property in SONICblue's "possession," and to demand that SONICblue assign the Asserted Patents in 2006 if those patents had already been assigned to S3G years earlier.

The terms of the agreements between SONICblue and ATI relating to SONICblue's sale of the FireGL Business, and the agreement between SONICblue and VIA to form the S3G joint venture further confirm that SONICblue transferred the Asserted Patents to ATI. As discussed above, the agreements between SONICblue and ATI broadly transferred all

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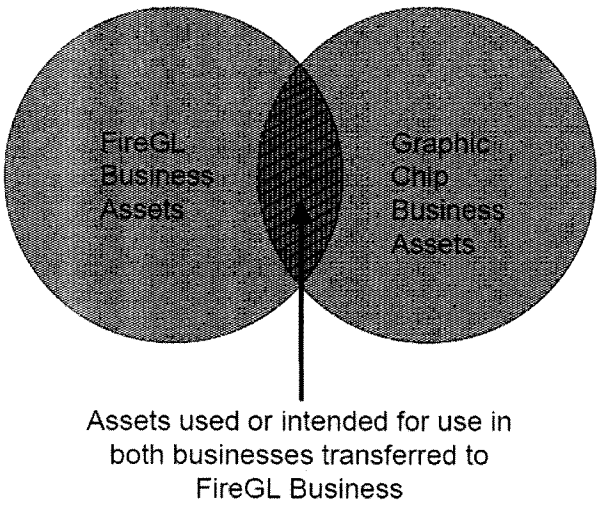
[6] As discussed *infra* at 32–33, the intellectual property used in the "Graphics Chip Business" did not include the Asserted Patents because the Graphics Chip Business does not include professional graphics products or the FireGL Business.

assets used in, held for use in, or intended for use in the FireGL Business whether owned by SONICblue or its Subsidiaries. By contrast, SONICblue's agreement with VIA to create S3G was narrower and made clear that anything relating to the FireGL Business was not part of the S3G joint venture. The ARIA signed by SONICblue and VIA explicitly states that the "Graphics Chip Business" to be operated by S3G does not include the professional graphics business and FireGL graphics board product line.

> "Graphics Chip Business" shall mean S3's current business which involves the development, design, and manufacture of discrete graphics chips or discrete graphics chips integrated with core logic. ***Notwithstanding anything to the contrary herein, the Graphics Chip Business shall not include S3's board or add-in card business even though the products of such business contain graphics chips or provide graphics functionality to their users or S3's professional graphics business (e.g., the FireGL graphics board product line) which S3 conducts through its professional graphics divisions.***

Ex. 13, § 1 (emphasis added.). In effect, the plain meaning of the terms in these agreements set up a structure where all assets and property that may have been used in both SONICblue's FireGL Business and the graphics business intended for the S3G joint venture were assigned to the FireGL Business and were not included in the graphics business to be operated by the S3G joint venture:



ii) ATI Owns the Asserted Patents Even if the May 7, 2002 Documents Contain an Earlier Assignment to S3G.

The May 7, 2002 Documents identify an execution date of "January 3, 2001." Ex. 15, Reel 012852 Frame 0016. The assignment was not recorded until May 7, 2002, more than three months after the execution date, and more than a year after SONICblue assigned the Asserted Patents to ATI on March 30, 2001. As a result, any assignment of the Asserted Patents in the May 7, 2002 Documents is void under 35 U.S.C. § 261 because ATI is a subsequent purchaser for valuable consideration without notice of the prior assignment to S3G.

[

]

[

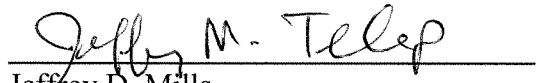
] S3G

owned at least 50% of the voting common stock with other undisclosed joint venture partners owning 48% and 2% respectively. Ex. 12, § 2.4.1. Thus, any rights that S3G may have possessed in the Asserted Patents when ATI acquired the FireGL Business were assigned or transferred to ATI under the "owned by ... Subsidiaries" clause of the Asset Purchase Agreement.

IV. CONCLUSION

For the foregoing reasons, AMD and ATI's motion to intervene should be granted, and the Commission should enter an order terminating the Investigation because S3G does not own the Asserted Patents. Alternatively, the Commission should grant AMD and ATI's motion to intervene and remand this proceeding to the Administrative Law Judge for an Initial Determination regarding S3G's standing and ATI's rights in the Asserted Patents.

Respectfully submitted,



Jeffrey D. Mills
Amina S. Dammann
KING & SPALDING, LLP
401 Congress Avenue, Suite 3200
Austin, TX 78701

Jeffrey M. Telep
KING & SPALDING, LLP
1700 Pennsylvania Ave NW, Suite 200
Washington, D.C. 20006-4707

Attorneys for Advanced Micro Devices, Inc., ATI Technologies ULC and ATI International SRL

Exhibit 1

BILL OF SALE AND ASSIGNMENT

BILL OF SALE AND ASSIGNMENT, dated as of March 30, 2001 (this "Bill of Sale and Assignment"), from SONICblue Incorporated, a Delaware corporation (the "Seller") to ATI International SRL, a Barbados society with restricted liability ("SRL"), Concepta Gesellschaft für Immobilieninvestitionen mbH, a German limited liability company ("GmbH"), and ATI Technologies (Europe) Limited, an Irish corporation ("ATL", and together with SRL, the "Purchasers").

W I T N E S S E T H:

WHEREAS, the Seller, ATI Technologies Inc., an Ontario corporation ("ATI"), and the Purchasers have entered into an Asset Purchase Agreement, dated as of March __, 2001 (the "Asset Purchase Agreement"; unless otherwise defined herein, capitalized terms shall be used herein as defined in the Asset Purchase Agreement); and

WHEREAS, the execution and delivery of this Bill of Sale and Assignment by the Seller is a condition to the obligations of ATI and the Purchasers to consummate the transactions contemplated by the Asset Purchase Agreement.

NOW, THEREFORE, for good and valuable consideration to the Seller receipt of which is hereby acknowledged, and pursuant to the Asset Purchase Agreement, the Seller, intending to be legally bound hereby, does hereby agree as follows:

1. Sale and Assignment of Assets and Properties. (a) On the terms and subject to the conditions of the Asset Purchase Agreement, the Seller hereby, on the Closing Date, sells, assigns, transfers, conveys and delivers to ATI and the Purchasers or has caused to be sold, assigned, transferred, conveyed and delivered to ATI and the Purchasers, and ATI and the Purchasers have purchased from the Seller, on the Closing Date, all of the right, title and interest as of the Closing Date of the Seller in and to the Acquired Assets, other than the Excluded Assets, including, without limitation, the following:

(i) all rights pursuant to all customer contracts or purchase orders (whether copies of written or oral) of the FireGL Business, except the Accounts Receivable, together with copies of all supporting files and documentation, in each case as listed in Section 2.01(a)(i) of the Disclosure Schedule of the Asset Purchase Agreement, (the "Customer Contracts");

(ii) all the Seller's right, title and interest in, to and under Intellectual Property as set out in Section 3.19(a) of the Disclosure Schedule of the Asset Purchase Agreement;

(iii) all rights to all revenues due to the Seller or any Subsidiary in connection with all Unshipped Orders;

(iv) all computers and related equipment and furniture that are used in the FireGL Business whether located on the Leased Real Property or any other warehouse dedicated to the FireGL Business as listed in Section 2.01(a)(iv) of the Disclosure Schedule of the Asset Purchase Agreement, (the "Fixed Assets");

(v) all sales and promotional literature, customer lists and other sales-related materials related to the FireGL Business owned, used, associated with or employed by the Seller at the Closing Date;

(vi) all Inventory;

(vii) the goodwill of the Seller relating to the FireGL Business;

(viii) assumption of all third party Licenses, permits or consents issued, granted or given by or under the authority of any Governmental Body or pursuant to any Legal Requirement that are held by the Seller and are used in connection with the FireGL Business and for which Required Consents have either been obtained by the Seller or such condition to closing has been waived by ATI and the Purchasers (collectively "Permits");

(ix) copies of all portions of books of account, general, financial, tax and personnel records, invoices, supplier lists, correspondence and other documents, records and files and all Software and programs and any rights thereto owned, associated with or employed by the Seller or its Subsidiaries or used in, or relating to, the FireGL Business at the Closing Date;

(x) all prepaid expenses and deposits as listed in Section 2.01(a)(x) of the Disclosure Schedule of the Asset Purchase Agreement; and

(xi) except for the Excluded Assets, all the Seller's right, title and interest on the Closing Date in, to and under all other assets, rights and claims of every kind and nature used or intended to be used or held for use in the operation of the FireGL Business.

(b) The Acquired Assets shall exclude the following assets owned by the Seller (the "Excluded Assets"):

(i) all cash, deposits in bank accounts, cash equivalents, and marketable securities;

(ii) all Accounts Receivable;

(iii) all Customer Contracts that are not effectively assigned to ATI or the Purchasers because a Required Consent has not been obtained and such condition to closing has been waived by ATI and the Purchasers;

(iv) all Obsolete Inventory;

(v) the Material Contracts listed in Section 2.01(b)(v) of the Disclosure Schedule; and

(vi) all rights of the Seller under the Asset Purchase Agreement and the Ancillary Agreements.

(c) For the purposes of this Article II, the term Purchasers refers to any of SRL, GmbH or ATL, or a combination of any of them, as determined in the sole discretion of ATI. The Acquired Assets shall be allocated in accordance with Section 2.04 of the Asset Purchase Agreement.

2. Power of Attorney. The Seller hereby constitutes and appoints ATI and the Purchasers, their respective successors and assigns, the true and lawful attorney and attorneys of the Seller with full power of substitution, in the name of ATI or the Purchasers or in the name and stead of the Seller but on behalf of, for the benefit and at the expense of ATI or the Purchasers, their respective successors and assigns, to take any and all reasonable action designed to vest more fully in ATI and the Purchasers the Acquired Assets hereby sold and assigned to ATI and the Purchasers or intended so to be and in order to provide for ATI and the Purchasers the benefit, use, enjoyment and possession of such Acquired Assets. The Seller hereby covenants that, from time to time after the delivery of this instrument, at ATI and the Purchasers' request and without further consideration, the Seller will do, execute, acknowledge, and deliver, or will cause to be done, executed, acknowledged and delivered, all and every such further acts, deeds, conveyances, transfers, assignments, powers of attorney and assurances as reasonably may be required more effectively to convey, transfer to and vest in ATI and the Purchasers, and to put ATI and the Purchasers in possession of, any of the Acquired Assets.

The Seller acknowledges that the foregoing powers are coupled with an interest and shall be irrevocable by it or upon its subsequent dissolution or in any manner or for any reason. ATI and the Purchasers shall be entitled to retain for their own account any amounts collected pursuant to the foregoing powers, including any amounts payable as interest with respect thereto. The Seller shall from time to time pay to ATI and the Purchasers, when received, any amounts which shall be received directly or indirectly by the Seller (including amounts received as interest) in respect of any Acquired Assets sold, assigned or transferred to ATI and the Purchasers pursuant hereto.

3. Obligations and Liabilities Not Assumed. Nothing expressed or implied in this Bill of Sale and Assignment shall be deemed to be an assumption by ATI or the Purchasers of any Excluded Liabilities of the Seller. Neither ATI nor the Purchasers by this Bill of Sale and Assignment assume or agree to pay, perform or discharge any Excluded Liabilities of the Seller of any nature, kind or description whatsoever. The terms and provisions of the assumption of the Assumed Liabilities by ATI and the Purchasers are set forth in the Assumption Agreement dated as of the date hereof among ATI and the Purchasers and the Seller.

4. No Third Party Beneficiaries. This Bill of Sale and Assignment shall be binding upon and inure solely to the benefit of the parties hereto and their permitted assigns and nothing herein, express or implied, is intended to or shall confer upon any other Person any legal or equitable right, benefit or remedy of any nature whatsoever, under or by reason of this Bill of Sale and Assignment.

5. Assignment. This Bill of Sale and Assignment may not be assigned by operation of law or otherwise without the express written consent of the Seller and the

Purchasers (which consent may be granted or withheld in the sole discretion of the Seller or the Purchasers), except by ATI or the Purchasers to one of their Affiliates.

6. Governing Law. This Bill of Sale and Assignment shall be governed by, and construed in accordance with, the laws of the State of Delaware.

IN WITNESS WHEREOF, the Seller has caused this Bill of Sale and Assignment to be executed as of the date first written above by its officer thereunto duly authorized.

SONICBLUE INCORPORATED

By: William F. McFarland
Name: William F. McFarland
Title: VP and CFO

[Corporate Seal]

Attest:

By: David Gershon
Name: DAVID GERSHON
Title: ASST. SECRETARY.

STATE California)
) ss.:
COUNTY OF Santa Clara)

On the 29 day of March, 2001, before me personally came William McFarland to me known, who, being by me duly sworn, did depose and say he resides at 2841 Mission College Blvd; and that he is the CFO of SONICblue Incorporated, the corporation described in and which executed the above instrument; that he knows the seal of said corporation; that the seal affixed to said instrument is such corporate seal; that it was so affixed by order of the Board of Directors and said corporation; that he signed his name thereto by like order; and that he acknowledged said instrument to be the free act and deed of said corporation.

JILL SEWILL
Commission # 1203918
Notary Public — California
Santa Clara County
My Comm. Expires Aug 14, 2004

Jill Sewill
Notary Public

[Notarial Seal]

Exhibit 2

ACKNOWLEDGMENT OF ASSIGNMENT AND TRANSFER OF RIGHTS IN PATENTS AND PATENT APPLICATIONS

WHEREAS, SONICblue, Incorporated (SONICblue Inc.), a corporation organized and existing under the laws of the State of Delaware, having changed its name from S3 Incorporated (S3 Inc.) to SONICblue Incorporated ("Assignor"), and having an office and place of business at 2841 Mission College Boulevard, Santa Clara CA 95054, is the owner of certain patents and patent applications, including the patents and applications listed in Schedule 1 annexed hereto and made a part hereof; and

WHEREAS, ATI Technologies Inc. is an Ontario Corporation that changed its to ATI Technologies ULC in 2006, and ATI International SRL is a Barbados society with restricted liability (together "Assignee");

WHEREAS, on March 30, 2001 Assignor agreed to sell, assign, transfer, convey and deliver to Assignee all of the assets, properties, goodwill and business of every kind and description and wherever located, owned by the Assignor or its Subsidiaries or used or held for use by the Assignor or its Subsidiaries in the FireGL Business other than the Excluded Assets including, except for the Excluded Assets all right, title and interest in, to and under all other assets, rights and claims of every kind and nature used or intended to be used or held for use in the operation of the FireGL Business (the assets to be purchased by Assignee and the Purchasers being referred to as the "Acquired Assets") pursuant to an Asset Purchase Agreement;

WHEREAS, on March 30, 2001 Assignor sold, assigned, transferred, conveyed and delivered to Assignee all of the assets, properties, goodwill and business of every kind and description and wherever located, owned by the Assignor or its Subsidiaries or used or held for use by the Assignor or its Subsidiaries in the FireGL Business other than the Excluded Assets including, except for the Excluded Assets all right, title and interest in, to and under all other assets, rights and claims of every kind and nature used or intended to be used or held for use in the operation of the FireGL Business pursuant to a Bill of Sale and Assignment (Schedule 2);

WHEREAS, the Assignor and Assignee desire to memorialize that the property and assets assigned to Assignee pursuant to the Bill of Sale and Assignment included Assignor's entire right, title, and interest in and to certain patents and patent applications owned by the Assignor or its Subsidiaries or used or intended to be used or held for use by the Assignor or its Subsidiaries in the FireGL Business, including the patents and patent applications listed in Schedule 1 annexed hereto;

NOW, THREFORE, TO ALL WHOM IT MAY CONCERN:

Be it known that for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the Assignor and Assignee agree that when Assignor sold, assigned, transferred, conveyed and delivered to Assignee all of the assets, properties, goodwill and business of every kind and description and wherever located, owned by the Assignor or its

Subsidiaries or used or held for use by the Assignor or its Subsidiaries in the FireGL Business other than the Excluded Assets including, except for the Excluded Assets all right, title and interest in, to and under all other assets, rights and claims of every kind and nature used or intended to be used or held for use in the operation of the FireGL Business, pursuant to the Bill of Sale and Assignment on March 30, 2001, Assignor intended to sell, assign, transfer, convey and deliver, and did sell, assign, transfer, convey and set over to Assignee, Assignor's entire right, title and interest in and to all patents and patent applications owned by the Assignor or its Subsidiaries or used or intended to be used or held for use by the Assignor or its Subsidiaries in the FireGL Business, including but not limited to the patents and patent applications listed in Schedule 1, and any and all reissues, continuations, continuations-in-part, divisions, extensions, reexaminations and renewals of and substitutes for said applications and all rights therein provided by multinational treaties or conventions and all improvements to the inventions disclosed in each such registration, patent or application, and in, to and under any and all Letters Patent which may be granted on or as a result thereof in the United States and any and all other countries, and any reissue or reissues or extension or extensions of said Letters Patent; and does hereby assign to and authorize said Assignee, to file applications for Letters Patent, in all countries, the same to be held and enjoyed by said Assignee, its successors, assigns, nominees or legal representatives, to the full end of the term or terms for which said Letters Patent respectively may be granted reissued or extended, as fully and entirely as the same would have been held and enjoyed by Assignor had this assignment, sale and transfer not been made.

AND Assignor covenants to execute all additional instruments and to do all things necessary for carrying out the purpose of this instrument, at the expense of said Assignee and its successors.

AND Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States and any official of any country or countries foreign to the United States whose duty it is to issue patents on applications as aforesaid, to issue to said Assignee, as assignee of the entire right, title and interest, any and all Letters Patent for said patents, patent applications, and disclosures referred to herein or listed in Schedule 1, including any all Letters Patent of the United States which may be issued and granted on or as a result of the applications aforesaid including all rights therein provided by multinational treaties or conventions and all improvements to the inventions disclosed in each such registration, patent or application, in accordance with the terms of this assignment. This assignment memorializes the prior assignment of March 30th 2001 and is effective on the 30th day of March, 2001.

AGREED to on Behalf of SONICblue, Inc.

By: Kevin O'Neil *

Print Name: Kevin O'Neil

Title: Director, Patents Legal ; ATI Technologies ULC

Date: Sept 6, 2011

* Executed on behalf of SONICblue, Inc. pursuant to power of attorney granted in paragraph 2 of the Bill of Sale and Assignment attached and incorporated as Schedule 2 hereto.

Province ~~State~~ of Ontario
County of York

On September 6, 2011, before me Linda Lam [name of notary public] personally appeared Kevin O'Neil [name of signatory on behalf of SonicBlue, Inc.] personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Linda Lam

AGREED to on Behalf of ATI Technologies ULC

By: [signature]

Print Name: Kevin O'Neil

Title: Director, Patents Legal

Date: Sept 6, 2011

Province ~~State~~ of Ontario
County of York

On September 6, 2011, before me Linda Lam [name of notary public] personally appeared Kevin O'Neil [name of signatory on behalf of ATI Technologies ULC] personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Linda Lam

AGREED to on Behalf of ATI International SRL

By: Robert Feldstein

Print Name: Robert Feldstein

Title: VP Game Console

Date: 9/7/2011

State of Massachusetts
County of Middlesex

On September 7, 2011, before me Christine F. McDade [name of notary public] personally appeared Robert Feldstein [name of signatory on behalf of ATI International SRL] personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

CHRISTINE F. McDADE
Notary Public
COMMONWEALTH OF MASSACHUSETTS
My Commission Expires
April 30, 2015

Christine F. McDade
9/7/11

Schedule 1

Application Serial No.	U.S. Patent No.
U.S. Ser. No. 09/351,930	U.S. 6,658,146
U.S. Ser. No. 09/442,114	U.S. 6,683,978
U.S. Ser. No. 10/052,613	U.S. 6,775,417
U.S. Ser. No. 10/893,084	U.S. 7,043,087

BILL OF SALE AND ASSIGNMENT

BILL OF SALE AND ASSIGNMENT, dated as of March 30, 2001 (this "Bill of Sale and Assignment"), from SONICblue Incorporated, a Delaware corporation (the "Seller") to ATI International SRL, a Barbados society with restricted liability ("SRL"), Concepta Gesellschaft für Immobilieninvestitionen mbH, a German limited liability company ("GmbH"), and ATI Technologies (Europe) Limited, an Irish corporation ("ATL", and together with SRL, the "Purchasers").

WITNESSETH:

WHEREAS, the Seller, ATI Technologies Inc., an Ontario corporation ("ATI"), and the Purchasers have entered into an Asset Purchase Agreement, dated as of March __, 2001 (the "Asset Purchase Agreement"; unless otherwise defined herein, capitalized terms shall be used herein as defined in the Asset Purchase Agreement); and

WHEREAS, the execution and delivery of this Bill of Sale and Assignment by the Seller is a condition to the obligations of ATI and the Purchasers to consummate the transactions contemplated by the Asset Purchase Agreement.

NOW, THEREFORE, for good and valuable consideration to the Seller receipt of which is hereby acknowledged, and pursuant to the Asset Purchase Agreement, the Seller, intending to be legally bound hereby, does hereby agree as follows:

1. Sale and Assignment of Assets and Properties. (a) On the terms and subject to the conditions of the Asset Purchase Agreement, the Seller hereby, on the Closing Date, sells, assigns, transfers, conveys and delivers to ATI and the Purchasers or has caused to be sold, assigned, transferred, conveyed and delivered to ATI and the Purchasers, and ATI and the Purchasers have purchased from the Seller, on the Closing Date, all of the right, title and interest as of the Closing Date of the Seller in and to the Acquired Assets, other than the Excluded Assets, including, without limitation, the following:

(i) all rights pursuant to all customer contracts or purchase orders (whether copies of written or oral) of the FireGL Business, except the Accounts Receivable, together with copies of all supporting files and documentation, in each case as listed in Section 2.01(a)(i) of the Disclosure Schedule of the Asset Purchase Agreement, (the "Customer Contracts");

(ii) all the Seller's right, title and interest in, to and under Intellectual Property as set out in Section 3.19(a) of the Disclosure Schedule of the Asset Purchase Agreement;

(iii) all rights to all revenues due to the Seller or any Subsidiary in connection with all Unshipped Orders;

(iv) all computers and related equipment and furniture that are used in the FireGL Business whether located on the Leased Real Property or any other warehouse dedicated to the FireGL Business as listed in Section 2.01(a)(iv) of the Disclosure Schedule of the Asset Purchase Agreement, (the "Fixed Assets");

(v) all sales and promotional literature, customer lists and other sales related materials related to the FireGL Business owned, used, associated with or employed by the Seller at the Closing Date;

(vi) all Inventory;

(vii) the goodwill of the Seller relating to the FireGL Business;

(viii) assumption of all third party Licenses, permits or consents issued, granted or given by or under the authority of any Governmental Body or pursuant to any Legal Requirement that are held by the Seller and are used in connection with the FireGL Business and for which Required Consents have either been obtained by the Seller or such condition to closing has been waived by ATI and the Purchasers (collectively "Permits");

(ix) copies of all portions of books of account, general, financial, tax and personnel records, invoices, supplier lists, correspondence and other documents, records and files and all Software and programs and any rights thereto owned, associated with or employed by the Seller or its Subsidiaries or used in, or relating to, the FireGL Business at the Closing Date;

(x) all prepaid expenses and deposits as listed in Section 2.01(a)(x) of the Disclosure Schedule of the Asset Purchase Agreement; and

(xi) except for the Excluded Assets, all the Seller's right, title and interest on the Closing Date in, to and under all other assets, rights and claims of every kind and nature used or intended to be used or held for use in the operation of the FireGL Business.

(b) The Acquired Assets shall exclude the following assets owned by the Seller (the "Excluded Assets"):

(i) all cash, deposits in bank accounts, cash equivalents, and marketable securities;

(ii) all Accounts Receivable;

(iii) all Customer Contracts that are not effectively assigned to ATI or the Purchasers because a Required Consent has not been obtained and such condition to closing has been waived by ATI and the Purchasers;

(iv) all Obsolete Inventory;

(v) the Material Contracts listed in Section 2.01(b)(v) of the Disclosure Schedule; and

(vi) all rights of the Seller under the Asset Purchase Agreement and the Ancillary Agreements.

(c) For the purposes of this Article II, the term Purchasers refers to any of SRL, GmbH or ATL, or a combination of any of them, as determined in the sole discretion of ATI. The Acquired Assets shall be allocated in accordance with Section 2.04 of the Asset Purchase Agreement.

2. Power of Attorney. The Seller hereby constitutes and appoints ATI and the Purchasers, their respective successors and assigns, the true and lawful attorney and attorneys of the Seller with full power of substitution, in the name of ATI or the Purchasers or in the name and stead of the Seller but on behalf of, for the benefit and at the expense of ATI or the Purchasers, their respective successors and assigns, to take any and all reasonable action designed to vest more fully in ATI and the Purchasers the Acquired Assets hereby sold and assigned to ATI and the Purchasers or intended so to be and in order to provide for ATI and the Purchasers the benefit, use, enjoyment and possession of such Acquired Assets. The Seller hereby covenants that, from time to time after the delivery of this instrument, at ATI and the Purchasers' request and without further consideration, the Seller will do, execute, acknowledge, and deliver, or will cause to be done, executed, acknowledged and delivered, all and every such further acts, deeds, conveyances, transfers, assignments, powers of attorney and assurances as reasonably may be required more effectively to convey, transfer to and vest in ATI and the Purchasers, and to put ATI and the Purchasers in possession of, any of the Acquired Assets.

The Seller acknowledges that the foregoing powers are coupled with an interest and shall be irrevocable by it or upon its subsequent dissolution or in any manner or for any reason. ATI and the Purchasers shall be entitled to retain for their own account any amounts collected pursuant to the foregoing powers, including any amounts payable as interest with respect thereto. The Seller shall from time to time pay to ATI and the Purchasers, when received, any amounts which shall be received directly or indirectly by the Seller (including amounts received as interest) in respect of any Acquired Assets sold, assigned or transferred to ATI and the Purchasers pursuant hereto.

3. Obligations and Liabilities Not Assumed. Nothing expressed or implied in this Bill of Sale and Assignment shall be deemed to be an assumption by ATI or the Purchasers of any Excluded Liabilities of the Seller. Neither ATI nor the Purchasers by this Bill of Sale and Assignment assume or agree to pay, perform or discharge any Excluded Liabilities of the Seller of any nature, kind or description whatsoever. The terms and provisions of the assumption of the Assumed Liabilities by ATI and the Purchasers are set forth in the Assumption Agreement dated as of the date hereof among ATI and the Purchasers and the Seller.

4. No Third Party Beneficiaries. This Bill of Sale and Assignment shall be binding upon and inure solely to the benefit of the parties hereto and their permitted assigns and nothing herein, express or implied, is intended to or shall confer upon any other Person any legal or equitable right, benefit or remedy of any nature whatsoever, under or by reason of this Bill of Sale and Assignment.

5. Assignment. This Bill of Sale and Assignment may not be assigned by operation of law or otherwise without the express written consent of the Seller and the

Purchasers (which consent may be granted or withheld in the sole discretion of the Seller or the Purchasers), except by ATI or the Purchasers to one of their Affiliates.

6. Governing Law. This Bill of Sale and Assignment shall be governed by, and construed in accordance with, the laws of the State of Delaware.

IN WITNESS WHEREOF, the Seller has caused this Bill of Sale and Assignment to be executed as of the date first written above by its officer thereunto duly authorized.

SONICBLUE INCORPORATED

By: William F. McFarland
Name: William F. McFarland
Title: VP and CFO

[Corporate Seal]

Attest:

By: David Gershon
Name: DAVID GERSHON
Title: ASST. SECRETARY.

STATE California)
) ss.:
COUNTY OF Santa Clara)

On the 29 day of March, 2001, before me personally came William McFarland to me known, who, being by me duly sworn, did depose and say he resides at 2841 Mission College Blvd.; and that he is the CFO of SONICblue Incorporated, the corporation described in and which executed the above instrument; that he knows the seal of said corporation; that the seal affixed to said instrument is such corporate seal; that it was so affixed by order of the Board of Directors and said corporation; that he signed his name thereto by like order; and that he acknowledged said instrument to be the free act and deed of said corporation.

JILL SEWILL
Commission # 1203918
Notary Public — California
Santa Clara County
My Comm. Expires Aug 14, 2004

Jill Sewill
Notary Public

[Notarial Seal]

Exhibit 3

Patent Assignment Abstract of Title

NOTE:Results display only for issued patents and published applications. For pending or abandoned applications please consult USPTO staff.

Total Assignments: 3

Patent #: 6658146 **Issue Dt:** 12/02/2003 **Application #:** 09351930 **Filing Dt:** 07/12/1999

Inventors: KONSTANTINE I. IOURCHA, KRISHNA S. NAYAK, ZHOU HONG

Title: FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES

Assignment: 1

Reel/Frame: 026597/0407 **Recorded:** 07/15/2011 **Pages:** 4

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: IOURCHA, KONSTANTINE I. **Exec Dt:** 02/05/1998

NAYAK, KRISHNA S. **Exec Dt:** 02/03/1998

HONG, ZHOU **Exec Dt:** 02/11/1998

Assignee: S3 INCORPORATED
2801 MISSION COLLEGE BOULEVARD
SANTA CLARA, CALIFORNIA 95052

Correspondent: DANIEL R. MCCLURE
400 INTERSTATE NORTH PKWY SE
SUITE 1500
ATLANTA, GA 30339

Assignment: 2

Reel/Frame: 026598/0134 **Recorded:** 07/15/2011 **Pages:** 3

Conveyance: CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).

Assignor: S3 INCORPORATED **Exec Dt:** 11/09/2000

Assignee: SONICBLUE INCORPORATED
2841 MISSION COLLEGE BOULEVARD
SANTA CLARA, CALIFORNIA 95054

Correspondent: DANIEL R. MCCLURE
400 INTERSTATE NORTH PKWY SE
SUITE 1500
ATLANTA, GA 30339

Assignment: 3

Reel/Frame: 026598/0177 **Recorded:** 07/15/2011 **Pages:** 12

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignor: SONICBLUE INCORPORATED **Exec Dt:** 01/15/2007

Assignee: S3 GRAPHICS CO., LTD.
CHARLES ADAMS, RITCHIE & DUCKWORTH
ZEPHYR HOUSE, MARY STREET, P.O. BOX 709
GRAND CAYMAN, BRITISH WEST INDIES, CAYMAN ISLANDS

Correspondent: DANIEL R. MCCLURE
400 INTERSTATE NORTH PKWY SE
SUITE 1500
ATLANTA, GA 30339

Exhibit 4

United States Patent and Trademark Office

Assignments on the Web > Patent Query

Patent Assignment Abstract of Title

NOTE:Results display only for issued patents and published applications. For pending or abandoned applications please consult USPTO staff.

Total Assignments: 3

Patent #: 6683978 **Issue Dt:** 01/27/2004 **Application #:** 09442114 **Filing Dt:** 11/17/1999

Inventors: KONSTANTINE I. IOURCHA, KRISHNA S. NAYAK, ZHOU HONG

Title: FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES

Assignment: 1

Reel/Frame: 026597/0407 **Recorded:** 07/15/2011 **Pages:** 4

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: IOURCHA, KONSTANTINE I. **Exec Dt:** 02/05/1998

NAYAK, KRISHNA S. **Exec Dt:** 02/03/1998

HONG, ZHOU **Exec Dt:** 02/11/1998

Assignee: S3 INCORPORATED
2801 MISSION COLLEGE BOULEVARD
SANTA CLARA, CALIFORNIA 95052

Correspondent: DANIEL R. MCCLURE
400 INTERSTATE NORTH PKWY SE
SUITE 1500
ATLANTA, GA 30339

Assignment: 2

Reel/Frame: 026598/0134 **Recorded:** 07/15/2011 **Pages:** 3

Conveyance: CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).

Assignor: S3 INCORPORATED **Exec Dt:** 11/09/2000

Assignee: SONICBLUE INCORPORATED
2841 MISSION COLLEGE BOULEVARD
SANTA CLARA, CALIFORNIA 95054

Correspondent: DANIEL R. MCCLURE
400 INTERSTATE NORTH PKWY SE
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ATLANTA, GA 30339

Assignment: 3

Reel/Frame: 026598/0177 **Recorded:** 07/15/2011 **Pages:** 12

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignor: SONICBLUE INCORPORATED **Exec Dt:** 01/15/2007

Assignee: S3 GRAPHICS CO., LTD.
CHARLES ADAMS, RITCHIE & DUCKWORTH
ZEPHYR HOUSE, MARY STREET, P.O. BOX 709
GRAND CAYMAN, BRITISH WEST INDIES, CAYMAN ISLANDS

Correspondent: DANIEL R. MCCLURE
400 INTERSTATE NORTH PKWY SE
SUITE 1500
ATLANTA, GA 30339

Search Results as of: 08/30/2011 05:22 PM

If you have any comments or questions concerning the data displayed, contact PRD / Assignments at 571-272-3350. v.2.2

Web interface last modified: July 25, 2011 v.2.2

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Konstantine I. Iourcha	02/05/1998
Krishna S. Nayak	02/03/1998
Zhou Hong	02/11/1998

RECEIVING PARTY DATA

Name:	S3 Incorporated
Street Address:	2801 Mission College Boulevard
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	95052

PROPERTY NUMBERS Total: 5

Property Type	Number
Patent Number:	6683978
Patent Number:	7043087
Patent Number:	7039244
Patent Number:	6658146
Patent Number:	6775417

OP $200.00 6683978

CORRESPONDENCE DATA

Fax Number: (770)951-0933
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 7709339500
Email: gina.silverio@tkhr.com
Correspondent Name: Daniel R. McClure
Address Line 1: 400 Interstate North Pkwy SE
Address Line 2: Suite 1500
Address Line 4: Atlanta, GEORGIA 30339

ATTORNEY DOCKET NUMBER:	252209-9010
NAME OF SUBMITTER:	Daniel R. McClure
Total Attachments: 2 source=01403552#page1.tif source=01403552#page2.tif	

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, the persons named below (referred to as "INVENTOR" whether singular or plural) have sold, assigned, and transferred and does hereby sell, assign, and transfer to S3 Incorporated, a Delaware corporation, having a place of business at 2801 Mission College Boulevard, Santa Clara, CA 95052-8058 ("ASSIGNEE"), for itself and its successors, transferees, and assignees, the following:

1. The entire worldwide right, title, and interest in all inventions and improvements ("SUBJECT MATTER") that are disclosed in the application for United States Letters Patent entitled: **"System and Method for Fixed-Rate Block-Based Image Compression With Inferred Pixel Values"** ("APPLICATION"), which:

☐ is to be filed herewith

☒ was filed on October 2, 1997, now bearing U.S. serial number 08/942,860

and for which a Declaration was executed by INVENTOR on the date(s) below; and

2. The entire worldwide right, title, and interest in and to:

(a) the APPLICATION, including any right of priority; (b) any divisional, continuation, substitute, renewal, reissue, and other related applications which have been or may be filed in the United States or elsewhere in the world; and (c) any patents which may be granted on the applications set forth in (a) and (b) above.

INVENTOR agrees that ASSIGNEE may apply for and receive patents for SUBJECT MATTER in ASSIGNEE's own name.

INVENTOR agrees to do the following, when requested, and without further consideration, in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to ASSIGNEE the rights, titles and interests herein conveyed; (2) communicate to ASSIGNEE all known facts relating to the SUBJECT MATTER; and (3) generally do all lawful acts that ASSIGNEE shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the SUBJECT MATTER and for vesting in ASSIGNEE the rights, titles, and interests herein conveyed. INVENTOR further agrees to provide any successor, assign, or legal representative of ASSIGNEE with the benefits and assistance provided to ASSIGNEE hereunder.

INVENTOR represents that INVENTOR has the rights, titles, and interests to convey as set forth herein, and covenants with ASSIGNEE that the INVENTOR has made or will make hereafter no assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed.

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original and all of which may be taken together as one and the same Assignment.

Name and Signature	Date of Signature	Date Declaration Executed By This Person
Konstantine I. Iourcha	2/5, 1998	2/5, 1998
Krishna S. Nayak	2/3, 1998	2/3, 1998
Zhou Hong	2/11, 1998	2/11, 1998

Case Docket # 3722

Title of Document: ASSIGNMENT

Re:
Title: System and Method for Fixed-Rate Block-Based Image Compression With Inferred Pixel Values
Filed: (if applicable) October 2, 1997
Serial No.: (if applicable) 08/942,860

State of California
County of Santa Clara

On February 5th 1998 [DATE] before me, Jacqueline E Ellison [NOTARY PUBLIC] personally appeared Konstantine I. Iourcha personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Jacqueline E Ellison

JACQUELINE E. ELLISON
Commission # 1088705
Notary Public — California
Santa Clara County
My Comm. Expires Feb 23, 2000

State of California
County of Santa Clara

On February 3, 1998 [DATE] before me, Jacqueline E Ellison [NOTARY PUBLIC] personally appeared Krishna S. Nayak personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Jacqueline E Ellison

JACQUELINE E. ELLISON
Commission # 1088705
Notary Public — California
Santa Clara County
My Comm. Expires Feb 23, 2000

State of California
County of Santa Clara

On February 11, 1998 [DATE] before me, Jacqueline E Ellison [NOTARY PUBLIC] personally appeared Zhou Hong personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Jacqueline E Ellison

JACQUELINE E. ELLISON
Commission # 1088705
Notary Public — California
Santa Clara County
My Comm. Expires Feb 23, 2000

Case Docket # 2733

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	CHANGE OF NAME

CONVEYING PARTY DATA

Name	Execution Date
S3 Incorporated	11/09/2000

RECEIVING PARTY DATA

Name:	Sonicblue Incorporated
Street Address:	2841 Mission College Boulevard
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 11

Property Type	Number
Application Number:	09443171
Application Number:	09708775
Application Number:	09430370
Application Number:	09430999
Application Number:	09442114
Application Number:	10857173
Application Number:	10893084
Application Number:	10893091
Application Number:	09481371
Application Number:	09351930
Application Number:	10052613

OP $440.00 09443171

CORRESPONDENCE DATA

Fax Number: (770)951-0933
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 7709339500

Email:	gina.silverio@tkhr.com
Correspondent Name:	Daniel R. McClure
Address Line 1:	400 Interstate North Pkwy SE
Address Line 2:	Suite 1500
Address Line 4:	Atlanta, GEORGIA 30339

ATTORNEY DOCKET NUMBER:	252209-9010
NAME OF SUBMITTER:	Daniel R. McClure

Total Attachments: 1
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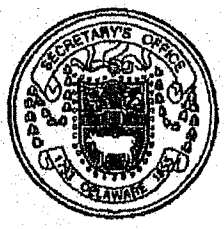
Delaware

The First State

I, HARRIET SMITH WINDSOR, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY THAT THE SAID "S3 INCORPORATED", FILED A CERTIFICATE OF OWNERSHIP, CHANGING ITS NAME TO "SONICBLUE INCORPORATED", THE NINTH DAY OF NOVEMBER, A.D. 2000, AT 4:30 O'CLOCK P.M.

AND I DO HEREBY FURTHER CERTIFY THAT THE EFFECTIVE DATE OF THE AFORESAID CERTIFICATE OF OWNERSHIP IS THE FIFTEENTH DAY OF NOVEMBER, A.D. 2000, AT 8 O'CLOCK A.M.



Harriet Smith Windsor

Harriet Smith Windsor, Secretary of State

2183836 8320

060844389

AUTHENTICATION: 5099091

DATE: 10-07-06

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Sonicblue Incorporated	01/15/2007

RECEIVING PARTY DATA

Name:	S3 Graphics Co., Ltd.
Street Address:	Charles Adams, Ritchie & Duckworth
Internal Address:	Zephyr House, Mary Street, P.O. Box 709
City:	Grand Cayman, British West Indies
State/Country:	CAYMAN ISLANDS

PROPERTY NUMBERS Total: 11

Property Type	Number
Application Number:	09443171
Application Number:	09708775
Application Number:	09430370
Application Number:	09430999
Application Number:	09442114
Application Number:	10857173
Application Number:	10893084
Application Number:	10893091
Application Number:	09481371
Application Number:	09351930
Application Number:	10052613

OP $440.00 09443171

CORRESPONDENCE DATA

Fax Number: (770)951-0933
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Email:	gina.silverio@tkhr.com
Correspondent Name:	Daniel R. McClure
Address Line 1:	400 Interstate North Pkwy SE
Address Line 2:	Suite 1500
Address Line 4:	Atlanta, GEORGIA 30339

ATTORNEY DOCKET NUMBER:	252209-9010
NAME OF SUBMITTER:	Daniel R. McClure

Total Attachments: 10
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ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS AND DISCLOSURES

WHEREAS, SONICblue Incorporated (SONICblue Inc.), a corporation organized and existing under the laws of the State of Delaware, having changed its name from S3 Incorporated (S3 Inc.) to SONICblue Incorporated ("Assignor"), and having an office and place of business at 2841 Mission College Boulevard, Santa Clara, CA 95054, is the owner of the inventions, patents, patent applications and disclosures listed in Schedule 1 annexed hereto and made a part hereof; and

WHEREAS, S3 Graphics Co., Ltd., a corporation organized and existing under the laws of the Cayman Islands, having a registered office at Charles Adams, Ritchie & Duckworth, Zephyr House, Mary Street, P.O. Box 709, Grand Cayman, British West Indies ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the inventions, patents, patent applications and disclosures listed in Schedule 1 annexed hereto, in the United States of America, and in its colonies, territories, and dependencies, and also in all countries foreign to the United States of America.

NOW, THEREFORE, TO ALL WHOM IT MAY CONCERN:

Be it known that for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the aforesaid Assignor, has sold, assigned, transferred and set over, and by these presents does hereby sell, assign, transfer and set over to said Assignee, the entire right, title and interest in and to said inventions, patents, patent applications and disclosures listed in Schedule 1, and any and all continuations, divisions and renewals of and substitutes for said applications, and in, to and under any and all Letters Patent which may be granted on or as a result thereof in the United States and any and all other countries, and any reissue or reissues or extension or extensions of said Letters Patent; and does hereby assign to and authorize said Assignee, to file applications for Letters Patent in all countries, the same to be held and enjoyed by said Assignee, its successors, assigns, nominees or legal representatives, to the full end of the term or terms for which said Letters Patent respectively may be granted, reissued or extended, as fully

and entirely as the same would have been held and enjoyed by Assignor had this assignment, sale and transfer not been made.

AND Assignor covenants to execute all additional instruments and to do all things necessary for carrying out the purpose of this instrument, at the expense of said Assignee and its successors.

AND Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States and any official of any country or countries foreign to the United States whose duty it is to issue patents on applications as aforesaid, to issue to said Assignee, as assignee of the entire right, title and interest, any and all Letters Patent for said inventions, patents, patent applications, and disclosures listed in Schedule 1, including any and all Letters Patent of the United States which may be issued and granted on or as a result of the applications aforesaid, in accordance with the terms of this assignment.

This assignment is effective November 14, 2006.

SONICblue Incorporated

Signed at San Jose, CA
This 15th day of January, 2007

By: M L
Name: Marcus Smith
Title: CFO

S3 Graphics Co., Ltd.

Signed at Fremont, CA
This 2nd day of March, 2006? JC

By: Jonathan Lou Chang
Name: JONATHAN CHANG
Title: CFO

700459035v3

Schedule 1

CR0001	PA1846US	1846	US	Method and Apparatus for Producing Perception of High Quality Grayscale Shading on Digitally Commanded Displays	1992/4/6	07/863,046	U.S. Patent No. 5,293,159	U.S. Patent No. 5,293,159	
CR0002	PA1847US	1847	US	Image Memory Controller for Controlling Multiple Memories and Method of Operation	1993/8/23	07/934,136	U.S. Patent No. 5,241,642	U.S. Patent No. 5,241,642	
CR0003	PA1848US	1848	US	Video Window Generator with Scalable Video	1994/8/27	08/206,154	U.S. Patent No. 5,402,513	U.S. Patent No. 5,402,513	
CR0004	PA1849US	1849	US	VGA Controller Circuitry	1993/1/19	08/147,486	U.S. Patent No. 5,561,276	U.S. Patent No. 5,561,276	
CR0005	PA1850US	1850	US	Video Processor Multiple Streams of Video Data in Real-Time	1994/10/20	08/326,342	U.S. Patent No. 5,440,683	U.S. Patent No. 5,440,683	
CR0005	PA1850JP	1850	JP	Digital Video Editing Processing Unit	1993/2/24	5047183	JP Patent No. 2866680	JP Patent No. 2866680	
CR0003	1836EP	1836	EP	Digital Video Editing Processing Unit				588,359	
CR0003 EP	PA1836DE	1836	DE	Digital Video Editing Processing Unit	1993/2/12	93301183.4	DE Patent No. 69321532.7	DE Patent No. 69321532.7	
CR0006	PA1851US	1851	US	Integrated Video Scaling and Sharpening Filter	1993/2/12	08/017,856	U.S. Patent No. 5,422,827	U.S. Patent No. 5,422,827	
CR0007	PA1852US	1852	US	Process for Producing Shaded Colored Images Using Dithering Techniques	1993/5/17	08/061,902	U.S. Patent No. 5,757,347	U.S. Patent No. 5,757,347	
CR0008	PA1853US	1853	US	System and Method for the Mixing of Graphics and Video Signals	1993/7/16	08/093,102	U.S. Patent No. 5,581,483	U.S. Patent No. 5,588,436	
CR0009	PA1854US	1854	US	Video Processing Apparatus, System and Methods	1993/3/3	08/102,935	U.S. Patent No. 5,625,378	U.S. Patent No. 5,625,378	
CR0010	PA1855US	1855	US	Shared Memory for Split-Panel LCD Display System	1993/3/4	08/181,770	U.S. Patent No. 5,537,128	U.S. Patent No. 5,537,128	
CR0011	PA1856US	1856	US	Variable Pixel Depth and Format for Video Windows	1994/4/28	08/223,764	U.S. Patent No. 5,608,864	U.S. Patent No. 5,608,864	
CR0011	PA1858KR	1858	KR	Variable Pixel Depth and Format for Video Windows	1995/4/28	95-700717	KR Patent No. 245306	KR Patent No. 245306	
CR0011	PA1856JP	1856	JP	Variable Pixel Depth and Format for Video Windows	1995/4/28	7-528399	JP Patent No. 3264778	JP Patent No. 3264778	
CR0011	PA1856EP	1856	EP	Variable Pixel Depth and Format for Video Windows	1995/4/28	95917184.3			
CR0012	PA1857US	1857	US	Method and Apparatus for Expanding and Centering VGA Text and Graphics	1994/4/28	08/235,427	U.S. Patent No. 5,521,614	U.S. Patent No. 5,521,614	
CR0013	PA1833US	1833	US	Video processing Apparatus System and Methods	1995/2/13	08/402,962	U.S. Patent No. 5,821,918	U.S. Patent No. 5,821,918	
CR0014	PA1859US	1859	US	Brightness Control for Liquid Crystal Displays	1995/6/7	08/474,410	U.S. Patent No. 5,734,363	U.S. Patent No. 5,734,363	
CR0015	PA1860US	1860	US	Optimized Implementation of X-Y Clipping on Pixel Boundary	1995/5/22	08/443,965	U.S. Patent No. 6,038,941	U.S. Patent No. 5,606,641	
CR0016	PA1870US	1870	US	Method and Apparatus for Upscaling Video Images in a Graphics Controller Chip	1996/3/12	08/678,870	U.S. Patent No. 6,115,507	U.S. Patent No. 6,115,507	
CR0017	PA1861US	1861	US	Method and Apparatus for Upscaling Video Images When Pixel Data Used for Upscaling a Source Video Image are Unavailable	1995/11/22	08/561,907	U.S. Patent No. 5,703,618	U.S. Patent No. 5,703,618	
CR0017	PA1861TW	1861	TW	[illegible]	1996/11/22	85114412	TW Patent No. 088278	TW Patent No. 088278	
CR0017	1861EP	1861	EP	Apparatus for Image Scaling Using Interpolation					
CR0017	1861JP	1861	JP	Method and Apparatus for Upscaling Video Images When Pixel Data Used for Upscaling a Source Video Image are Unavailable					
CR0017 EP	PA1861UK	1861	UK	Apparatus for Image Scaling Using Interpolation	1996/11/21	96308452	UK Patent No. 0775975	UK Patent No. 0775975	
CR0017 EP	PA1861NL	1861	NL	Apparatus for Image Scaling Using Interpolation	1996/11/21	96308452	NL Patent No. 0775975	NL Patent No. 0775975	
CR0017 EP	PA1861DE	1861	DE	Apparatus for Image Scaling Using Interpolation	1996/11/21	96308452	DE Patent No. 69623218.3	DE Patent No. 69623218.3	
CR0018	PA1862US	1862	US	Controller for Processing Different Pixel Data Types Stored in the Same Display Memory By Use of Tag Bits	1995/12/21	08/576,870	U.S. Patent No. 5,828,383	U.S. Patent No. 5,828,383	
CR0020	PA1789US	1789	US	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	1996/10/23	09/430,370	U.S. Patent No. 6,353,440	U.S. Patent No. 6,353,440	
CR0020	PA1863US	1863	US	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	1996/3/21	08/618,303	U.S. Patent No. 6,005,546	U.S. Patent No. 6,005,546	This same as PA1789

Initial ~~AJ~~

Schedule 1

CR0020	PA1863TW	1863	TW	[illegible]	1997/3/3	86103702	TW Patent No. 115483	TW Patent No. 115483	
CR0020	PA1863JP	1863	JP	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	1997/10/21	9-88787	JP Patent No. 3442232	JP Patent No. 3442232	
CR0020	PA1863EP	1863	EP	Hardware Assist for YUV Data Format Conversion to Software MPEG Decoder	1997/10/15	97104448.0			
CR0021	PA1864US	1864	US	Register Set Reordering for a Graphics Processor Based Upon the Type of Primitive to be Rendered	1996/8/28	08/072,630	U.S. Patent No. 5,793,386	U.S. Patent No. 5,793,386	
CR0021	PA1864TW	1864	TW	[illegible]	1997/8/3	86112820	TW Patent No. 093478	TW Patent No. 093478	
CR0021	PA1864JP	1864	JP	Register Set Reordering for a Graphics Processor Based Upon the Type of Primitive to be Rendered	1997/9/27	9-172331			
CR0021	PA1864EP	1864	EP	Register Set Reordering for a Graphics Processor Based Upon the Type of Primitive to be Rendered	1997/8/25	97306513.1			
CR0022	PA1865US	1865	US	Object Referenced Memory Mapping	1996/6/27	08/673,774	U.S. Patent No. 5,758,128	U.S. Patent No. 5,758,128	
CR0022	PA1865UK	1865	UK	Memory Mapping Method and Apparatus	1997/6/23	97304374.3	UK Patent No. 0817127	UK Patent No. 0817127	
CR0022	PA1865TW	1865	TW	[illegible]	1997/8/4	86109688	TW Patent No. 102348	TW Patent No. 102348	
CR0022	PA1865JP	1865	JP	Object Referenced Memory Mapping	1997/6/24	9-4?1090			
CR0022	PA1865IE	1865	IE	Memory Mapping Method and Apparatus	1997/6/23	97304374.3	IE Patent No. 0817127	IE Patent No. 0817127	
CR0022	PA1865FR	1865	FR	Memory Mapping Method and Apparatus	1997/6/23	97304374.3	UK Patent No. 0817127	UK Patent No. 0817127	
CR0022	PA1865DE	1865	DE	Memory Mapping Method and Apparatus	1997/6/23	97304374.3	DE Patent No. 69728[illegible]	DE Patent No. 69728[illegible]	
CR0022	1865EP	1865	EP	Memory Mapping Method and Apparatus					
CR0023	PA1866US	1866	US	Apparatus, Systems, and Methods for Controlling Data Overlay in Multimedia Data Processing and Display Systems Using Mask Techniques	1996/9/19	08/707,932	U.S. Patent No. 5,877,983	U.S. Patent No. 5,877,983	
CR0024	PA1867US	1867	US	Instruction Format for Ensuring Safe Execution of Display List	1996/9/30	08/724,838	U.S. Patent No. 5,875,295	U.S. Patent No. 5,875,295	
CR0024	PA1867TW	1867	TW	[illegible]	1997/9/30	86114238	TW Patent No. 117622	TW Patent No. 117622	
CR0025	PA1868US	1868	US	Dithering Method and Apparatus Using Ramp Probability Logic	1996/12/30	08/772,857	U.S. Patent No. 6,008,818	U.S. Patent No. 6,008,818	
CR0025	PA1868TW	1868	TW	[illegible]	1997/12/30	86120018	TW Patent No. 138137	TW Patent No. 138137	
CR0025	PA3089US	1868	US	Software-Based Dithering Method and Apparatus Using RAMP Probability Logic	1997/5/15	08/856,546	U.S. Patent No. 6,008,796	U.S. Patent No. 6,008,796	
CR0026	PA1870US	1870	US	Method for Triangle Subdivision in Computer Graphics Texture Mapping to Eliminate Artifacts in High Perspective Polygons	1997/2/20	08/803,460	U.S. Patent No. 5,841,443	U.S. Patent No. 5,841,443	
CR0027	PA1871US	1871	US	Method and Apparatus for Adjusting Graphics Processing Procedures Based on a Selectable Speed/Quality Gauge	1997/2/26	08/805,461	U.S. Patent No. 5,977,983	U.S. Patent No. 5,977,983	
CR0028	PA1872US	1872	US	Method and Apparatus for Shadowing Display List Instructions	1996/3/14	08/828,033	U.S. Patent No. 5,872,508	U.S. Patent No. 5,872,508	
CR0028	1872PCT	1872	PCT	Method and Apparatus for Shadowing Display List Instructions					
CR0029	PA1873US	1873	US	Method and Apparatus for Programming a Graphics Subsystem Register Set	1997/3/28	08/827,125	U.S. Patent No. 6,025,813	U.S. Patent No. 6,025,813	
CR0029	1873PCT	1873	PCT	Method and Apparatus for Programming a Graphics Subsystem Register Set					
CR0029 PCT	PA1873JP	1873	JP	Method and Apparatus for Programming a Graphics Subsystem Register Set	1998/3/12	2000-542818			
CR0029 PCT	PA1873EP	1873	EP	Method and Apparatus for Programming a Graphics Subsystem Register Set	1998/3/12	98921186			
CR0030	?	?	US	Method for Emulating Video Port Manager Interface					
CR0031	PA1874US	1874	US	Variable Band Size Compositing Buffer Method and Apparatus	1997/6/23	08/881,380	U.S. Patent No. 5,835,104	U.S. Patent No. 5,835,104	
CR0032	PA1875US	1875	US	Opposing Directional Fill Calculators in a Graphics Processor	1997/11/12	08/968,306	U.S. Patent No. 6,141,020	U.S. Patent No. 6,141,020	
CR0033	PA1786US	1786	US	Parallel Architecture For Graphics Primitive Decomposition	2001/5/15	09/858,354			

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Schedule 1

CX0030	[illegible]	[illegible]	US	Parallel Architecture For Graphics Primitive Decomposition					
CR0034	1997?SC	1987	US	Graphics Primitives Decomposition Using Edge Function and Recursive Tile Subdivision					
CR0034	[illegible]US	2002	US	Graphics Primitives Decomposition Using Edge Function and Recursive Tile Subdivision					
EX0026	PA1644US	1644	US	Gating and Video Queues for Multi-Processor Chip	1998/10/23	09/749,344	U.S. Patent No. 5,848,284	U.S. Patent No. 5,848,284	
EX0032	PA1838CA	1838	CA	Multiplier for Performing 3D Graphics Interpolations	1997/11/20	2272587	CA Patent No. 2,272,587	CA Patent No. 2,272,587	
EX0032	PA1838US	1838	US	Multiplier with Selectable Booth Encoders for Performing 3D Graphics Interpolations with Two Multiplies in a Single Pass Through the Multiplier	1998/11/22	08/735,545	U.S. Patent No. 5,935,198	U.S. Patent No. 5,935,198	
EX0032	PA1838DE	1838	DE	Multiplier for Performing 3D Graphics Interpolations	1997/11/20	19782?88.7			
EX0032	1838UK	1838	GB	Multiplier for Performing 3D Graphics Interpolations					
EX0032	3838JP	1838	JP	Multiplier for Performing 3D Graphics Interpolations					
B30001	PA1733US	1733	US	Open High Speed Bus for Microcomputer System	1993/1/29	08/011,448	U.S. Patent No. 5,317,828	U.S. Patent No. 5,317,828	
B30003	PA1820US	1820	US	Improved Data Retrieval From Sequential-Access Memory Devices	1993/12/10	08/165,835	U.S. Patent No. 5,418,749	U.S. Patent No. 5,418,749	
B30009	PA1674US	1834	US	Method and Apparatus for Correction of Video Tearing Associated with a Video Graphics Shared Frame Buffer, As Displayed on a Graphics Monitor	1996/4/5	08/628,764	U.S. Patent No. 5,764,240	U.S. Patent No. 5,764,240	
B38014	PA1728US	1728	US	Grayscale Shading for Liquid Crystal Display Panels	1995/8/25	08/519,880	U.S. Patent No. 5,777,598	U.S. Patent No. 5,777,598	
B30014	PA1728JP	1728	JP	Grayscale Shading for Liquid Crystal Display Panels	1996/8/23	8-510348	JP Patent No. 3141285	JP Patent No. 3141285	
B30015	PA1734US	1734	US	Decompression of MPEG Compressed Data in A Computer System	1995/8/12	08/448,488	U.S. Patent No. 5,778,856	U.S. Patent No. 5,778,856	
B30015 T	PA1735US	1735	US	Method and Apparatus for Decompression of MPEG Compressed Data in a Computer System	1995/10/3	08/536,687	U.S. Patent No. 5,774,676	U.S. Patent No. 5,774,676	
B30036	PA1728US	1726	US	Correction of Flicker Associated with Noninterlaced to Interlaced Video Conversion	1996/3/15	08/621,567	U.S. Patent No. 5,610,630	U.S. Patent No. 5,610,630	
B20016	PA1729JP	1729	JP	Correction of Flicker Associated with Noninterlaced-to-Interlaced Video Conversion	1997/2/24	9-40730			
B30017	PA1730US	1730	US	Video Decoder Engine	1995/8/17	08/515,333	U.S. Patent No. 5,818,887	U.S. Patent No. 5,818,887	
B30018	PA1734US	1734	US	Frame Reconstruction for Video Data Compression	1995/7/25	08/508,636	U.S. Patent No. 5,767,878	U.S. Patent No. 5,767,878	
B10020	PA1721US	1721	US	Multi-Function Controller and Method for a Computer Graphics Display System	2000/1/18	09/461,371	U.S. Patent No. 6,480,188	U.S. Patent No. 6,480,188	This same as PA1821
B30020 7	PA1821US	1821	US	Multi-Function Controller and Method for a Computer Graphics Display System	1998/6/7	09/094,381	U.S. Patent No. 6,052,133	U.S. Patent No. 6,052,133	
B10022	PA1822TW	1822	TW	[illegible]	1999/5/26	88107413	TW Patent No. 100111	TW Patent No. 100111	
B30022	PA1822US	1822	US	Close Captioning Processing Architecture for Providing Text Data During Multiple Fields of a Video Frame	1996/7/8	08/676,537	U.S. Patent No. 5,883,675	U.S. Patent No. 5,883,675	
B10022	PA1822JP	1822	JP	Close Captioning Processing Architecture	1997/7/8	H9-184254			
B30023	PA1823US	1823	US	Index and Storage System for Data Provided in the Vertical Blanking Interval	1996/11/25	08/753,923	U.S. Patent No. 5,914,719	U.S. Patent No. 5,914,719	
B30023	PA1823JP	1823	JP	Index and Storage System for Data Provided in the Vertical Blanking Interval	1997/12/5	19753298.9			
B30023	PA1823DE	1823	DE	Index and Storage System for Data Provided in the Vertical Blanking Interval	1997/12/6	19753298.9			
B30024	PA1737US	1737	US	Dual Image Computer Display Controller	1994/1/11	08/583,136	U.S. Patent No. 5,877,833	U.S. Patent No. 5,877,833	
B10024	PA1737TW	1737	TW	[illegible]	1998/3/12	88103336	TW Patent No. 84432	TW Patent No. 84432	
B30027	PA1826US	1826	US	Virtual Address Access to Tiled Surfaces	1997/6/27	08/884,873	U.S. Patent No. 5,990,912	U.S. Patent No. 5,990,912	
B30027	PA1826EP	1826	EP	Virtual Address Access to Tiled Surfaces	1998/6/18	98931238			
B30027	PA1826CA	1826	CA	Virtual Address Access to Tiled Surfaces	1998/6/18	2,284,884			
B30026	PA1825US	1825	US	Pixel Reordering for Improved Texture Mapping	1997/5/5	08/769,787	U.S. Patent No. 5,982,451	U.S. Patent No. 5,982,451	

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Schedule 1

830029	PA1825JP	1825	JP	Pixel Reordering for Improved Texture Mapping	1997/12/18	H10-530893			
830021	PA1825EP	1825	EP	Pixel Reordering for Improved Texture Mapping	1997/12/16	97954228.1			
830026	PA1825CA	1825	CA	Pixel Reordering for Improved Texture Mapping	1997/12/18	2275237	CA Patent No. 2,275,237	CA Patent No. 2,275,237	
830031	PA1828US	1828	US	System and Method for a Fast Carry/Save Select Adder	1997/11/27	08/788,391	U.S. Patent No. 5,852,568	5,852,568	
830031	PA1828JP	1828	JP	System and Method for a Fast Carry/Save Select Adder	1998/1/20	H10-554580	JP Patent No. 3183321		
830031	PA1828EP	1828	EP	System and Method for a Fast Carry/Save Select Adder	1998/1/20	98902913.4			
830031	PA1828CA	1828	CA	System and Method for a Fast Carry/Save Select Adder	1998/1/23	2,275,188	CA Patent No. 2,275,188	CA Patent No. 2,275,188	
830032	PA1827US	1827	US	System and Method for Simultaneous Flicker Filtering and Overscan Compensation	1997/8/28	08/942,145	U.S. Patent No. 5,936,965	U.S. Patent No. 5,936,965	
830032	PA1827JP	1827	JP	Flicker Filtering and Overscan Compensation	1998/8/28	2000-514455			
830032	PA1827EP	1827	EP	Flicker Filtering and Overscan Compensation	1998/9/29	98950891.0-2202			
830032	PA1827CA	1827	CA	Flicker Filtering and Overscan Compensation	1998/9/28	2303365		U.S. Patent No. 5,932,955	
830032	?	?	JP	System and Method for Simultaneous Flicker Filtering and Overscan Compensation				JP Patent No. 3183321	
830032	1827KR	1827	KR	Flicker Filtering and Overscan Compensation					
830033	PA1831US	1831	US	Block- and Band-Oriented Traversal in Three-Dimensional Triangle Rendering	1997/8/28	08/923,538	U.S. Patent No. 5,945,997	U.S. Patent No. 5,945,997	
830033	PA1831JP	1831	JP	Block- and Band-Oriented Traversal in Three-Dimensional Triangle Rendering	1998/8/18	H11-505057			
830033	PA1831CA	1831	CA	Block- and Band-Oriented Traversal in Three-Dimensional Triangle Rendering	1998/8/18	2294323			
830033	1831PCT	1831	PCT	Block- and Band-Oriented Traversal in Three-Dimensional Triangle Rendering					
830033 PCT	PA1831EP	1831	EP	Block- and Band-Oriented Traversal in Three-Dimensional Triangle Rendering	1998/8/18	98931505.8			
830034	PA1830US	1830	US	System and Methods for 2-Tap and 3-Tap Flicker Filtering of Non-Interlaced Computer Graphics to Interlaced Lines for Television Display	1997/11/13	08/969,837	U.S. Patent No. 6,084,568	U.S. Patent No. 6,084,568	
830034	PA1830JP	1830	JP	System and Method for 2-Tap/3-Tap Flicker Filtering	1998/11/12	2000-521610			
830034	PA1830EP	1830	EP	System and Method for 2-Tap/3-Tap Flicker Filtering	1998/11/12	98958543.7			
830034	PA1830CA	1830	CA	System and Method for 2-Tap/3-Tap Flicker Filtering	1998/11/12	2309908			
830035 ?	PA2473US	2473	US	Based Image Compression with Inferred Pixel Values	1999/11/17	09/442,114	U.S. Patent No. 6,683,978	U.S. Patent No. 6,683,978	
830035	PA1730US	1730	US	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	1997/10/2	08/942,860	U.S. Patent No. 5,956,431	U.S. Patent No. 5,956,431	
830035	PA1730KR	1730	KR	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	1998/9/29	7003814/2000			
830035	PA1731US	1731	US	Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	1999/7/12	09/351,930	U.S. Patent No. 6,658,146	U.S. Patent No. 6,658,146	
830035	PA1732US	1732	US	System and Method For Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	2002/1/17	10/052,613	U.S. Patent No. 6,775,417	U.S. Patent No. 6,775,417	
830035	?	?	US	System and Method for Fixed-Rate Block-Based Image 3-D Compression with Inferred Pixel Values					
830035	1730PCT	?	PCT	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values					
830035 PCT	PA1730JP	1730	JP	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	1998/9/28	2000-515252			

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Schedule I

830035 PCT	PA1730IL	1730	IL	Based Image Compression with Inferred Pixel Values	1998/6/26	125382	IL Patent No. 125382	IL Patent No. 125382	
830035 PCT	PA1730HK	1730	HK	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	2001/10/23	1101814.1			
830035 PCT	PA1730EP	1730	EP	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	1998/6/15	98914057.9			
830035 PCT	PA1730CA	1730	CA	System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values	1998/6/26	2283472			
830037	PA1828EP	1828	EP	Integrated DRAM with High Speed Interleaving	1998/8/25	98943365.9-2212			
830037	PA1828US	1828	US	Integrated DRAM with High Speed Interleaving	1997/8/27	08/920,904	U.S. Patent No. 5,856,947	U.S. Patent No. 5,856,947	
830037	PA1828TW	1828	TW	[illegible]	1998/8/24	87114218	TW Patent No. 120183	TW Patent No. 120183	
830037	PA1828KR	1828	KR	Integrated DRAM with High Speed Interleaving	1998/8/25	10-2000-7002103			
830037	PA1828CA	1828	CA	Integrated DRAM with High Speed Interleaving	1998/8/26	2,302,913			
830037	1828PCT	1828	PCT	Integrated DRAM with High Speed Interleaving					
830037 PCT	PA1828JP	1828	JP	Integrated DRAM with High Speed Interleaving	1998/8/25	2000-508045			
830044	PA1774US	1774	US	System and Method for Rasterizing Primitives using Direct Interpolation	1999/3/18	09/271,872			
830045	PA1832US	1832	US	Hi DC Current and Stagger Power/Ground Pad	1996/4/6	09/630,281			
830047	PA1835US	1835	US	System and Method for a Self-Adjusting Data Strobe	1997/10/24	08/941,402	U.S. Patent No. 6,031,298	U.S. Patent No. 6,031,298	
830048	PA1834UK	1834	UK	Computer Processor and Method for Data Streaming	1996/11/6	96939831	UK Patent No. 1027841	UK Patent No. 1027841	
830048	PA1834DE	1834	DE	Computer Processor and Method for Data Streaming	1996/11/6	96939831	DE Patent No. 69624032.4	DE Patent No. 69624032.4	
830048	PA1834US	1834	US	Computer Processor and Method for Data Streaming	1997/11/07	08/968,904	U.S. Patent No. 5,898,032	U.S. Patent No. 5,898,032	
830048	PA1834JP	1834	JP	Computer Processor and Method for Data Streaming	1996/11/6	2000-518831			
830048	PA1834CA	1834	CA	Computer Processor and Method for Data Streaming	1996/11/6	2264772			
830049	PA1769US	1769	US	Apparatus and Method for Texture Mapping	1999/3/12	09/273,814	U.S. Patent No. 6,373,496	U.S. Patent No. 6,373,496	
830049	1769DSC	1769	US	Efficient X, Y Based Level of Detail Scheme for Mipmapped Texturing					
830050	PA1722EP	1722	EP	Trilinear Texture Filter with Optimized Memory Access	2000/5/19	00931103.9			
830050	1722PCT	1722	PCT	Trilinear Texture Filter with Optimized Memory Access					
830050	PA1773US	1773	US	Trilinear Texture Filtering of Two Levels of Detail Based on a Single Level of Detail	1999/11/18	09/758,941	U.S. Patent No. 6,304,268	U.S. Patent No. 6,304,268	
830050	?	?	US	Trilinear Texture Filter with Optimized Memory Access					
830051	PA1877US	1877	US	Double Buffered Graphics and Video Accelerator Having a Write Blocking Memory Interface and Method of Doing the Same	1998/7/24	09/122,472	U.S. Patent No. 6,128,026	U.S. Patent No. 6,128,026	
830051	1877DSC	1877	US	Double Buffered Graphics and Video Accelerator Having a Write Blocking Memory Interface and Method of Doing the Same					
830051	1877PCT	1877	PCT	Double Buffered Graphics and Video Accelerator Having a Write Blocking Memory Interface and Method of Doing the Same					
830051 PCT	PA1877JP	1877	JP	Double Buffered Graphics and Video Accelerator Having a Write Blocking Memory Interface and Method of Doing the Same	1999/5/3	2000-547551			

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Schedule 1

830051 PCT	PA1977EP	1977	EP	Double Buffered Graphics and Video Accelerator Having a Write Blocking Memory Interface and Method of Doing the Same	1998/[illegible]	98922778.8			
830052	1728UK	1728	UK	Communicating the Status of a Peripheral Device Controller to a Host Processor					
830052	1728PCT	1728	PCT	Communicating the Status of a Peripheral Device Controller to a Host Processor					
830052	?	?	US	Computer System and Method for Efficiently Communicating Peripheral Device Status					
830052 PCT	PA1728EP	1728	EP	Communicating the Status of a Peripheral Device Controller to a Host Processor	2001/02/[illegible]	99142081.3			
830053	PA1778US	1778	US	Device and method for Blending True Colors and Fog Colors to Generate Display Colors	1999/[illegible]	09/360,181	U.S. Patent No. 6,417,862	U.S. Patent No. 6,417,862	
830053	1778PCT	1778	US	Device & Method for Blending True Colors & Fog Colors to Generate Display Colors					
830057	PA1746US	1746	US	System and Method for Mapping Textures onto Surfaces of Computer-Generated Objects	2000/11/7	09/708,797			
830057	PA1747US	1747	US	System and Method for Mapping Textures Onto Surfaces of Computer-Generated Objects	2000/11/11	09/709,773	U.S. Patent No. 6,837,250	U.S. Patent No. 6,837,290	
830057	PA1765US	1765	US	System and Method for Mapping Textures Onto Surfaces of Computer-Generated Objects	1997/8/27	08/924,944	U.S. Patent No. 6,236,405	U.S. Patent No. 6,236,405	
830058	?	?	US	Out of Order Dispatch Unit for Graphics Primitives					
830060	PA1835US	1835	US	Real Time DRAM Eliminating a Performance Penalty for Crossing a Page Boundary	1998/2/5	09/019,346	U.S. Patent No. 6,009,018	U.S. Patent No. 6,009,018	
830060	1835PCT	1835	PCT	Real time DRAM Page Boundary Adjustment					
830061	PA1718US	1718	US	System and Method for Copy Protecting Computer Graphics	1998/5/22	09/083,823	U.S. Patent No. 6,345,888	U.S. Patent No. 6,345,888	
830064	PA1837US	1837	US	Adaptive Dynamic Aperture Correction	1998/4/17	09/061,725	U.S. Patent No. 6,172,736	U.S. Patent No. 6,172,716	
830065	PA1836US	1836	US	Flat-Panel Display Controller with Improved Dithering and Frame Rate Control	1998/2/10	09/021,718	U.S. Patent No. 6,008,794	U.S. Patent No. 6,008,794	
830066	PA1838US	1838	US	Programmable Delay Timing Calibrator for High Speed Data Interface	1997/5/27	09/093,964	U.S. Patent No. 6,041,419	U.S. Patent No. 6,041,419	
830066	PA1838CA	1838	CA	Programmable Delay Timing Calibrator for High Speed Data Interface	1998/5/24	2239141			
830071	PA1840US	1840	US	AGP/DDR Interfaces for Full Swing and Reduced Swing (SSTL) Signals on an Integrated Circuit Chip	[illegible]	09/057,047	U.S. Patent No. 6,093,412	U.S. Patent No. 6,083,412	
830071	PA1840KR	1840	KR	Reduced Swing (SSTL) Signals on an Integrated Circuit Chip	1999/3/18	10-1999-7011515			
830071	PA1840JP	1840	JP	Reduced Swing (SSTL) Signals on an Integrated Circuit Chip	1999/3/18	H11-550186			
830071	1840PCT	1840	PCT	AGP/DDR Interfaces for Full Swing and Reduced Swing (SSTL) Signals on an Integrated Circuit Chip					
830072	PA1841US	1841	US	Non-Stalled Requesting Texture Cache System and Method	1998/4/3	09/057,828	U.S. Patent No. 6,011,565	U.S. Patent No. 6,011,565	
830072	PA1841JP	1841	JP	Non-Stalled Requesting Texture Cache System and Method	1999/3/4	H11-551062			
830072	PA1841EP	1841	EP	Non-Stalled Requesting Texture Cache System and Method	1999/3/4	99711171.8	EP Patent No. 0986799	EP Patent No. 0986799	
830072	PA1841CA	1841	CA	Non-Stalled Requesting Texture Cache System and Method	1999/3/4	2,283,634			
830072 EP	PA1841UK	1841	UK	Non-Stalled Requesting Texture Cache System and Method	1999/3/4	99 911 111.5	UK Patent No. 0986799	UK Patent No. 0986799	
830072 EP	PA1841DE	1841	DE	Non-Stalled Requesting Texture Cache System and Method	1999/3/4	99 911 111.5	DE Patent No. 69918022	DE Patent No. 69918022	
830073	PA1842US	1842	US	System and Method for Performing Dithering with a Graphics Unit Having an Oversampling Buffer	1998/5/14	09/079,873	U.S. Patent No. 6,154,195	U.S. Patent No. 6,154,195	
830074	PA1843US	1843	US	System and Method for Performing Blending Using an Oversampling Buffer	1998/4/16	09/060,823	U.S. Patent No. 6,144,365	U.S. Patent No. 6,144,365	

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Schedule 1

[illegible]	PA1709US	1709	US	Command Interpretation System and Method	2000/1/27	09/492,907	U.S. Patent No. 6,623,083	U.S. Patent No. 6,623,083	
830075	7	7	US	A Device to Control Two Synchronous Command Streams					
830082	PA1718US	1718	US	State Parser for a Multi-Stage Graphics Pipeline					
[illegible]	1704US	1704	US	An Improved Self Burn-in Apparatus and Method for Semiconductor Devices	1998/4/4	09/128,923	U.S. Patent No. 6,268,474	U.S. Patent No. 6,268,474	
830085	PA1744EP	1744	EP	Graphical Image System and Apparatus					
830085	PA1744US	1744	US	Area and Span Based Z-Buffer	2001/3/20	[illegible]			
830085	1744DIVC	1744	US	Span-Based Z-Buffer	2001/3/20	[illegible]			
830085	1744UR	1744	US	Span-Based Z-Buffer					
830087	PA1770US	1770	US	Removal of Interpolation Artifacts in a Non-Interlaced Video System					
830056	PA1706US	1706	US	Z-Buffer Based Interpenetrating Object Detection for Antialiasing	1998/3/3	09/128,357	U.S. Patent No. 6,297,847	U.S. Patent No. 6,297,847	
830089	PA2783US	2783	US	Z-Buffer Based Interpenetrating Object Detection For Antialiasing	1999/1/17	09/111,482	U.S. Patent No. 6,780,025	U.S. Patent No. 6,780,025	
830089	PA1706US	1706	US	Method and Apparatus for Interpolation, Adaptive Illumination in 3D Graphics	2004/3/26	10/938,882			
[illegible]	PA1745US	1745	US	System and Method for Software Capture of Video Frames	[illegible]	09/132,880	U.S. Patent No. 6,259,454	U.S. Patent No. 6,259,454	
830090	PA1643US	1646	US	Enhancement of Non-Deterministically Arriving Interlaced Video Data	1999/11/16	09/443,171	U.S. Patent No. 6,317,165		
[illegible]	1771US	1771	US	Image Blending with Color Key Edge Removal in Bitmaps	1998/7/26	09/122,117	U.S. Patent No. 6,034,733	U.S. Patent No. 6,034,733	
830097	PA1783US	1783	US	Apparatus and Method for Gray-Scale and Brightness Display Control					
830096	PA1785KR	1785	KR	Capacitance and/or Inductance in an Integrated Circuit	1999/10/7	09/187,966	U.S. Patent No. 6,284,989	U.S. Patent No. 6,284,989	
830096	PA1705US	1705	US	Capacitance and/or Inductance of an Integrated Circuit	2001/2/15	2001-7007786			
830098	PA1785TW	1785	TW	[illegible]	1998/8/11	09/230,744	U.S. Patent No. 6,281,305	U.S. Patent No. 6,281,305	
830099	PA1719US	1719	US	Apparatus and Method for Z-Buffer Compression	2000/6/7	89111344	TW Patent No. 060887	TW Patent No. 060887	
830400	PA1725US	1725	US	Command Reordering for Out of Order Bus Transfer	1999/11/22	09/453,596	U.S. Patent No. 6,411,295	U.S. Patent No. 6,411,295	
830100	1725PCT	1725	PCT	Command Reordering for Out of Order Bus Transfer	1999/1/22	09/236,082	U.S. Patent No. 6,405,267	U.S. Patent No. 6,405,267	
830101	PA1785US	1785	US	Fast and Cheap Correct Resolution Conversion for Digital Numbers					
830102	1707RV	1707	US	Optimized Illumination Computation	2001/3/16	09/860,417	U.S. Patent No. 6,707,460	U.S. Patent No. 6,707,460	
830103	1856DIVC	1856	US	Logarithm-Based Level-of-Detail Computation					
830104	1857DIVC	1857	US	Logarithm-Based Level-of-Detail Computation					
830105	PA2813US	2813	US	System and Method for Shadow Rendering	2004/3/24	10/723,448			
830105	PA1711US	1711	US	Shadow Rendering System and Method	2000/6/18	[illegible]	U.S. Patent No. 6,731,544	U.S. Patent No. 6,731,544	
830105	1711DIVC	1711	US	One Pass Shadow Algorithm for Hardware Graphics					
830108	PA1712US	1712	US	System for Low Miss Rate Replacement of Texture Cache Lines	2000/6/15	09/864,983	U.S. Patent No. 6,580,578	U.S. Patent No. 6,580,578	
830109	PA1715US	1715	US	System and Method for Implementing a Two-Layer Z-Range Buffer	1999/3/16	09/313,857	U.S. Patent No. 6,473,082	U.S. Patent No. 6,473,082	
830109	1715PCT	1715	PCT	System and Method for Implementing a Two-Layer Z-Range Buffer					
830109 PCT	PA1715EP	1715	EP	System and Method for Implementing a Two-Layer Z-Range Buffer	2001/7/31	922385			
[illegible]	1775US	1775	US	Parameterized Method for De-Interlacing System					
830111	PA1779US	1779	US	Multichip Module Packaging Process for Known Good Die Burn-in	1999/9/1	09/763,967	U.S. Patent No. 6,351,895	U.S. Patent No. 6,351,895	
830111	PA1779TW	1779	TW	[illegible]	2000/9/1	89117818	TW Patent No. 148458	TW Patent No. 159958	
830111	PA1779KR	1779	KR	Multichip Module Packaging Process for Known Good Die Burn-in	2000/9/1	10-2000-61513			
830111	PA1779JP	1779	JP	Multichip Module Packaging Process for Known Good Die Burn-in	2000/9/1	2000-264997			

Initial MJ

Schedule 1

830111	PA1778EP	1778	EP	Multichip Packaging Process for Known Good Die Burn-in	2000/9/9	[illegible]			
830112	1777US	1777	US	Direct Evaluation of Multi-Pixel Multi-Texture Rendering					
830113	PA1714TW	1714	TW	[illegible]	2000/10/31	89122933	TW Patent No. 178504	TW Patent No. 178504	
830113	PA1714US	1714	US	Multi-Stage Fixed Cycle Pipe-Lined Lighting Equation Evaluator	2000/10/16	09/691,644	U.S. Patent No. 6,611,265	U.S. Patent No. 6,611,265	
830113	1714PCT	1714	PCT	Multi-Stage Fixed Cycle Pipe-Lined Lighting Equation Evaluator					
830114	PA1770US	1770	US	Token-Based Buffer System and method for a Geometry Pipeline in Three Dimensional Graphics	1999/10/14	09/419,866	U.S. Patent No. 6,476,808	U.S. Patent No. 6,476,808	
830115	PA1713US	1713	US	Mode Transfer Data Storage Access Environment	1999/9/16	09/[illegible]	U.S. Patent No. 6,799,[illegible]	U.S. Patent No. 6,799,[illegible]	This same as PA2774US
830115	1713PCT	1713	PCT	Mode Transfer Data Storage Access Environment					
830115	PA2774US	2774	US	Non Flushing Atomic Operation in a Burst Mode Transfer Data Storage Access Environment	2004/5/26	10/857,139			
830116	PA1752US	1752	US	Macroblock Tiling Format for Motion Compensation	2000/6/26	09/604,550	U.S. Patent No. 6,614,442	U.S. Patent No. 6,614,442	
830116	PA1743US	1743	US	Fetching Pixel Data with Reduced Memory Bandwidth	2001/7/6	09/901,[illegible]			
830117	PA1706US	1706	US	Method of and Apparatus for Managing Cache Data	1999/11/2	09/432,881			
830117	1706DSC	1706	US	Method & Apparatus for Managing Cache Data					
830118	PA1728US	1728	US	Synchronized Two-Level Graphics Processing Cache	1999/9/17	09/398,380	U.S. Patent No. 6,825,848	U.S. Patent No. 6,825,848	
830118	1728PCT	1728	PCT	Synchronized Two-Level Graphics Processing Cache					
830118	PA2848US	2848	US	Synchronized Two-Level Graphics Processing Cache	2004/10/18	10/968,346			
830119	PA1727US	1727	US	Dynamic Allocation of Texture Cache Memory	1999/9/17	09/399,280	U.S. Patent No. 6,750,872	U.S. Patent No. 6,750,872	This same as PA2773US
830119	1727DSC	1727	US	A Multi-Stage Fixed Cycle Pipelined Lighting Equation Evaluator					
830119	1727PCT	1727	PCT	Dynamic Allocation of Texture Cache Memory					
830119	PA2773US	2773	US	Dynamic Allocation Of Texture Cache Memory	2004/5/28	10/857,273			
830120	PA1743US	1743	US	Selective Super-Sampling/Adaptive Anti-Aliasing of Complex 3D Data	2000/5/12; 2001/8/14	09/704,215; 09/835,360	U.S. Patent No. 6,828,983	U.S. Patent No. 6,828,983	
830121	PA1742US	1742	US	Matched Texture Filter Design for Rendering Multi-Rate Data Samples	2001/5/14	09/855,322	U.S. Patent No. 6,780,281	U.S. Patent No. 6,780,281	
[illegible]	1999DSC		US	Multiple Hardware Overlay System for a Computer Display					
Nov 7	PA1781US	1781	US	Flat-Panel Controller with Improved Dithering and Frame Rate Control	1999/11/1	09/[illegible]	U.S. Patent No. 6,362,834	U.S. Patent No. 6,362,834	
	PA2772US	2772	US	Method Texture Filtering Design for Rendering Multi-Rate Data Samples	2004/5/28	10/855,858			
	PA2788US	2788	US	Image Processing System	2004/7/15	10/893,064			
	PA2891US	2891	US	Fixed-Rate Block-Based Image Compression	2004/7/16	10/893,081			
Nov 7	PA2845US	2845	US	Selective Super-Sampling/Adaptive Anti-Aliasing of Complex 3D Data	2004/10/14	10/966,832			

Initial MJ

Exhibit 5

Patent Assignment Abstract of Title

NOTE:Results display only for issued patents and published applications. For pending or abandoned applications please consult USPTO staff.

Total Assignments: 3

Patent #: 6775417 **Issue Dt:** 08/10/2004 **Application #:** 10052613 **Filing Dt:** 01/17/2002

Publication #: 20030053706 **Pub Dt:** 03/20/2003

Inventors: Zhou Hong, Konstantine I Iourcha, Krishna S. Nayak

Title: FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES

Assignment: 1

Reel/Frame: 026597/0407 **Recorded:** 07/15/2011 **Pages:** 4

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: IOURCHA, KONSTANTINE I. **Exec Dt:** 02/05/1998

NAYAK, KRISHNA S. **Exec Dt:** 02/03/1998

HONG, ZHOU **Exec Dt:** 02/11/1998

Assignee: S3 INCORPORATED
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SANTA CLARA, CALIFORNIA 95052

Correspondent: DANIEL R. MCCLURE
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Assignment: 2

Reel/Frame: 026598/0134 **Recorded:** 07/15/2011 **Pages:** 3

Conveyance: CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).

Assignor: S3 INCORPORATED **Exec Dt:** 11/09/2000

Assignee: SONICBLUE INCORPORATED
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SANTA CLARA, CALIFORNIA 95054

Correspondent: DANIEL R. MCCLURE
400 INTERSTATE NORTH PKWY SE
SUITE 1500
ATLANTA, GA 30339

Assignment: 3

Reel/Frame: 026598/0177 **Recorded:** 07/15/2011 **Pages:** 12

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignor: SONICBLUE INCORPORATED **Exec Dt:** 01/15/2007

Assignee: S3 GRAPHICS CO., LTD.
CHARLES ADAMS, RITCHIE & DUCKWORTH
ZEPHYR HOUSE, MARY STREET, P.O. BOX 709
GRAND CAYMAN, BRITISH WEST INDIES, CAYMAN ISLANDS

Correspondent: DANIEL R. MCCLURE
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SUITE 1500
ATLANTA, GA 30339

Exhibit 6

Patent Assignment Abstract of Title

NOTE:Results display only for issued patents and published applications. For pending or abandoned applications please consult USPTO staff.

Total Assignments: 3

Patent #: 7043087 **Issue Dt:** 05/09/2006 **Application #:** 10893084 **Filing Dt:** 07/16/2004

Publication #: 20040258321 **Pub Dt:** 12/23/2004

Inventors: Zhou Hong, Konstantine I. Iourcha, Krishna S. Nayak

Title: IMAGE PROCESSING SYSTEM

Assignment: 1

Reel/Frame: 026597/0407 **Recorded:** 07/15/2011 **Pages:** 4

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: IOURCHA, KONSTANTINE I. **Exec Dt:** 02/05/1998

NAYAK, KRISHNA S. **Exec Dt:** 02/03/1998

HONG, ZHOU **Exec Dt:** 02/11/1998

Assignee: S3 INCORPORATED
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ATLANTA, GA 30339

Assignment: 2

Reel/Frame: 026598/0134 **Recorded:** 07/15/2011 **Pages:** 3

Conveyance: CHANGE OF NAME (SEE DOCUMENT FOR DETAILS).

Assignor: S3 INCORPORATED **Exec Dt:** 11/09/2000

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ATLANTA, GA 30339

Assignment: 3

Reel/Frame: 026598/0177 **Recorded:** 07/15/2011 **Pages:** 12

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignor: SONICBLUE INCORPORATED **Exec Dt:** 01/15/2007

Assignee: S3 GRAPHICS CO., LTD.
CHARLES ADAMS, RITCHIE & DUCKWORTH
ZEPHYR HOUSE, MARY STREET, P.O. BOX 709
GRAND CAYMAN, BRITISH WEST INDIES, CAYMAN ISLANDS

Correspondent: DANIEL R. MCCLURE
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ENTIRE EXHIBIT NOT SUSCEPTIBLE TO PUBLIC SUMMARY

Exhibit 8

US006658146B1

(12) **United States Patent**
Iourcha et al.

(10) **Patent No.: US 6,658,146 B1**
(45) **Date of Patent: *Dec. 2, 2003**

(54) **FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES**

(75) Inventors: **Konstantine I. Iourcha**, San Jose, CA (US); **Krishna S. Nayak**, Stanford, CA (US); **Zhou Hong**, San Jose, CA (US)

(73) Assignee: **S3 Graphics Co., Ltd.**, Grand Cayman (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/351,930**

(22) Filed: **Jul. 12, 1999**

Related U.S. Application Data

(63) Continuation of application No. 08/942,850, filed on Oct. 2, 1997, now Pat. No. 5,956,431.

(51) **Int. Cl.**[7] **G06K 9/00**
(52) **U.S. Cl.** **382/166**; 382/162; 382/232
(58) **Field of Search** 382/232, 253, 382/239, 236, 166, 162, 272; 345/593; 341/106; 358/1.9, 500

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,821,208 A * 4/1989 Ryan et al. 364/158

FOREIGN PATENT DOCUMENTS

JP 405216993 A * 8/1993 ..... G06F/15/70

OTHER PUBLICATIONS

Feng et al., "A Dynamic Address Vector Quantization Algorithm Based on Inter–Block and Inter–Color Correction for Color image Coding", IEEE International Conference on Acoustics, Speech, and Signal Processing, vol. 3, May 1989, pps. 1755–1758.*

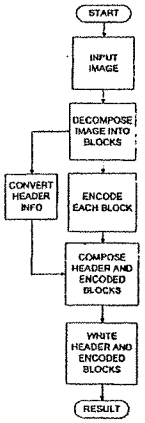
(List continued on next page.)

Primary Examiner—Anh Hong Do
(74) *Attorney, Agent, or Firm*—Carr & Ferrell LLP

(57) **ABSTRACT**

An image processing system includes an image encoder system and a image decoder system that are coupled together. The image encoder system includes a block decomposer and a block encoder that are coupled together. The block encoder includes a color quantizer and a bitmap construction module. The block decomposer breaks an original image into blocks. Each block is then processed by the block encoder. Specifically, the color quantizer selects some number of base points, or codewords, that serve as reference pixel values, such as colors, from which quantized pixel values are derived. The bitmap construction module then maps each pixel colors to one of the derived quantized colors. The codewords and bitmap are output as encoded image blocks. The decoder system includes a block decoder. The block decoder includes a block type detector, one or more decoder units, and an output selector. Using the codewords of the encoded data blocks, the comparator and the decoder units determine the quantized colors for the encoded image block and map each pixel to one of the quantized colors. The output selector outputs the appropriate color, which is ordered in an image composer with the other decoded blocks to output an image representative of the original image. A method for encoding an original image and for decoding the encoded image to generate a representation of the original image is also disclosed.

22 Claims, 16 Drawing Sheets



U.S. PATENT DOCUMENTS

4,887,151	A	*	12/1989	Wataya	358/539
5,734,744	A		3/1998	Wittenstein et al.	382/166
5,748,904	A	*	5/1998	Huang et al.	345/544
5,787,192	A	*	7/1998	Takaichi et al.	382/166
5,822,465	A		10/1998	Normile et al.	382/253
5,956,425	A	*	9/1999	Yoshida	382/234
5,956,431	A	*	9/1999	Iourcha et al.	382/253
6,075,619	A	*	6/2000	Iizuka	358/432

OTHER PUBLICATIONS

A. Schilling, et al.; "Texram: A Smart Memory for Texturing"; IEEE Computer Graphics & Applications; May 1996; 16(3) pp. 9–19.

G. Knittel, et al.; "Hardware and Software for Superior Texture Performance"; In 10; Eurographics Hardware Workshop '95; Maastricht, NL; Aug. 28–29, 1995; pp. 1–8.

G. Campbell, et al.; "Two Bit/Pixel Full Color Encoding"; Computer Graphics, (Proc. Siggraph '86); Aug. 18–22, 1986; vol. 20, No. 4, Dallas TX; pp. 215–219.

* cited by examiner

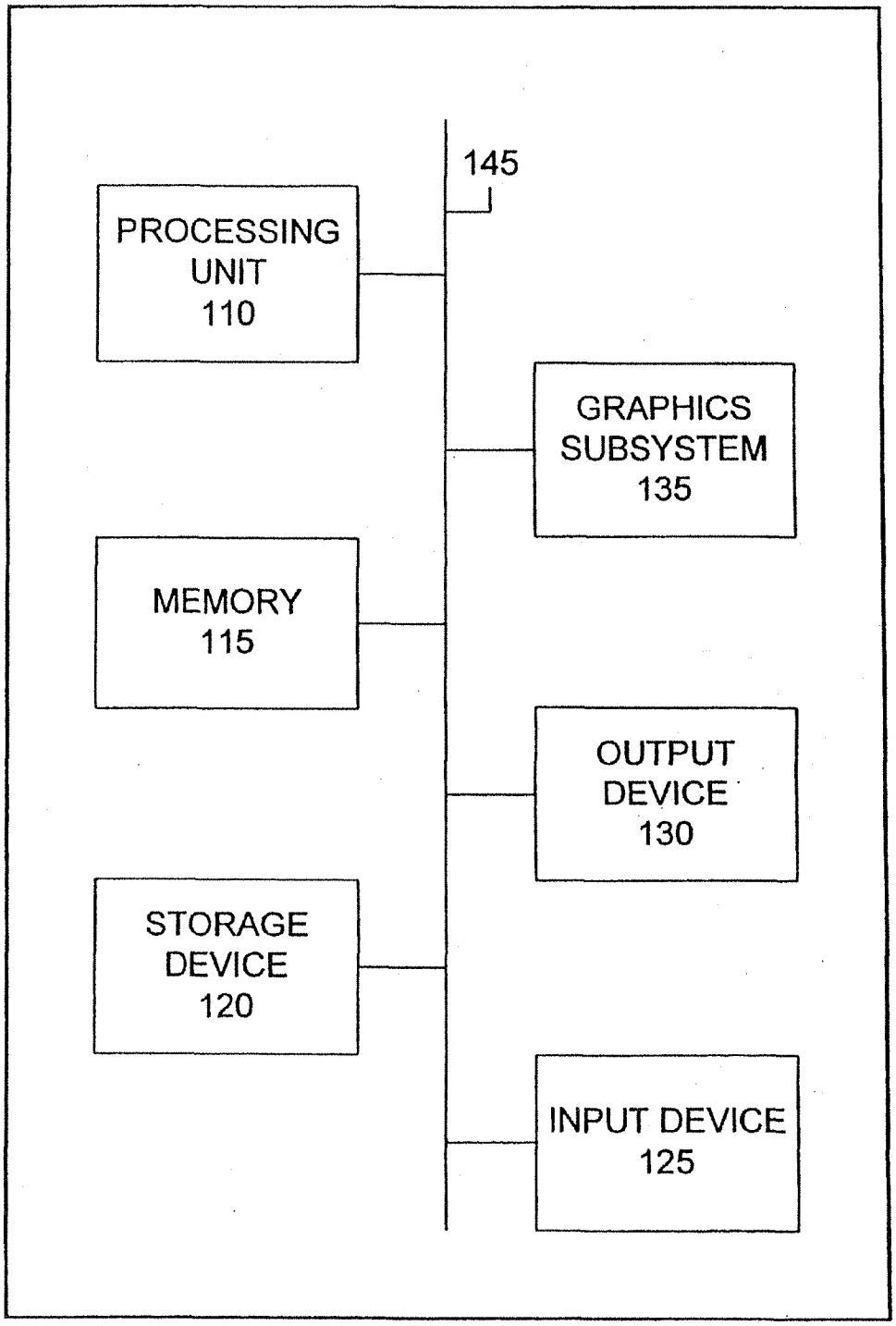

145
PROCESSING UNIT 110
GRAPHICS SUBSYSTEM 135
MEMORY 115
OUTPUT DEVICE 130
STORAGE DEVICE 120
INPUT DEVICE 125

FIG. 1 105

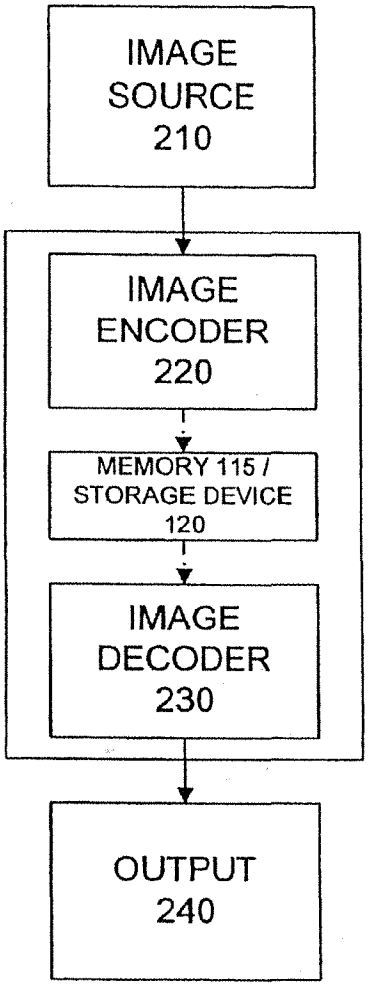


IMAGE SOURCE 210
IMAGE ENCODER 220
MEMORY 115 / STORAGE DEVICE 120
IMAGE DECODER 230
OUTPUT 240
205

FIG. 2A

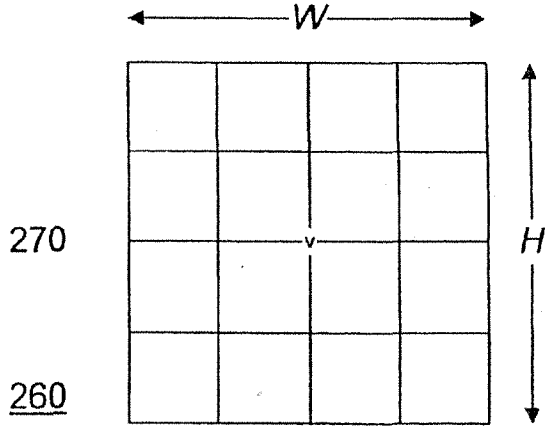

W
H
270
260

FIG. 2B

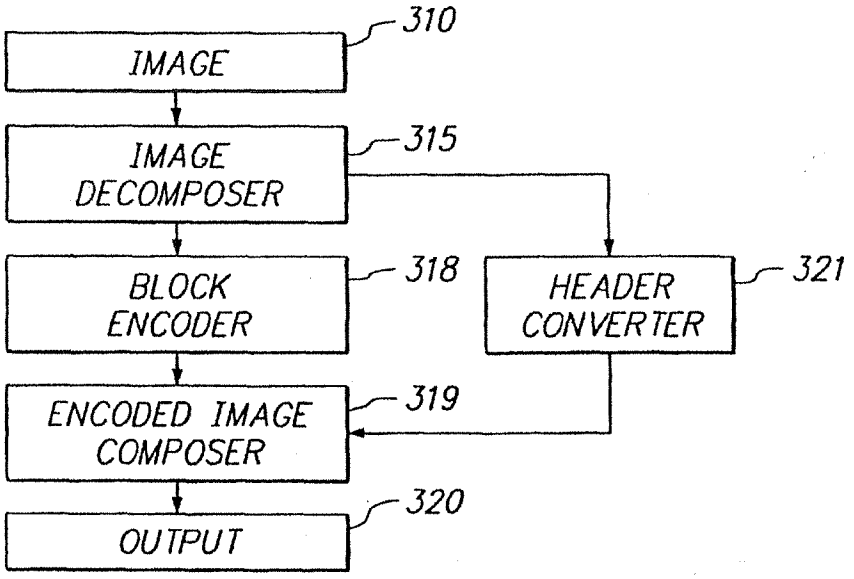


IMAGE
310
IMAGE DECOMPOSER
315
BLOCK ENCODER
318
HEADER CONVERTER
321
ENCODED IMAGE COMPOSER
319
OUTPUT
320
220

FIG. 3A

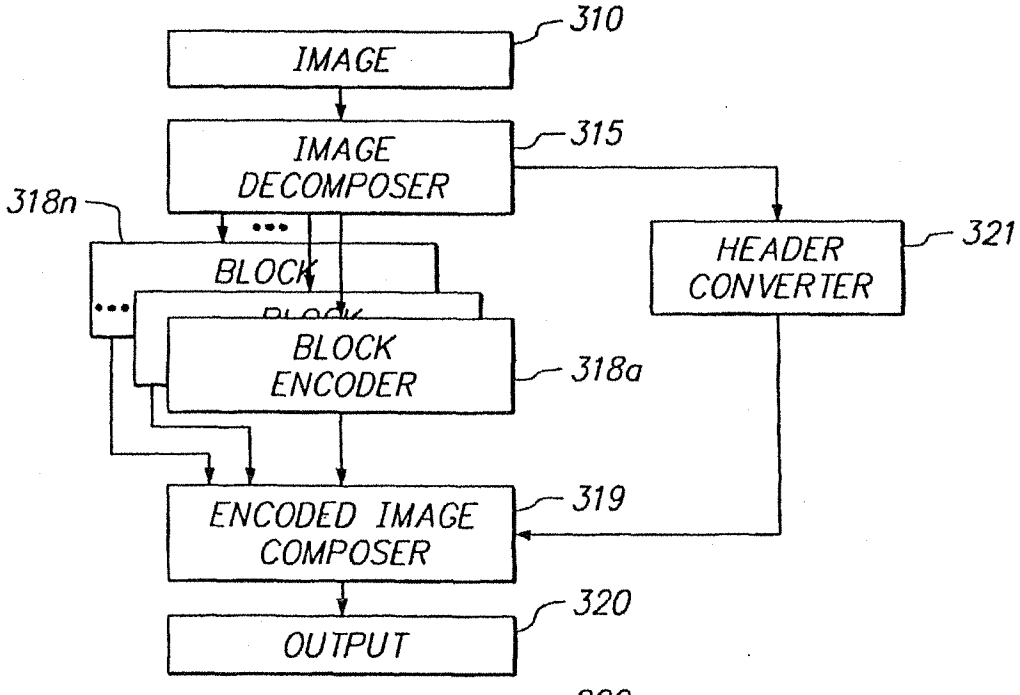


IMAGE
310
IMAGE DECOMPOSER
315
318n
BLOCK
HEADER CONVERTER
321
BLOCK ENCODER
318a
ENCODED IMAGE COMPOSER
319
OUTPUT
320
220

FIG. 3B

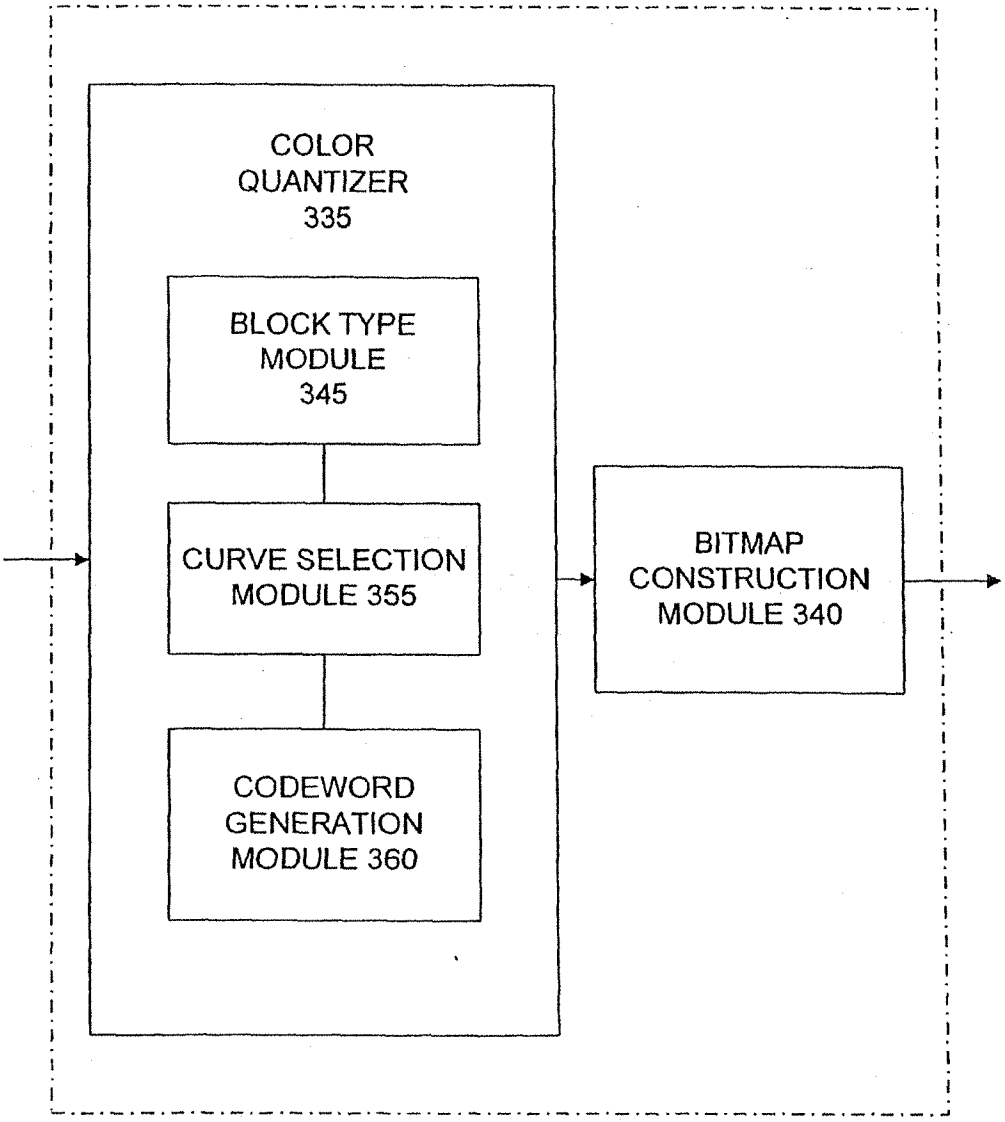

COLOR
QUANTIZER
335
BLOCK TYPE
MODULE
345
CURVE SELECTION
MODULE 355
CODEWORD
GENERATION
MODULE 360
BITMAP
CONSTRUCTION
MODULE 340
318

FIG. 3C

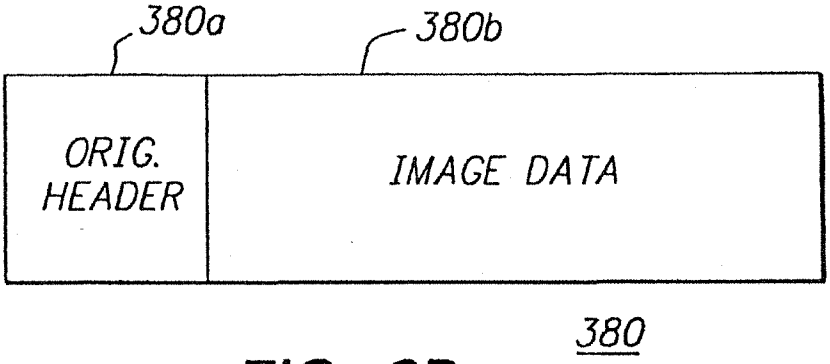


FIG. 3D

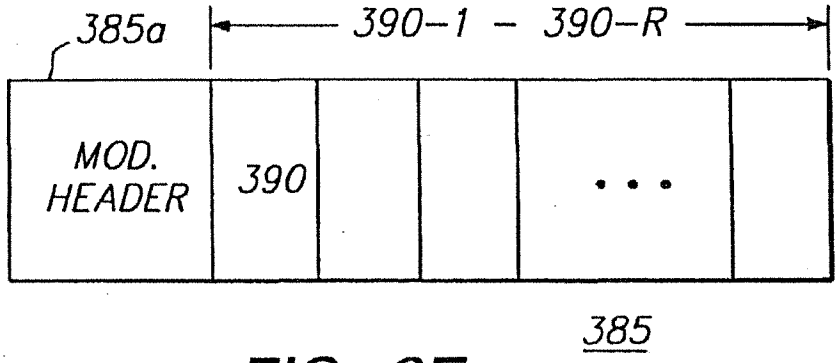


FIG. 3E

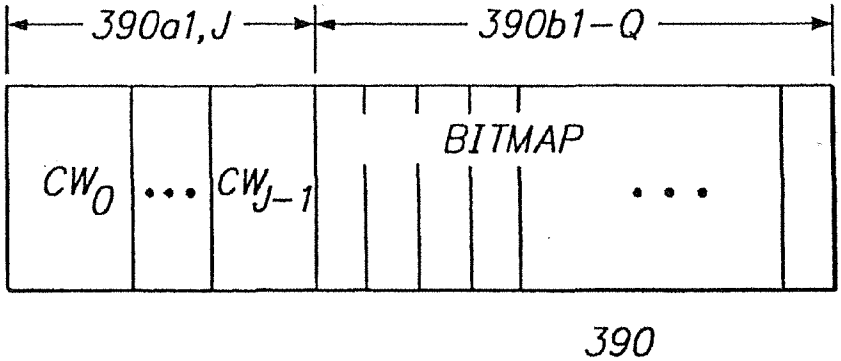


FIG. 3F

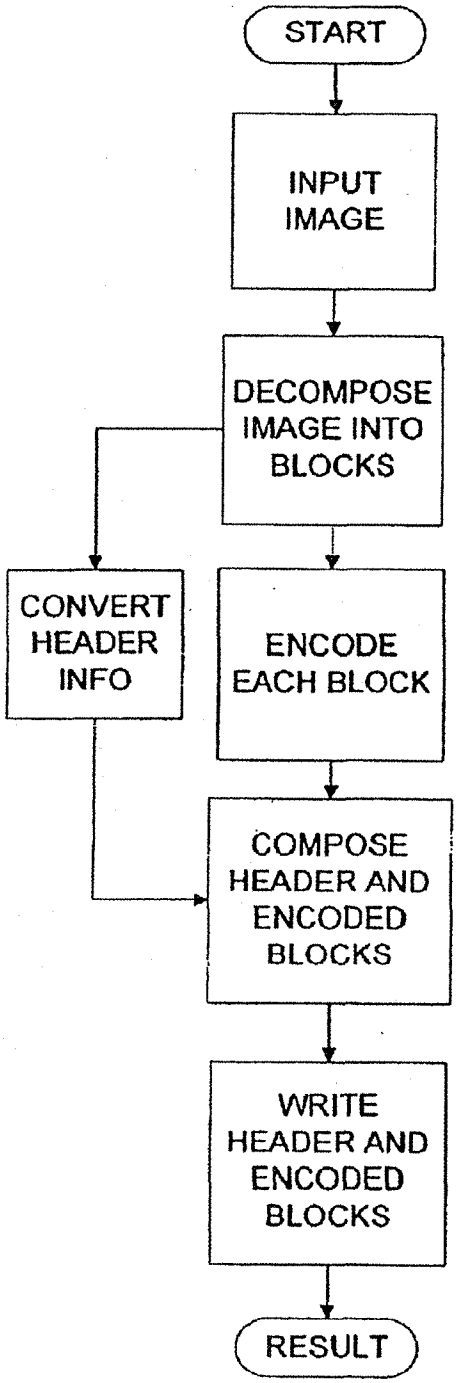

START
INPUT IMAGE
DECOMPOSE IMAGE INTO BLOCKS
CONVERT HEADER INFO
ENCODE EACH BLOCK
COMPOSE HEADER AND ENCODED BLOCKS
WRITE HEADER AND ENCODED BLOCKS
RESULT

Fig 4A

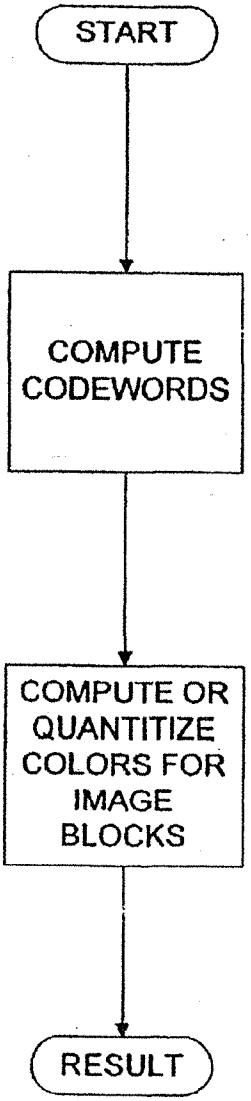

START
COMPUTE CODEWORDS
COMPUTE OR QUANTITIZE COLORS FOR IMAGE BLOCKS
RESULT

Fig 4B

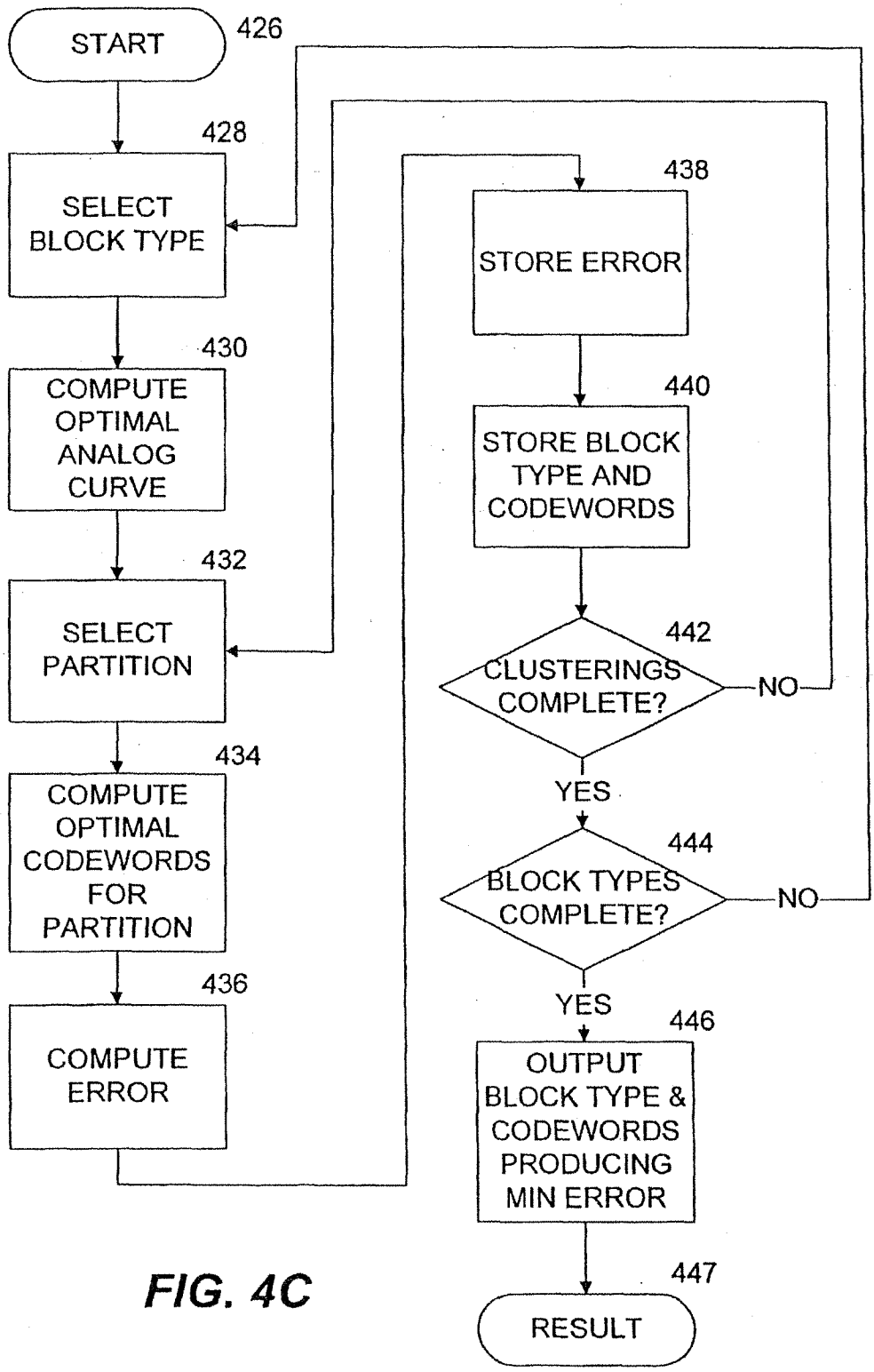

START
426
428
SELECT BLOCK TYPE
430
COMPUTE OPTIMAL ANALOG CURVE
432
SELECT PARTITION
434
COMPUTE OPTIMAL CODEWORDS FOR PARTITION
436
COMPUTE ERROR
438
STORE ERROR
440
STORE BLOCK TYPE AND CODEWORDS
442
CLUSTERINGS COMPLETE?
NO
YES
444
BLOCK TYPES COMPLETE?
NO
YES
446
OUTPUT BLOCK TYPE & CODEWORDS PRODUCING MIN ERROR
447
RESULT

FIG. 4C

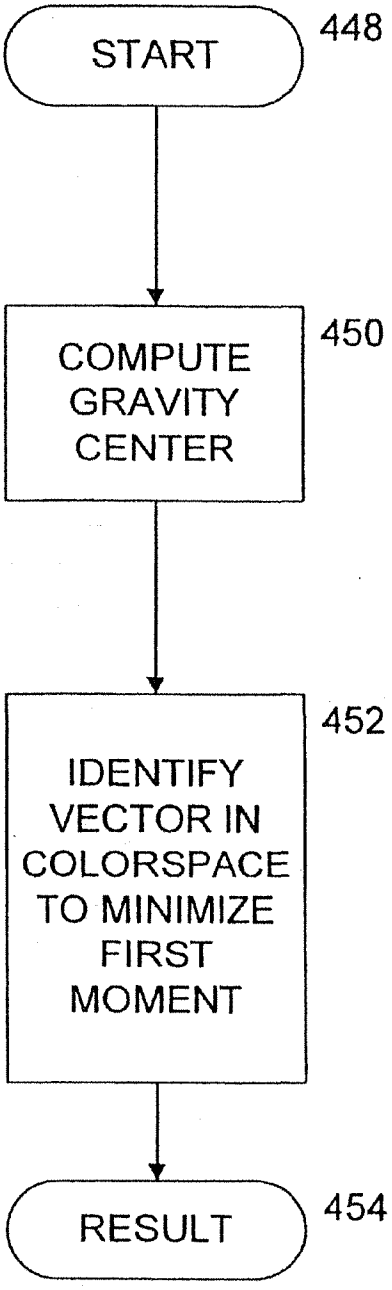

START
448
COMPUTE GRAVITY CENTER
450
IDENTIFY VECTOR IN COLORSPACE TO MINIMIZE FIRST MOMENT
452
RESULT
454

FIG. 4D

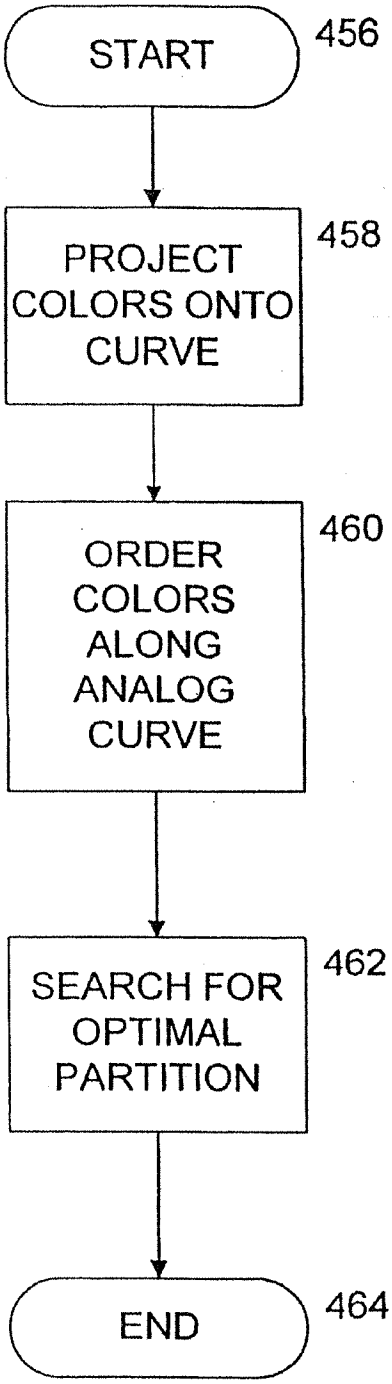

START
456
PROJECT COLORS ONTO CURVE
458
ORDER COLORS ALONG ANALOG CURVE
460
SEARCH FOR OPTIMAL PARTITION
462
END
464

FIG. 4E

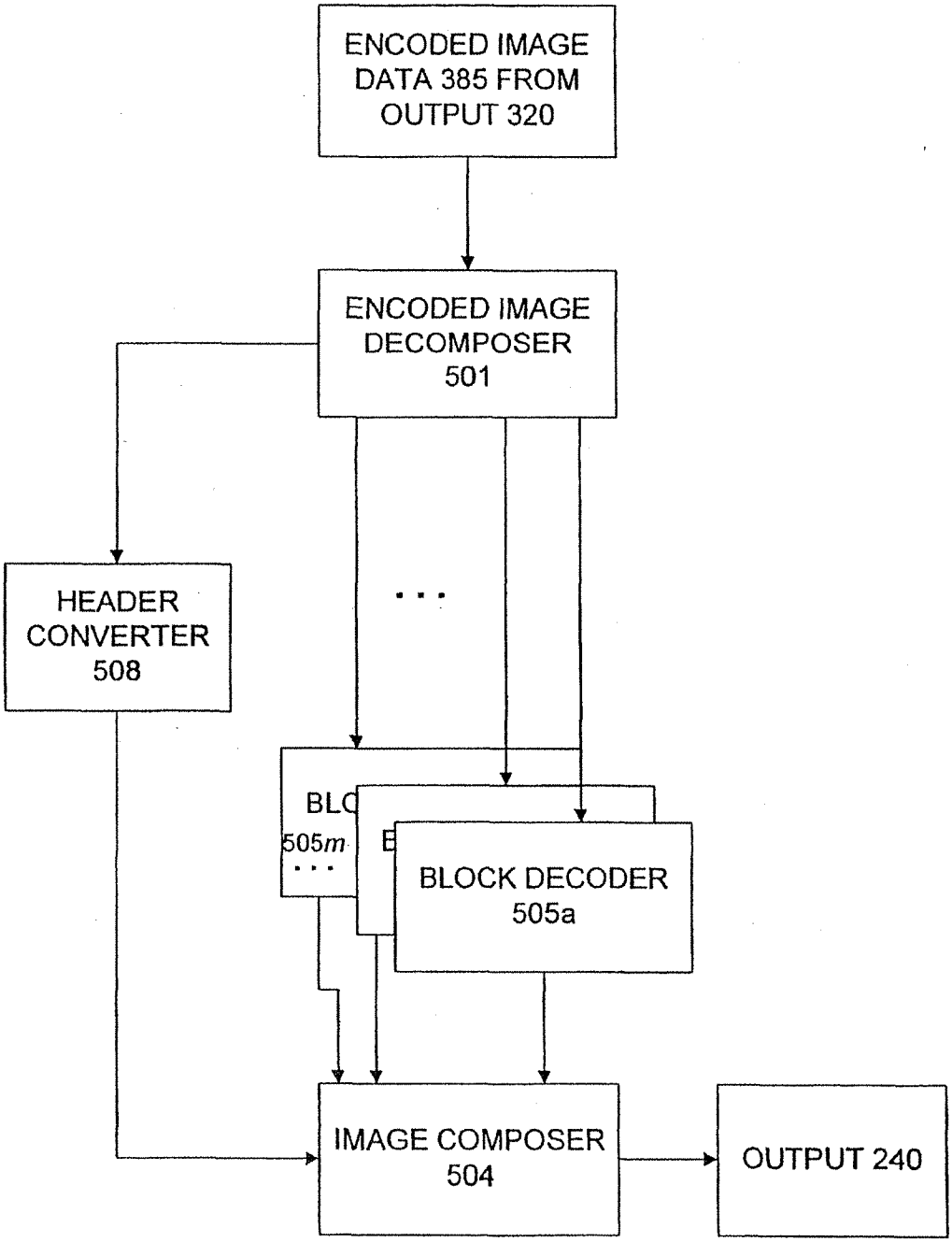

ENCODED IMAGE DATA 385 FROM OUTPUT 320
ENCODED IMAGE DECOMPOSER 501
HEADER CONVERTER 508
BLOCK DECODER 505a
IMAGE COMPOSER 504
OUTPUT 240

FIG. 5A

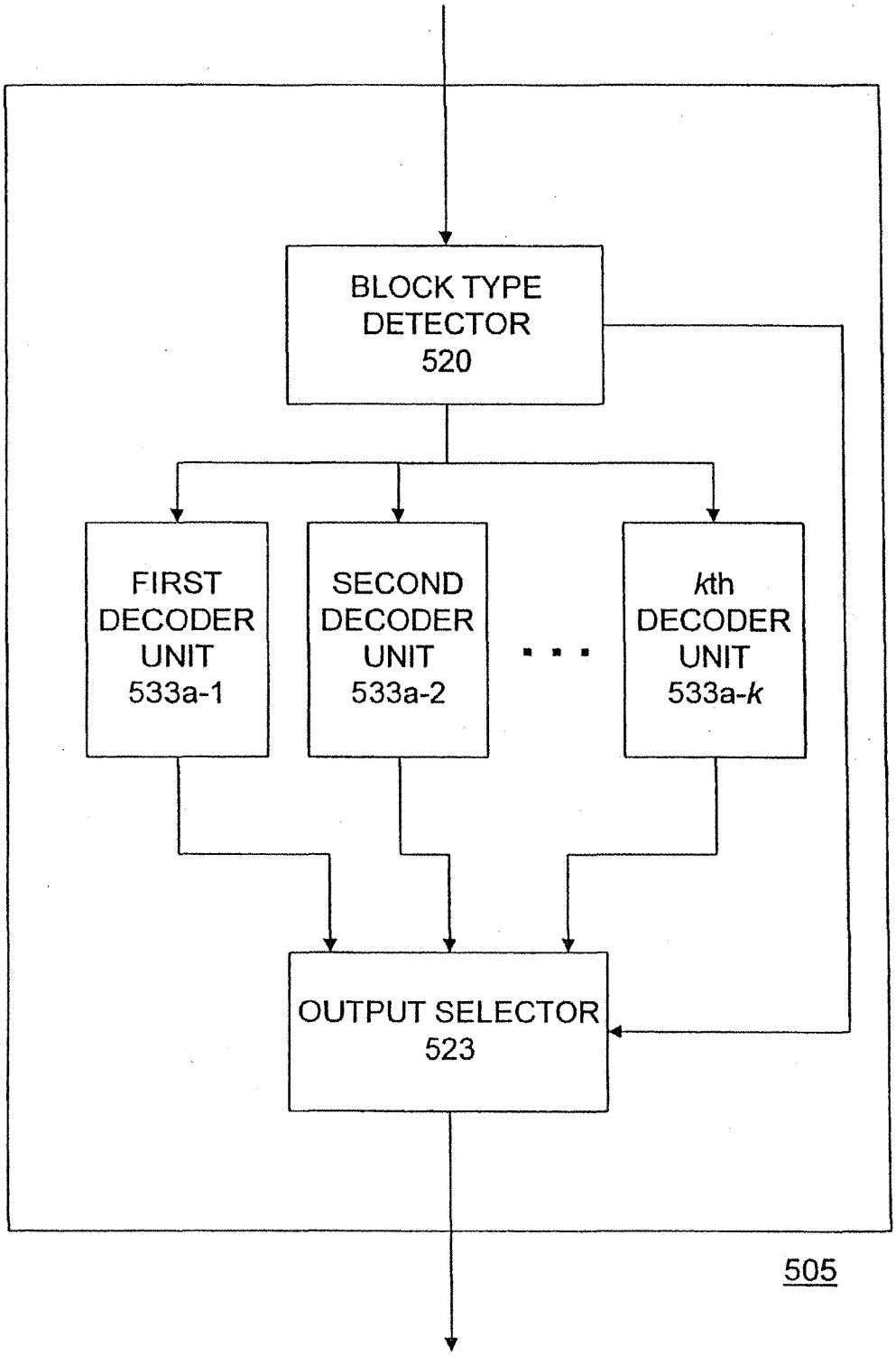

BLOCK TYPE DETECTOR 520
FIRST DECODER UNIT 533a-1
SECOND DECODER UNIT 533a-2
kth DECODER UNIT 533a-k
OUTPUT SELECTOR 523
505

FIG. 5B

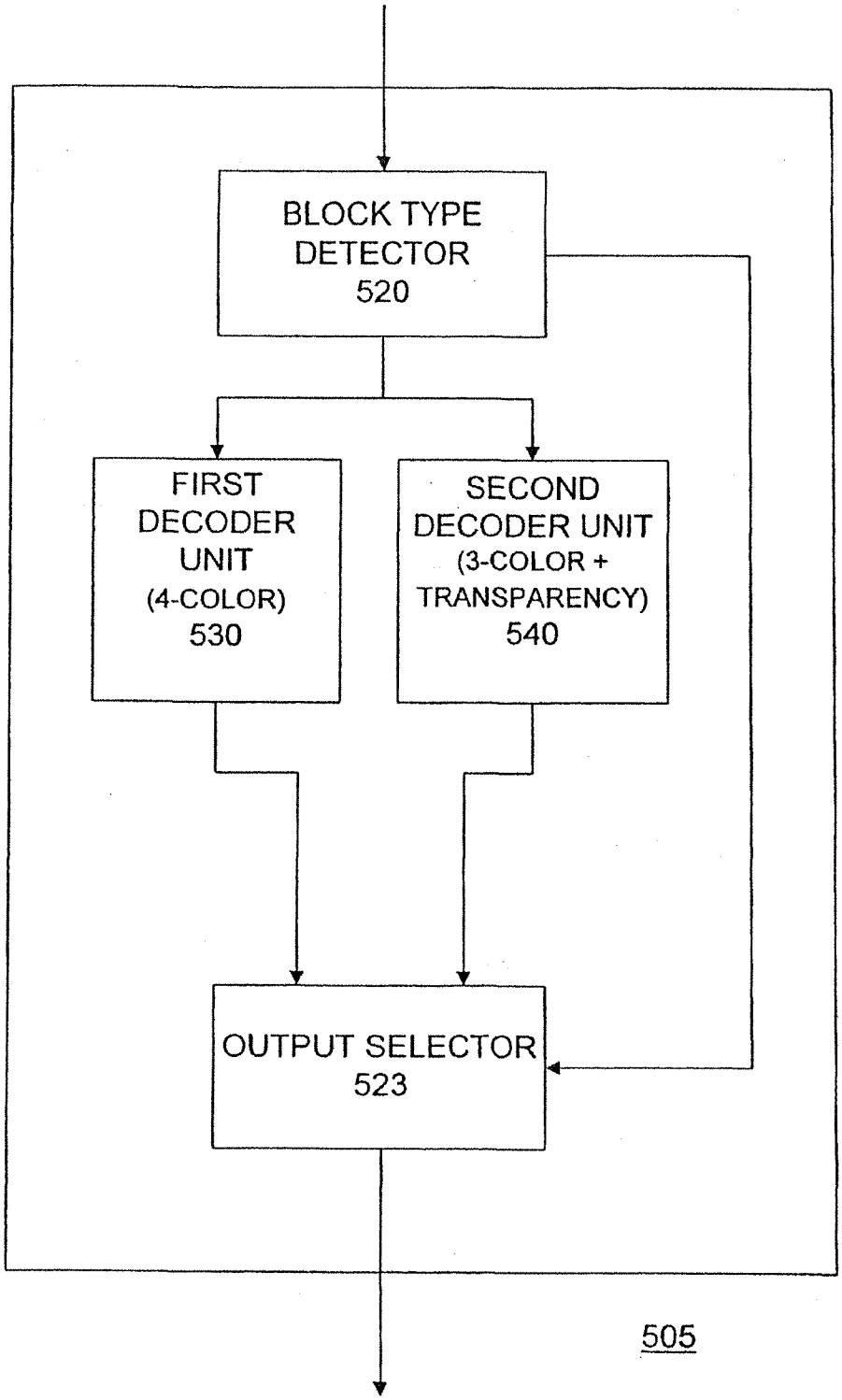

BLOCK TYPE DETECTOR 520
FIRST DECODER UNIT (4-COLOR) 530
SECOND DECODER UNIT (3-COLOR + TRANSPARENCY) 540
OUTPUT SELECTOR 523
505

FIG. 5C

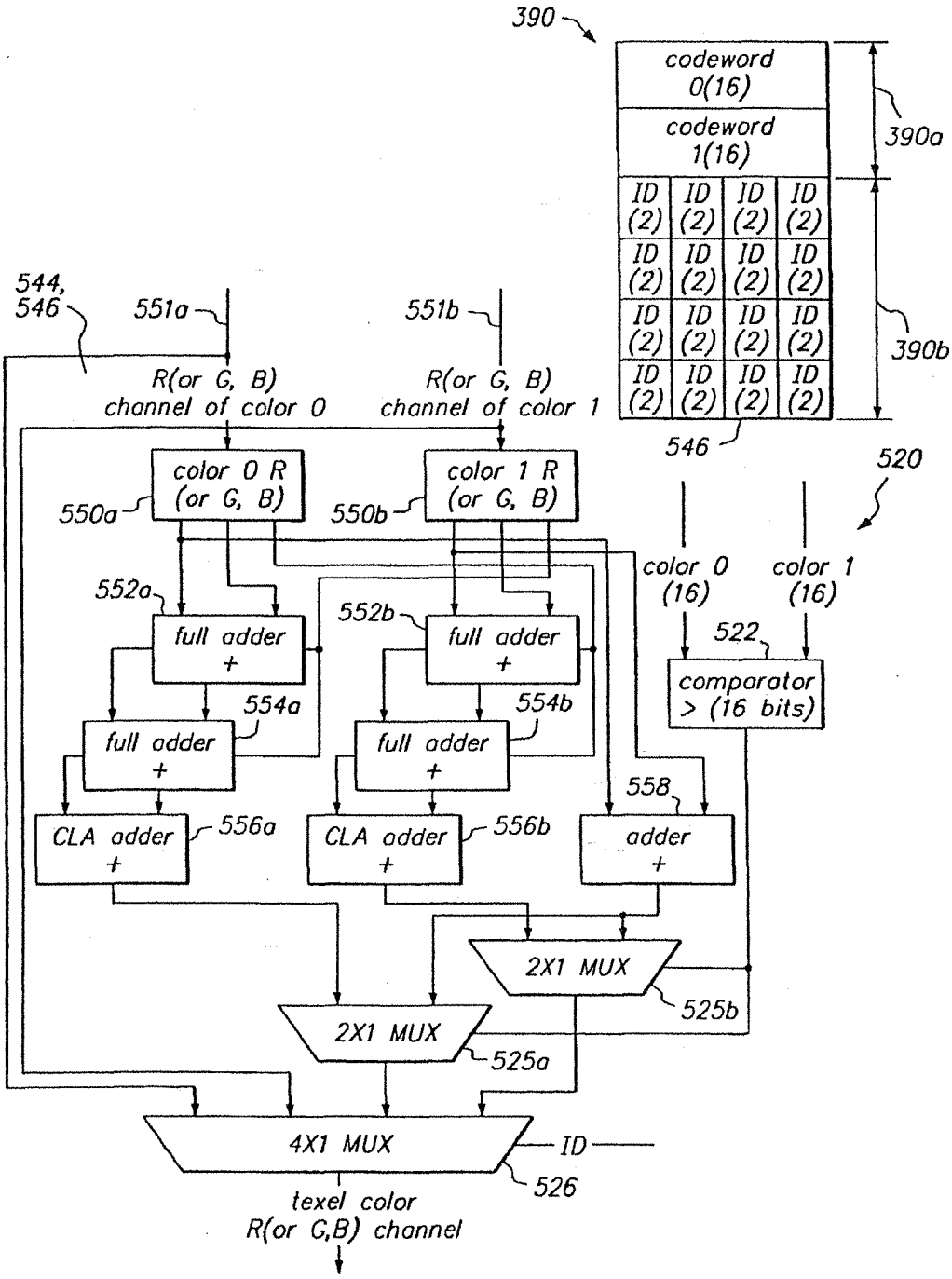

390
codeword 0(16)
codeword 1(16)
ID (2)
390a
390b
544, 546
551a
551b
R(or G, B) channel of color 0
R(or G, B) channel of color 1
546
520
color 0 R (or G, B)
color 1 R (or G, B)
550a
550b
color 0 (16)
color 1 (16)
552a
552b
522
full adder +
comparator > (16 bits)
554a
554b
558
CLA adder +
556a
556b
adder +
2X1 MUX
525b
525a
4X1 MUX
ID
526
texel color R(or G,B) channel

FIG. 5D

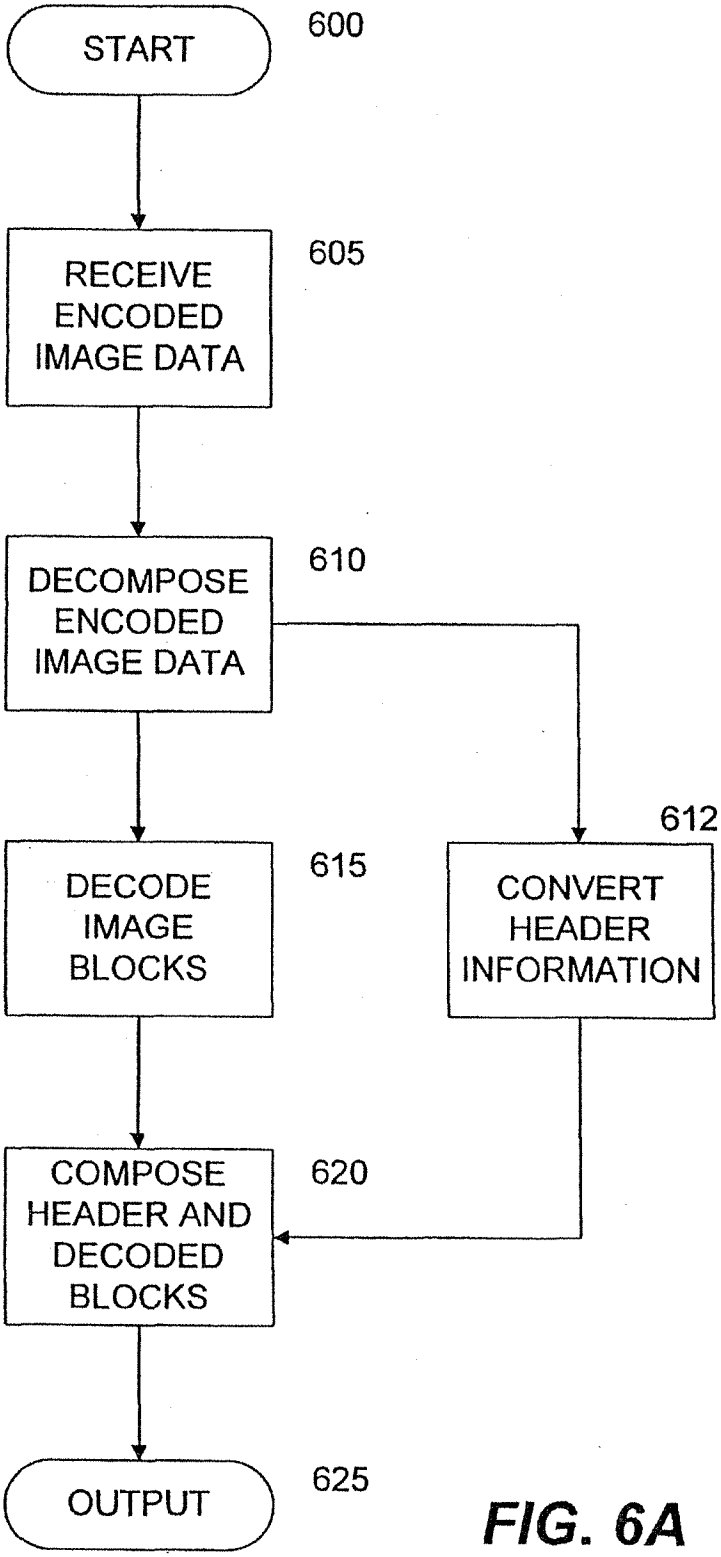

START
600
RECEIVE ENCODED IMAGE DATA
605
DECOMPOSE ENCODED IMAGE DATA
610
612
DECODE IMAGE BLOCKS
615
CONVERT HEADER INFORMATION
COMPOSE HEADER AND DECODED BLOCKS
620
OUTPUT
625

FIG. 6A

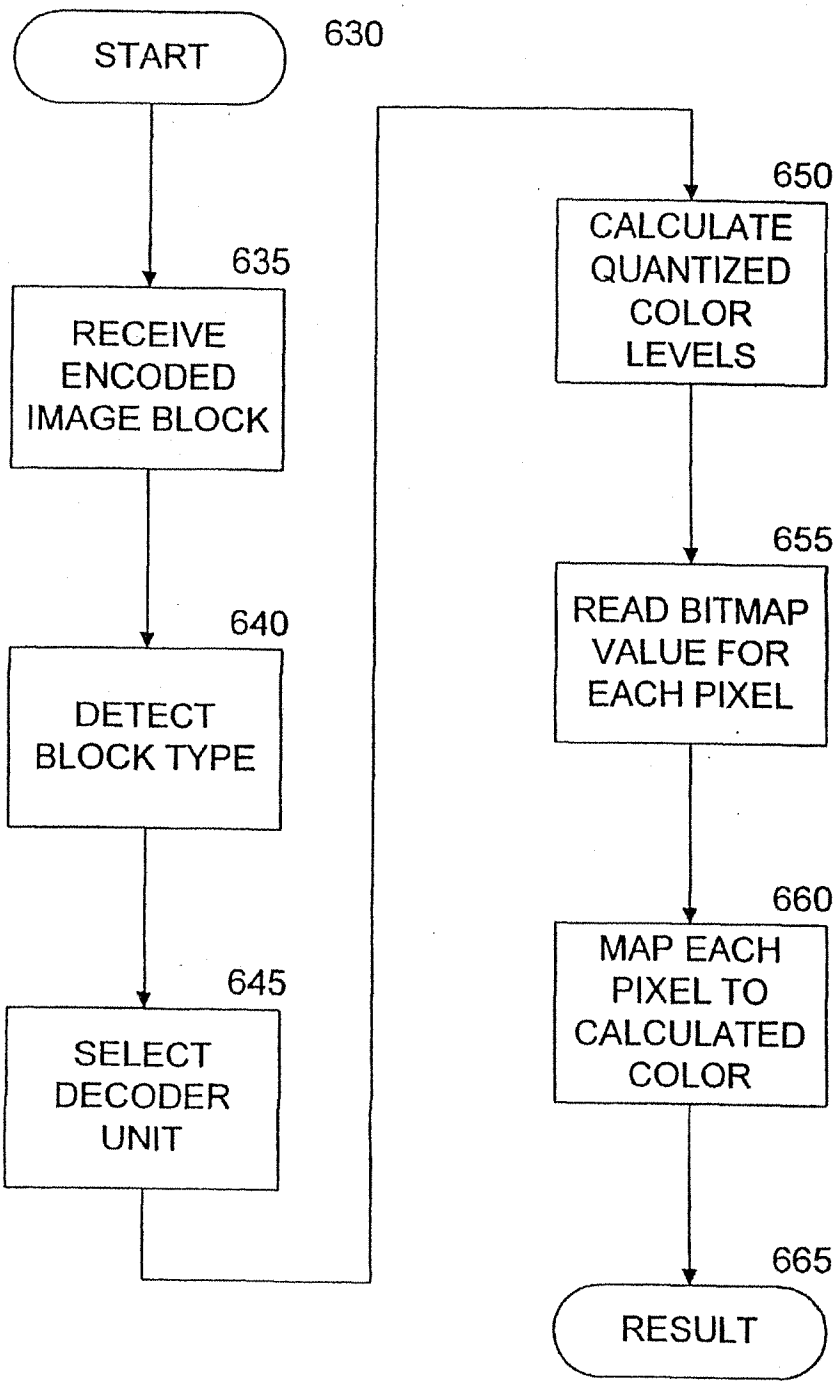

START
630
635
RECEIVE ENCODED IMAGE BLOCK
640
DETECT BLOCK TYPE
645
SELECT DECODER UNIT
650
CALCULATE QUANTIZED COLOR LEVELS
655
READ BITMAP VALUE FOR EACH PIXEL
660
MAP EACH PIXEL TO CALCULATED COLOR
665
RESULT

FIG. 6B

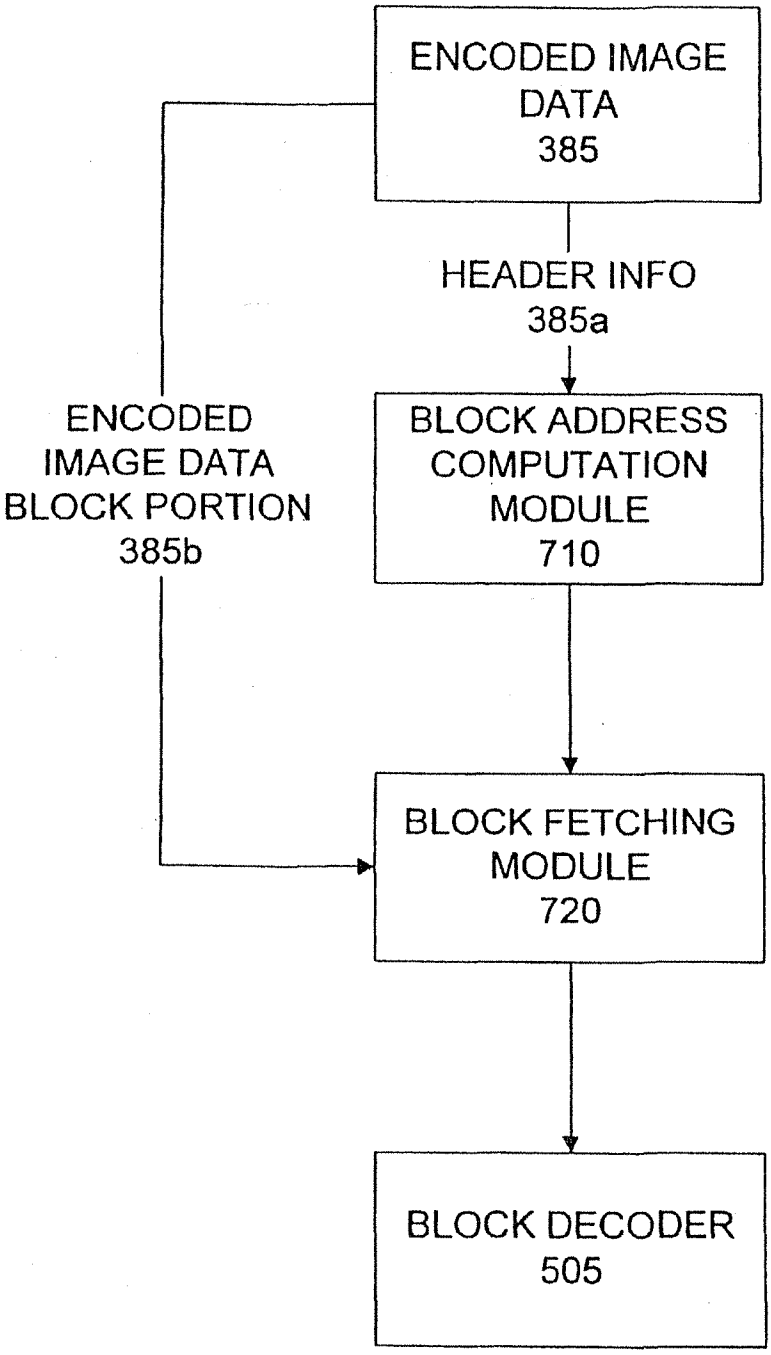

ENCODED IMAGE DATA 385
HEADER INFO 385a
ENCODED IMAGE DATA BLOCK PORTION 385b
BLOCK ADDRESS COMPUTATION MODULE 710
BLOCK FETCHING MODULE 720
BLOCK DECODER 505
700

FIG. 7A

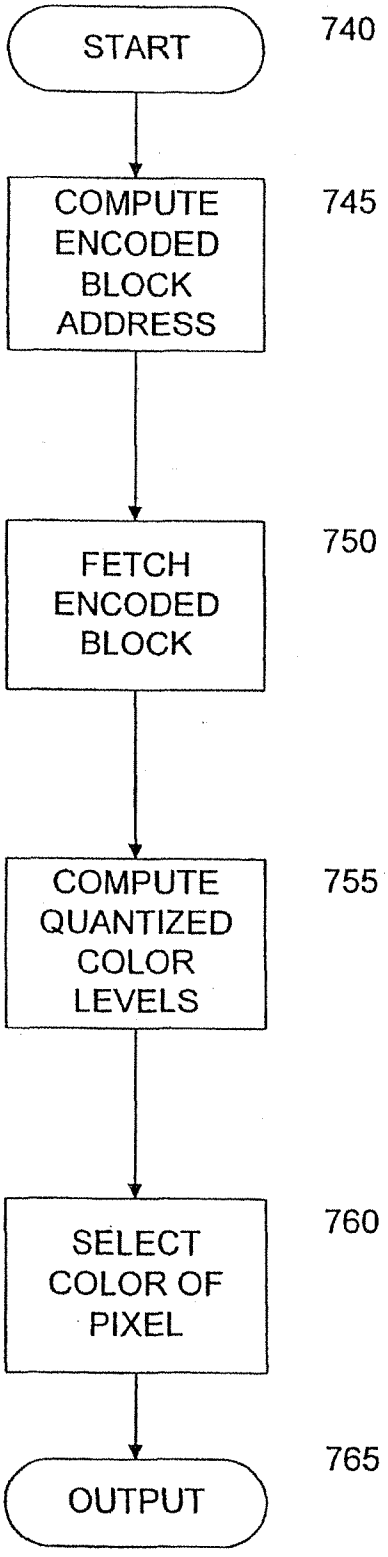

START
740
COMPUTE ENCODED BLOCK ADDRESS
745
FETCH ENCODED BLOCK
750
COMPUTE QUANTIZED COLOR LEVELS
755
SELECT COLOR OF PIXEL
760
OUTPUT
765

FIG. 7B

FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES

This is a CON of Ser. No. 08/942,850, filed Oct. 2, 1997, now U.S. Pat. No. 5,956,431.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to image processing systems, and more specifically, to three-dimensional rendering systems using fixed-rate image compression for textures.

2. Description of the Related Art

The art of generating images, such as realistic or animated graphics on a computer is known. To generate such images requires tremendous memory bandwidth and processing power on a graphics subsystem. To reduce the bandwidth and processing power requirements, various compression methods and systems were developed. These methods and systems included Entropy or lossless encoders, discrete cosine transform or JPEG type compressors, block truncation coding, color cell compression, and others. Each of these methods and systems, however, have numerous drawbacks.

Entropy or lossless encoders include Lempel-Ziv encoders and are used for many different purposes. Entropy coding relies on predictability. For data compression using Entropy encoders, a few bits are used to encode the most commonly occurring symbols. In stationary systems where the probabilities are fixed, Entropy coding provides a lower bound for the compression than can be achieved with a given alphabet of symbols. A problem with Entropy coding is that it does not allow random access to any given symbol. The part of the compressed data preceding a symbol of interest must be first fetched and decompressed to decode the symbol which takes considerable processing time and resources as well as decreasing memory throughput. Another problem with existing Entropy methods and systems is that they do not provide any guaranteed compression factor which makes this type of encoding scheme impractical where the memory size is fixed.

Discrete Cosine Transform ("DCT") or JPEG-type compressors, allow users to select a level of image quality. With DCT, uncorrelated coefficients are produced so that each coefficient can be treated independently without loss of compression efficiency. The DCT coefficients can be quantized using visually-weighted quantization values which selectively discard the least important information.

DCT, however, suffers from a number of shortcomings. One problem with DCT and JPEG-type compressors is that they require usually bigger blocks of pixels, typically 8×8 or 16×16 pixels, as a minimally accessible unit in order to obtain a reasonable compression factor and quality. Access to a very small area, or even a single pixel involves fetching a large quantity of compressed data, thus requiring increased processor power and memory bandwidth. A second problem with DCT and JPEG-type compressors is that the compression factor is variable, therefore requiring a complicated memory management system that, in turn, requires greater processor resources. A third problem with DCT and JPEG-type compression is that using a large compression factor significantly degrades image quality. For example, the image may be considerably distorted with a form of a ringing around the edges in the image as well as noticeable color shifts in areas of the image. Neither artifact can be removed with subsequent low-pass filtering.

A fourth problem with DCT and JPEG-type compression is that such a decompressor is complex and has a significant associated hardware cost. Further, the high latency of the decompressor results in a large additional hardware cost for buffering throughout the system to compensate for the latency. Finally, a fifth problem with DCT and JPEG-type compressors is that it is not clear whether a color keyed image can be compressed with such a method and system.

Block truncation coding ("BTC") and color cell compression ("CCC") use a local one-bit quantizer on 4×4 pixel blocks. The compressed data for such a block consists of only two colors and 16-bits that indicate which one of the two colors is assigned to each of the 16 pixels. Decoding a BTC/CCC image consists of using a multiplexer with a look-up table so that once a 16-texel-block (32-bits) is retrieved from memory, the individual pixels are decoded by looking up the two possible colors for that block and selecting the color according to the associated bit from the 16 decision bits.

The BTC/CCC methods quantize each block to just two color levels resulting in significant image degradation. Further, a two-bit variation of CCC stores the two colors as eight-bit indices into a 256-entry color lookup table. Thus, such pixel blocks cannot be decoded without fetching additional information that can consume additional memory bandwidth.

The BTC/CCC methods and systems can use a three-bit per pixel scheme which store the two colors as 16-bit values (not indices into a table) resulting in pixel blocks of six bytes. Fetching such units, however, decreases system performance because of additional overhead due to memory misalignment. Another problem with BTC/CCC is that when it is used to compress images that use color keying to indicate transparent pixels, there will be a high degradation of image quality.

Therefore, there is a need for a method and system that maximizes the accuracy of compressed images while minimizing storage, memory bandwidth requirements, and decoding hardware complexities, while also compressing image data blocks into convenient sizes to maintain alignment for random access to any one or more pixels.

SUMMARY OF THE INVENTION

An image processing system includes an image encoder system and an image decoder system that are coupled together. The image encoder system includes a block decomposer and a block encoder that are coupled together. The block encoder includes a color quantizer and a bitmap construction module. The block decomposer breaks an original image into image blocks, each having a plurality of pixel values (e.g. colors) or equivalent color points. Each image block is then processed by the block encoder. Specifically, the color quantizer computes some number of base points, or codewords, that serve as reference pixel values, such as colors, from which computed or quantized pixel values are derived. The bitmap construction module then maps at least one pixel value in the image block to one of the computed or quantized colors or one of the codewords. The codewords and bitmap are output as encoded image blocks.

The decoder system includes a block decoder having one or more decoder units and an output selector. The block decoder may also include a block type detector for determining the block type of an image block. The block type determines the number of computed colors to use for mapping each pixel color from an image block. Using the codewords of the encoded data blocks, the comparator and

the decoder units determine the computed colors for the encoded image block and map each pixel to one of the computed colors. The output selector outputs the appropriate color, which is ordered in an image composer with the other decoded blocks to output an image representative of the original image.

The present invention also includes a method of compressing an original image block having a set of original colors. The method includes: computing a set of codewords from the set of original colors; computing a set of computed colors using the set of codewords; and mapping each original color to one of the computed colors or one of the codewords to produce an index for each original color.

The compressed or encoded image block, which has a first set of indices and a set of codewords, where a set is equal to or greater than one, is decoded by: computing at least one computed color using the set of codewords; and mapping an index within the first set of indices to one of the computed colors or one of the codewords.

Those of ordinary skill in the art will readily recognize that the present invention may be practiced using any general purpose computer system, such as the computer system described below, or any "hardwired" device specifically designed to perform the method, such as but not limited to devices implemented using ASIC or FPGA technology and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a data processing system in accordance with the present invention;

FIG. **2A** is a block diagram of an image processing system in accordance with the present invention;

FIG. **2B** is a graphical representation of an image block in accordance with the present invention;

FIG. **3A** is a block diagram of a first embodiment an image encoder system in accordance with the present invention;

FIG. **3B** is a block diagram of a second embodiment of an image encoder system in accordance with the present invention;

FIG. **3C** is a block diagram of an image block encoder in accordance with the present invention;

FIG. **3D** is a data sequence diagram of an original image in accordance with the present invention;

FIG. **3E** is a data sequence diagram of encoded image data of the original image output from the image encoder system in accordance with the present invention;

FIG. **3F** is a data sequence diagram of an encoded image block from the image block encoder in accordance with the present invention;

FIGS. **4A–4F** are flow diagrams illustrating an encoding process in accordance with the present invention;

FIG. **5A** is a block diagram of an image decoder system in accordance with the present invention;

FIG. **5B** is a block diagram of a first embodiment of a block decoder in accordance with the present invention;

FIG. **5C** is a block diagram of a second embodiment of a block decoder in accordance with the present invention;

FIG. **5D** is a logic diagram illustrating a first embodiment of a decoder unit in accordance with the present invention;

FIGS. **6A–6B** are flow diagrams illustrating a decoding process in accordance with the present invention;

FIG. **7A** is a block diagram of a subsystem for random access to a pixel or an image block in accordance with the present invention; and

FIG. **7B** is a flow diagram illustrating random access to a pixel or an image block in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** is a block diagram of a data processing system **105** constructed in accordance with the present invention. The data processing system **105** includes a processing unit **110**, a memory **115**, a storage device **120**, an input device **125**, an output device **130**, and a graphics subsystem **135**. In addition, the data processing system **105** includes a data bus **145** that couples each of the other components **110, 115, 120, 125, 130, 135** of the data processing system **105**.

The data bus **145** is a conventional data bus and while shown as a single line it may be a combination of a processor bus, a PCI bus, a graphical bus, and an ISA bus. The processing unit **110** is a conventional processing unit such as the Intel Pentium processor, Sun SPARC processor, or Motorola PowerPC processor, for example. The processing unit **110** processes data within the data processing system **105**. The memory **115**, the storage device **120**, the input device **125**, and the output device **130** are also conventional components as recognized by those skilled in the art. The memory **115** and storage device **120** store data within the data processing system **105**. The input device **125** inputs data into the system while the output device **130** receives data from the data processing system **105**.

FIG. **2A** is a block diagram of an image processing system **205** constructed in accordance with the present invention. In one embodiment, the image processing system **205** runs within the data processing system **105**. The image processing system **205** includes an image encoder system **220** and an image decoder system **230**. The image processing system **205** may also include a unit for producing an image source **210** from which images are received, and an output **240** to which processed images are forwarded for storage or further processing. The image encoder system **220** is coupled to receive an image from the image source **210**. The image decoder system **230** is coupled to output the image produced by the image processing system **205**. The image encoder system **220** is coupled to the image decoder system **230** through a data line and may be coupled via a storage device **120** and/or a memory **115**, for example.

Within the image encoder system **220**, the image is broken down into individual blocks and processed before being forwarded to, e.g., the storage device **140**, as compressed or encoded image data. When the encoded image data is ready for further data processing, the encoded image data is forwarded to the image decoder system **230**. The image decoder system **230** receives the encoded image data and decodes it to generate an output that is a representation of the original image that was received from the image source **210**.

FIGS. **3A** and **3B** are block diagrams illustrating two separate embodiments of the image encoder system **220** of the present invention. The image encoder system **220** includes an image decomposer **315**, a header converter **321**, one or more block encoders **318** (**318***a*–**318***n*, where n is the nth encoder, n being any positive integer), and an encoded image composer **319**. The image decomposer **315** is coupled to receive an original image **310** from a source, such as the image source **210**. The image decomposer **315** is also coupled to the one or more block encoders **318** and to the header converter **321**. The header converter **321** is also coupled to the encoded image composer **319**. Each block encoder **318** is also coupled to the encoded image composer **319**. The encoded image composer **319** is coupled to the output **320**.

The image decomposer **315** receives the original image **310** and forwards information from a header of the original image **310** to the header converter **321**. The header converter **321** modifies the original header to generate a modified header, as further described below. The image decomposer **315** also breaks, or decomposes, the original image **310** into R number of image blocks, where R is some integer value. The number of image blocks an original image **310** is broken into may depend on the number of image pixels. For example, in a preferred embodiment an image **310** comprised of A image pixels by B image pixels will typically be (A/4)*(B/4) blocks, where A and B are integer values. For example, where an image is 256 pixels by 256 pixels, there will be 64×64 blocks. In other words, the image is decomposed such that each image block is 4 pixels by 4 pixels (16 pixels). Those skilled in the art will recognize that the number of pixels or the image block size may be varied, for example m×n pixels, where m and n are positive integer values.

Briefly turning to FIG. 2B, there is illustrated an example of a single image block **260** in accordance with the present invention. The image block **260** is comprised of pixels **270**. The image block **260** may be defined as an image region W pixels **270** in width by H pixels **270** in height, where W and H are integer values. In a preferred embodiment, the image block **260** is comprised of W=4 pixels **270** by H=4 pixels **270** (4×4).

Turning back to FIGS. **3A** and **3B**, each block encoder **318** receives an image block **260** from the image decomposer **315**. Each block encoder **318** encodes or compresses each image block **260** that it receives to generate an encoded or compressed image block. Each encoded image block is received by the encoded image composer **319** which orders the encoded blocks in a data file. The data file from the encoded image composer **319** is concatenated with a modified header from the header converter **321** to generate an encoded image data file that is forwarded to the output **320**. Further, it is noted that having more than one block encoder **318***a*–**318***n* allows for encoding multiple image blocks simultaneously, one image block per block encoder **318***a*–**318***n*, within the image encoder system **220** to increase image processing efficiency and performance.

The modified header and the encoded image blocks together form the encoded image data that represents the original image **310**. The function of each element of the image encoder system **220**, including the block encoder **318**, will be further described below with respect to FIGS. **4A**–**4E**.

The original image **310** may be in any one of a variety of formats including red-green-blue ("RGB"), YUV **420**, YUV **422**, or a proprietary color space. It may be useful in some cases to convert to a different color space before encoding the original image **310**. It is noted that in one embodiment of the present invention, each image block **260** is a 4×4 set of pixels where each pixel **270** is 24-bits in size. For each pixel **270** there are 8-bits for a Red(R)-channel, 8-bits for a Green(G)-channel, and 8-bits for a Blue(B)-channel channel in a red-green-blue ("RGB") implementation color space. Further, each encoded image block is also a 4×4 set of pixels, but, each pixel is only 2-bits in size and has an aggregate size of 4-bits as will be further described below.

FIG. **3C** is a block diagram illustrating a block encoder **318** of the present invention in greater detail. The block encoder **318** includes a color quantizer **335** and a bitmap construction module **340**. The color quantizer **335** is coupled to the bitmap construction module **340**. Further, the color quantizer **335** further emphasizes a block type module **345**, a selection module **355**, and a codeword generation module **360**. The block type module **345** is coupled to the selection module **355**. The selection module **355** is coupled to the codeword generation module **360**.

Each image block **260** of the decomposed original image **310** is received and initially processed by the color quantizer **335** before being forwarded to the bitmap construction module **340** for further processing. The bitmap construction module **340** outputs encoded image blocks for the encoded image composer **319** to order. The bitmap construction module **340** and the color quantizer **335**, including the block type module **345**, the selection module **355**, and the codeword generation module **360**, are further discussed below in FIGS. **4A**–**4E**.

Briefly, FIG. **3D** is a diagram of a data sequence or string **380** representing the original image **310** that is received by the block decomposer **315**. The data string **380** of the original image **310** includes an a-bit header **380***a* and a b-bit image data **380***b*, where a and b are integer values. The header **380***a* may include information such as the pixel width of the image **310**, the pixel height of the image **310**, and the format of the image **310**, e.g., the number of bits to the pixel in RGB or YUV format, for example, as well as other information. The image data is the data **380***b* representing the original image **310** itself.

FIG. **3E** is a diagram of a data sequence or string **385** representing encoded image data **385** that is generated and output **320** by the image encoder system **220**. The data string for the encoded image data **385** includes a modified header portion **385***a* and an encoded image block portion **390-1**–**390-R**. The modified header portion **385***a* is generated by the header converter **321** from the original header **380***a* for the original image **310**. The modified header generated by the header converter **321** includes information about file type, a number of bits per pixel of the original image **310**, addressing into the original image **310**, other miscellaneous encoding parameters, as well as the width and height information indicating the size of that original image **310**. The encoded image block portion **390-1**-R includes the encoded image blocks **390-1**–**390-R** from the block encoders **318**, where R is an integer value that is the number of blocks resulting from the decomposed original image **310**.

FIG. **3F** is a diagram of a data sequence or string **390** representing an encoded image block in accordance with the present invention. It is understood that the data string **390** representing the encoded image block may be similar to any one of the encoded image blocks **390-1**–**390-R** shown in the encoded image data string **385**.

The data string **390** of the encoded image block includes a codeword section **390***a* which includes J codewords, where J is an integer value, and a bitmap section **390***b*. The codeword section **390***a* includes J codewords **390***a* that are used to compute the colors indexed by the bitmap **390***b*. A codeword is a n-bit data string, where n is an integer value, that identifies a pixel property, for example a color component. In a preferred embodiment, there are two 16-bit codewords **390***a*, CW0, CW1 (J=2). The bitmap is a Q-bit data portion and is further discussed below in FIG. **4B**.

Further, in a preferred embodiment, each encoded image block is 64-bits, which includes two 16-bit codewords and a 32-bit (4×4×2 bit) bitmap **395**. Encoding the image block **260** as described provides greater system flexibility and increased data processing efficiency as will be further discussed below.

FIGS. **4A**–**4E** describe the operation of the image encoder system **220**. FIG. **4A** describes the general operation of the

image encoder system **220**. At the start **402** of operation, data string **380** of the original image **310**, that includes the a-bit header **380***a* and the b-bit image data **380***b*, is input **404** into the block decomposer **315** from the image source **210**. The block decomposer **315** decomposes **406** the original image **310** to extract the a-bit header **380***a* and forward it to the header converter **321**. The block decomposer also **315** decomposes, **406** the original image **310** into image blocks. Each image block **260** is independently compressed, or encoded, **410** in the one or more block encoders **318**.

The header converter **321** converts **408** the a-bit header to generate a modified header **385***a*. The modified header **385***a* is forwarded to the encoded image composer **319**. Simultaneous with the header converter **321** converting **408** the α-bit header, each image block is encoded **410** by the one or more image encoders **318***a*–**318***n* to generate the encoded image blocks **390**-1–**390**-R. Again, it is noted that each image block **260** may be processed sequentially in one block encoder **318***a* or multiple image blocks **260** may be processed in parallel in multiple block encoders **318***a*–**318***n*.

The encoded image blocks **390** are output from the block encoders **318** and are placed into a predefined order by the encoded image composer **319**. In a preferred embodiment, the encoded image blocks **390** are ordered in a file from left to right and top to bottom in the same order in which they were broken down by the block decomposer **315**. The image encoder system **220** continues by composing **412** the modified header information **385***a* from the header converter **321** and the encoded image blocks **390**. Specifically, the modified header **385***a* and the ordered encoded image blocks **390** are concatenated to generate the encoded image data file **385**. The encoded image data file **385** is written **414** as encoded output **320** to the memory **115**, the storage device **120**, or the output device **130**, for example.

FIG. 4B shows the encoding process **410** for the encoder system **220** described above in FIG. 2. At the start **418** of operation, codewords are computed **420**. As discussed above in FIG. 3F, in a preferred embodiment there are two codewords **390***a*, CW0, CW1. The process for computing codewords is further described below in FIG. 4C.

Once the codewords are computed **420** pixel values or properties, such as colors, for the image block **260** are computed or quantized quantized **422**. Specifically, the codewords **390***a* provide points in a pixel space from which M quantized pixel values may be inferred, where M is an integer value. The M quantized pixel values are a limited subset of pixels in a pixel space that are used to represent the current image block. The process for quantizing pixel values, and more specifically colors, will be described below in FIGS. 4D and 4E. Further, it is noted that the embodiments will now be described with respect to colors of a pixel value although one skilled in the art will recognize that in general any pixel value may be used with respect to the present invention.

In a preferred embodiment, each pixel is encoded with two bits of data which can index one of M quantized colors (M=4). Further, in a preferred embodiment the four quantized colors are derived from the two codewords **390***a* where two colors are the codewords themselves and the other two colors are inferred from the codewords, as will be described below. It is also possible to use the codewords **390***a* so that there is one index to indicate a transparent color and three indices to indicate colors, of which one color is inferred.

In a preferred embodiment, the bitmap **390***b* is a 32-bit data string. The bitmap **390***b* and codewords **390***a* are output **424** as a 64-bit data string representing an encoded image block **390**. Specifically, the encoded image block **390** includes the two 16-bit codewords **390***a* (n=16) and a 32-bit bitmap **390***b*. Each codeword **390***a* CW0, CW1 that is a 16-bit data string includes a 5-bit red-channel, 6-bit green-channel, and 5-bit blue-channel.

Each of the encoded image blocks **390** is placed together **390***a*1–**390***a*R, and concatenated with header information **385***a* derived from the original header **380***a* of the original image **310**. The resulting **424** output is the encoded image data **385** representing the original image **310**.

FIG. 4C describes the process for computing **420** the codewords for the image blocks **260** in more detail. At the start **426** of the process, the color quantizer **335** uses the block type module **345** to select **428** the first block type for the image block **260** that is being processed. For example, one block type selected **428** may be a four-color and another block type selected **428** may be a three-color plus transparency, where the colors within the particular block type have equidistant spacing in a color space.

Those of ordinary skill in the art will readily recognize that selecting a block type for each image is not intended to be limiting in any way. Instead, the present invention may be limited to processing image blocks that are of a single block type. This eliminates the need to distinguish between different block types, such as the three and four color block types discussed above. Consequently, the block type module **345** in FIG. 3B and reference number **428** in FIG. 4C are optional and are not intended to limit the present invention in any way.

Once the block type is selected **428**, the process computes **430** an optimal analog curve for the block type. Computation **430** of the optimal analog curve **430** will be further described below in FIG. 4D. The analog curve is used to simplify quantizing of the colors in the image block. After computing **430** the optimal analog curve, the process selects **432** a partition of the points along the analog curve. A partition may be defined as a grouping of indices {1 . . . . (WxH)} into M nonintersecting sets. In a preferred embodiment, the indices (1 . . . 16) are divided into three or four groups, or clusters, (M=3 or 4) depending on the block type.

Once a partition is selected **432**, the optimal codewords for that **20** particular partition are computed **434**. Computation **434** of the optimal codewords is further described below in FIG. 4E. In addition to computing **434** the codewords, an error value (squared error as describe below) for the codewords is also computed **436**. Computation **436** of the error values is further described below with respect to FIG. 4E also. If the computed **436** error value is the first error value it is stored. Otherwise, the computed **436** error value is stored **438** only if it is less than the previously stored error value. For each stored **438** error value, the corresponding block type and codewords are also stored **440**. It is noted that the process seeks to find the block type and codewords that minimize the error function.

The process continues by determining **442** if the all the possible partitions are complete. If there are more partitions possible, the process selects **432** the next partition and once again computes **434** the codewords, computes **436** the associated error value, and stores **438** the error value and stores **440** associated block type and codewords only if the error value is less than the previously stored error value.

After all the possible partitions are completed, the process determines **444** whether all the block types have been selected. If there are more block types, the process selects **428** the next block type. Once again, the process will

compute **430** the optimal analog curve, select **432**, **442** all the possible partitions, for each partition it will compute **434**, **436** the codewords and associated error value, and store **438**, **440** the error value and associated block type and codeword only if the error value is less than the previously stored error value. After the last block type is processed, the process outputs **446** a result **447** of the block type and codewords **390***a* having the minimum error.

In an alternative embodiment, the optimal analog curve may be computed **430** before searching the block type. That is, the process may compute **430** the optimal analog curve before proceeding with selecting **428** the block type, selecting **432** the partition, computing **434** the codewords, computing **436** the error, storing **438** the error, and storing **440** the block type and codeword. Computing **430** the optimal analog curve first is useful if all the block types use the same analog curve and color space because the analog curve does not need to be recomputed for each block type.

FIG. 4D further describes the process of identifying the optimal analog curve. The selection module **355** starts **448** the process by computing a center of gravity **450** for pixel **270** colors of an image block **260**. Computing **450** the center of gravity includes averaging the pixel **270** colors of the image block **260**. Once the center of gravity is computed **450**, the process identifies **452** a vector in color space to minimize the first moment of the pixel **270** colors of the image block **260**.

Specifically, for identifying **452** the vector the process fits a straight line to a set of data points, which are the original pixel **270** colors of the image block **260**. A straight line is chosen passing through the center of gravity of the set of points such that it minimizes the "moment of inertia" (the means square error). For example, for three pixel properties, to compute the direction of the line minimizing the moment of inertia, tensor inertia, T, is calculated from the individual colors as follows:

$$T = \sum \begin{matrix} C_{1i}^2 + C_{2i}^2 & -C_{0i}C_{1i} & -C_{0i}C_{2i} \\ -C_{0i}C_{1i} & C_{0i}^2 + C_{2i}^2 & -C_{1i}C_{2i} \\ -C_{0i}C_{2i} & -C_{2i}C_{1i} & C_{0i}^2 + C_{1i}^2 \end{matrix}$$

where C_0, C_1, and C_2 represent pixel properties, for example color components in RGB or YUV, relative to a center of gravity. In a preferred embodiment of an RGB color space, C_{0i} is the value of red, C_{1i} is the value of green, and C_{2i} is the value of blue for each pixel, i, of the image block. Further, i takes on integer values from 1 to WxH, so that if W=4 and H=4, i ranges from 1 to 16.

The eigenvector of tensor, T, with the smallest eigenvalue is calculated using conventional methods known to those skilled in the art. The eigenvector direction along with the calculated gravity center, defines the axis that minimizes the moment of inertia. This axis is used as the optimal analog curve, which in a preferred embodiment is a straight line. Those of ordinary skill in the art will readily recognize that the term optimal analog curve is not limited solely to a straight line but may include a set of parameters, such as pixel values or colors, that minimizes the moment of inertia or means square error when fitted to the center of gravity of the pixel colors in the image block. The set of parameters may define any geometric element, such as but not limited to a curve, a plane, a trapezoid, or the like.

FIG. 4E illustrates the process undertaken by the codeword generation module **360** for selecting **432** the partitions, computing **434**, **436** the codewords for the partitions and the associated error, and storing **438**, **440** the error value, block type, and codeword if the error value is less than a previously stored error value. The process starts **456** with the codeword generation module **360** projecting **458** the WxH color values onto the previously constructed optimal analog curve. The value of WxH is the size in number of pixels **270** of an image block **260**. In a preferred embodiment, where W and H are both **4** pixels, WxH is 16 pixels.

Once the colors are projected **458** onto the analog curve, the colors are ordered **460** sequentially along that analog curve based on the position of the color on the one-dimensional analog curve. After the colors are ordered **460**, the codeword generation module **360** searches **462** for optimal partitions. That is, the codeword generation module **360** takes the WxH colors (one color associated with each pixel) that are ordered **460** along the analog curve and partitions, or groups, them into a finite number of clusters with a predefined relative spacing. In a preferred embodiment, where W=4 and H=4, so that WxH is 16, the 16 colors are placed in three or four clusters (M=3 or 4).

In conducting the search **462** for the optimal partition, the color selection module **360** finds the best M clusters for the WxH points projected onto the optimal curve, so that the error associated with the selection is minimized. The best M clusters are determined by minimizing the mean square error with the constraint that the points associated with each cluster are spaced to conform to the predefined spacing.

In a preferred embodiment, for a block type of four equidistant colors, the error may be defined as a squared error along the analog curve, such as

$$E^2=\Sigma_{cluster0}(x_i-p_0)^2+\Sigma_{cluster1}(x_i-((⅓)p_0+(⅔)p_1))^2+\Sigma_{cluster2}(x_i-((⅔)p_0+(⅓)p_1))^2+\Sigma_{cluster3}(x_i-p_1)^2$$

where E is the error for the particular grouping or clustering, p_0 and p_1 are the coded colors, and x_i are the projected points on the optimal analog curve.

In instances where the block type indicates three equidistant colors, the error may be defined as a squared error along the analog curve, such as

$$E^2=\Sigma_{cluster0}(x_i-p_0)^2+\Sigma_{cluster1}(x_i-((½)p_0+(½)p_1))^2+\Sigma_{cluster2}(x_i-p_1)^2$$

where, again, E is the error for the particular grouping or clustering, p_0 and p_1 are the coded colors, and x_i are the projected points on the optimal analog curve.

After the resulting **447** optimal codewords **390***a* are identified, they are forwarded to the bitmap construction module **340**. The bitmap construction module **340** uses the codewords **390***a* to identify the M colors that may be specified or inferred from those codewords **390***a*. In a preferred embodiment, the bitmap construction module **340** uses the codewords **390***a*, e.g., CW0, CW1, to identify the three or four colors that may be specified or inferred from those codewords **390***a*.

The bitmap construction module **340** constructs a block bitmap **390***b* using the codewords **390***a* associated with the image block **260**. Colors in the image block **260** are mapped to the closest color associated with one of the quantized colors specified by, or inferred from, the codewords **390***a*. The result is a color index, referenced as ID, per pixel in the block identifying the associated quantized color.

Information indicating the block type is implied by the codewords **390***a* and the bitmap **390***b*. In a preferred embodiment, the order of the codewords **390***a* CW0, CW1, indicate the block type. If a numerical value of CW0 is greater than a numerical value of CW1, the image block is a four color block. Otherwise, the block is a three color plus transparency block.

As discussed above, in a preferred embodiment, there are two image block types. One image block type has four equidistant colors, while the other image block type has three equidistant colors with the fourth color index used to specify that a pixel is transparent. For both image block types the color index is two bits.

The output of the bitmap construction module **340** is an encoded image block **390** having the M codewords **390***a* plus the bitmap **390***b*. Each encoded image block **390** is received by the encoded image composer **319** that, in turn, orders the encoded image blocks **390** in a file. In a preferred embodiment, the encoded image blocks **390** are ordered from left to right and from top to bottom in the same order as the blocks were broken down by the block decomposer **315**. The ordered file having the encoded image blocks **390** is concatenated with the header information **385***a* that is derived from the header **380***a* of the original image **310** to generate the encoded image data **385** that is the image encoder system **220** output **320**. The image encoder system **220** output **320** may be forwarded to the memory **115**, the storage device **120**, or the output device **130**, for example.

The image encoder system **220** of the present invention advantageously reduces the effective data size of an image, for example, from 24-bits per pixel to 4-bits per pixel. Further, the present invention beneficially addresses transparency issues by allowing for codewords to be used with a transparency identifier.

FIG. **5**A is a block diagram of an image decoder system **230** in accordance with the present invention. The image decoder system **230** includes an encoded image decomposing unit **501**, a header converter **508**, one or more block decoders **505** (**505***a*–**505***m*, where m is any positive integer value representing the last block decoder), and an image composer **504**. The encoded image decomposer **501** is coupled to receive the encoded image data **385** that was output **320** from the image encoder system **220**. The encoded image decomposer **501** is coupled to the one or more block decoders **505***a*–**505***m*. The one or more block decoders **505***a*–**505***m* are coupled to the image composer **504** that, in turn, is coupled to the output **240**.

The encoded image decomposer **501** receives the encoded image data **385** and decomposes, or breaks, it into its header **385***a* and the encoded image blocks **390**-1 –**390**-R. The encoded image decomposer **501** reads the modified header **385***a* of the encoded image data **385** and forwards the modified header **385***a* to the header converter **508**. The encoded image decomposer **501** also decomposes the encoded image data **385** into the individual encoded image blocks **390**-1–**390**-R that are forwarded to the one or more block decoders **505***a*–**505***m*.

The header converter **508** converts the modified header **385***a* to an output header. Simultaneously, the encoded image blocks **390**-1–**390**-R are decompressed or decoded by the one or more block decoders **505***a*–**505***m*. It is noted that the each encoded image block **390** may be processed sequentially in one block decoder **505***a* or multiple encoded image blocks **390**-1–**390**-R may be processed in parallel with one block decoder **505***a*–**505***m* for each encoded image block **390**–**390**-R. Thus, multiple block decoders **505***a*–**505***m* allows for parallel processing that increases the processing performance and efficiency of the image decoder system **230**.

The image composer **504** receives each decoded image block from the one or more block decoders **505***a*–**505***m* and orders them in a file. Further, the image composer **504** receives the converted header from the header converter **508**. The converted header and the decoded image blocks are placed together to generate output **240** data representing the original image **310**.

FIG. **5**B is a block diagram of a first embodiment of a block decoder **505** in accordance with the present invention. Each block decoder **505***a*–**505***m* includes a block type detector **520**, one or more decoder units, e.g., **533***a*–*l* to **533***a*–*k* (k is any integer value), and an output selector **523**. The block type detector **520** is coupled to the encoded image decomposer **501**, the output selector **523**, and each of the one or more decoder units, e.g., **533***a*–*l*–**533***a*–*k*. Each of the decoder units, e.g., **533***a*–*l*–**533***a*–*k*, is coupled to the output selector **523** that, in turn, is coupled to the image composer **504**.

The block type detector **520** receives the encoded image blocks **390** and determines the block type for each encoded image block **390**. Specifically, the block type detector **520** passes a selector signal to the output selector **523** that will be used to select an output corresponding to the block type detected. The block type is detected based on the codewords **390***a*. After the block type is determined, the encoded image blocks **390** are passed to each of the decoder units, e.g., **533***a*–*l*–**533***a*–*k*. The decoder units, e.g., **533***a*–*l*–**533***a*–*k*, decompress or decode each encoded image block **390** to generate the colors for the particular encoded image block **390**. The decoder units, e.g., **533***a*–*l*–**53***a*–*k*, may be c-channels wide (one channel for each color component (or pixel property) being encoded), where c is any integer value. Using the selector signal, the block type detector **520** enables the output selector **523** to output the color of the encoded image block **390** from one of the decoder units, e.g., **533***a*–*l*–**533***a*–*k* that corresponds with the block type detected by the block type detector **520**. Alternatively, using the selector signal, the appropriate decoder unit **533** could be selected so the encoded block is processed through that decoder unit only.

FIG. **5**C is a block diagram of a second embodiment of a block decoder **505** in accordance with the present invention. In a second embodiment, the block decoder **505** includes a block type detector **520**, a first and a second decoder unit **530**, **540**, and the output selector **523**. The block type detector **520** is coupled to receive the encoded image blocks **390** and is coupled to the first and the second decoder units **530**, **540** and the output selector **523**.

The block type detector **520** receives the encoded image blocks **390** and determines, by comparing the codewords **390***a* of the encoded image block **390**, the block type for each encoded image block **390**. For example, in a preferred embodiment, the block type is four quantized colors or three quantized colors and a transparency. Once the block type is selected and a selector signal is forwarded to the output selector **523**, the encoded image blocks **390** are decoded by the first and the second decoder units **530**, **540**. The first and the second decoder units **530**, **540** decode the encoded image block **390** to produce the pixel colors of each image block. The output selector **523** is enabled by the block type detector **520** to output the colors from the decoder unit **530**, **540** that corresponds to the block type selected.

FIG. **5**D is a logic diagram illustrating one embodiment of a decoder unit through a red-channel of the that decoder unit in accordance with the present invention. Specifically, the decoder unit is similar to the decoder units **530**, **540** illustrated in FIG. **5**C. Moreover, the functionality of each of those decoder units **530**, **540** is merged into the single logic diagram illustrated in FIG. **5**D. Further, those skilled in the art will understand that although described with respect to the red-channel of the decoder units **530**, **540** the remaining channels, e.g., the green-channel and the blue-channel, in

each decoder unit **530**, **540** are similarly coupled and functionally equivalent.

The logic diagram illustrating the decoder units **530**, **540** is shown to include portions of the block type detector **520**, for example a comparator unit **522**. The comparator unit **522** works with a first 2×1 multiplexer **525***a* and a second 2×1 multiplexer **525***b*. The comparator unit **522** is coupled to the first and the second 2×1 multiplexers **525***a*, **525***b*. Both 2×1 multiplexers **525***a*, **525***b* are coupled to a 4×1 multiplexer **526** that serves to select the appropriate color to output.

The red-channel **544**, **546** of the first decoder unit **530** includes a first and a second red-channel line **551***a*, **551***b* and a first and a second red-color block **550***a*, **550***b*. Along the path of each red-color block **550***a*, **550***b* is a first full adder **552***a*, **552***b*, a second full adder **554***a*, **554***b*, and a CLA ("carry-look ahead") adder **556***a*, **556***b*. The first and the second red-channel lines **551***a*, **551***b* are coupled to the first and the second red-color blocks **550***a*, **550***b*, respectively. Each red-color block **550***a*, **550***b* is coupled to the first full adder **552***a*, **552***b* associated with that red-color block **550***a*, **550***b*. Each first full adder **552***a*, **552***b* is coupled to the respective second full adder **554***a*, **554***b*. Each second full adder **554***a*, **554***b* is coupled to the respective CLA adder **556***a*, **556***b*.

The second decoder unit **540** comprises the first and the second red-channel lines **551***a*, **551***b* and the respective first and second red-color blocks **550***a*, **550***b* and an adder **558**. The first and the second channel lines **551***a*, **551***b* are coupled to their respective red-color blocks **550***a*, **550***b* as described above. Each red-color block **550***a*, **550***b* is coupled to the adder **558**.

The CLA adder **556***a* from the path of the first red-color block **550***a* of the first decoder unit **530** is coupled to the first 2×1 multiplexer **525***a* and the CLA adder **556***b* from the path of the second red-color block **550***b* of the first decoder unit **530** is coupled to the second 2×1 multiplexer **525***b*. The adder **558** of the second decoder unit **540** is coupled to both the first and the second 2×1 multiplexers **525***a*, **525***b*.

The 4×1 multiplexer **526** is coupled to the first and the second red-channel lines **551***a*, **551***b*, as well as to the first and the second 2×1 multiplexers **525***a*, **525***b*. The 4×1 multiplexer **526** is also coupled to receive a transparency indicator signal that indicates whether or not a transparency (no color) is being sent. The 4×1 multiplexer **526** selects a color for output based on the value of the color index, referenced as the ID signal, that references the associated quantized color for an individual pixel of the encoded image block **390**.

FIG. **6**A is a flow diagram illustrating operation of the decoder system **230** in accordance with the present invention. For purposes of illustration only, the process for the decoder system **230** will be described with a single block encoder **505** having two decoding units, e.g., **530**, **540**. Those skilled in the art will recognize that the process is functionally equivalent for decoder systems having more than one block decoder **505** and more than one decoder units, e.g., **533***a–l–***533***a–k*.

The process starts **600** with the encoded image decomposer **501** receiving **605** the encoded, or compressed, image data **385** from the encoder system **220**, for example, through the memory **115** or the storage device **120**. The encoded image decomposer **501** decomposes **610** the encoded image data **385** by forwarding the modified header **385***a* to the header converter **508**. In addition, the encoded image decomposer **501** also decomposes **610** the encoded image data **385** into the individual encoded image blocks **390**-**1**–**390**-R.

The header converter **508** converts **612** the header information to generate an output header that is forwarded to the image composer **504**. Simultaneously, the one or more block decoders **505***a–***505***m* decodes **615** the pixel colors for each encoded image block **390**. It is again noted that each encoded image block **390** may be decoded **615** sequentially in one block decoder **505***a* or multiple encoded image blocks **390**-**1**–**390**-R may be decoded **615** in parallel in multiple block decoders **505***a–***505***m*, as described above. The process for decoding the encoded image blocks **390** is further described in FIG. **6**B. Each decoded **615** image block is then composed **620** into a data file with the converted **612** header information by the image composer **504**. The image composer **504** generates the data file as an output **625** that represents the original image **310**.

FIG. **6**B is a flow diagram illustrating operation of the block encoder **505** in accordance with the present invention. Once the process is started **630**, each encoded image block **390** is received by the block decoder **505** and the block type for each encoded image block **390** is detected **640**. Specifically, for a preferred embodiment the first and the second codewords **390***a*, CW**0**, CW**1**, respectively, are received **635** by the block type detector **520** of the block decoder **505**. As discussed above, comparing the numerical values of CW**0** and CW**1** reveals the block type.

In addition, the first five bits of each codeword **390***a*, e.g., CW**0**, CW**1**, that represent the red-channel color are received by the red-channel **545** of each of the first and the second decoder units **530**, **540**, the second 6-bits of each codeword **390***a* CW**0**, CW**1** that represent the green-channel color are received by the green-channel of each of the first and the second decoder units **530**, **540**, and the last 5-bits of each codeword **390***a* CW**0**, CW**1** that represent the blue-channel color are received by the blue-channel of each of the first and the second decoder units **530**, **540**.

The block type detector **520** detects **640** the block type for an encoded image block **390**. Specifically, the comparator **522** compares the first and the second codewords **390***a*, CW**0**, CW**1**, and generates a flag signal to enable the first 2×1 multiplexers **525***a* or the second 2×1 multiplexers **525***b* which, in turn, selects **645** either the first decoding unit **530** or the second decoding unit **540**, respectively. The process then calculates **650** the quantized color levels for the decoder units **530**, **540**.

To calculate **650** the quantized color levels, the first decoding unit **530** calculates the four colors associated with the two codewords **390***a*, CW**0**, CW**1**, using the following relationship:

CW**0**=first codeword=first color;

CW**1**=second codeword=second color;

CW2=third color=(⅔)CW**0**+(⅓)CW**1**;

CW3=fourth color=(⅓)CW**0**+(⅔)CW**1**.

In one embodiment, the first decoder unit **530** may estimate the above equations for CW2 and CW3, for example, as follows:

CW2=(⅝)CW**0**+(⅜)CW**1**; and

CW3=(⅜)CW**0**+(⅝)CW**1**.

The red-color blocks **550***a*, **550***b* serve as a one-bit shift register to get (½)CW**0** or (½)CW**1** and each full adder **552***a*, **552***b*, **554***a*, **554***b* also serves to shift the signal left by 1-bit. Thus, the signal from the first full adders **552***a*, **552***b* is (¼)CW**0** or (¼)CW**1**, respectively, because of a two-bit overall shift and the signal from the second full adders **554***a*, **554***b* is (⅛)CW**0** or (⅛)CW**1**, respectively, because of a three-bit overall shift. These values allow for the above approximations for the color signals.

The second decoder unit **540** calculates 650 three colors associated with the codewords **390***a*, CW0, CW1, and includes a fourth signal that indicates a transparency is being passed. The second decoder unit **540** calculates colors, for example, as:

CW0=first codeword=first color;

CW1=second codeword=second color;

CW3=third color=(½)CW0+(½)CW1; and

T=Transparency.

In one embodiment the second decoder unit **540** has no approximation because the signals received from the red-color blocks **550***a*, **550***b* is shifted left by one-bit so that the color is already calculated to (½)CW0 and (½)CW1, respectively.

After the quantized color levels for the selected **645** decoder unit **530**, **540** have been calculated **650**, each bitmap value for each pixel is read **655** from the encoded image data block **385**. As each index is read **655** it is mapped **660** to one of the four calculated colors if the first decoder unit **530** is selected **645** or one of the three colors and transparency if the second decoder unit **540** is selected. The mapped **660** colors are selected by the 4×1 multiplexer **526** based on the value of the ID signal from the bitmap **390***b* of the encoded image block **390**. As stated previously, a similar process occurs for selection of colors in the green-channel and the blue-channel.

As the colors are output from the red-, green-, and blue-channels, the output is received by the image composer **504**. The image composer **504** orders the output from the block encoders **505** in the same order as the original image **310** was decomposed. The resulting **665** image that is output from the image decoder system **230** is the original image that is forwarded to an output source **240**, e.g., a computer screen, which displays that image.

The system and method of the present invention beneficially allows for random access to any desired image block **260** within an image, and any pixel **270** within an image block **260**. FIG. **7**A is a block diagram of a subsystem **700** that provides random access to a pixel **270** or an image block **260** in accordance with the present invention.

The random access subsystem **700** includes a block address computation module **710**, a block fetching module **720**, and the one or more block decoders **505**. The block address computation module **710** is coupled to receive the header information **385***a* of the encoded image data **385**. The block address computation module **710** is also coupled to the block fetching module **720**. The block fetching module **720** is coupled to receive the encoded image block portion **390-1**-R of the encoded image data **385**. The block fetching module **720** is also coupled to the block decoders **505**.

FIG. **7**B is a flow diagram illustrating a process of random access to a pixel **270** or an image block **260** using the random access subsystem **700** in accordance with the present invention. When particular pixels **270** have been identified for decoding, the process starts **740** with the image decoder system **230** receiving the encoded image data **385**. The modified header **385***a* of the encoded image data **385** is forwarded to the block address computation module **710** and the encoded image block portion **390-1**-R of the encoded image data **385** is forwarded to the block fetching module **720**.

The block address computation module **710** reads the modified header **385***a* to compute **745** the address of the encoded image block portion **390-1**-R having the desired pixels **270**. The address computed **745** is dependent upon the pixel coordinates within an image. Using, the computed **745** address, the block fetching module **720** identifies the encoded image block **390** of the encoded image block portion **390-1**-R that has the desired pixels **270**. Once the encoded image block **390** having the desired pixels **270** has been identified, only the identified encoded image block **390** is forwarded to the block decoders **505** for processing.

Similar to the process described above in FIG. **6**B, the block decoders **505** compute **755** the quantized color levels for the identified encoded image blocks **390** having the desired pixels. After the quantized color levels have been computed **755**, the color of the desired pixel is selected **760** and output **765** from the image decoder system **230**.

Random access to pixels **270** of an image block **260** advantageously allows for selective decoding of only needed portions or sections of an image. Random access also allows the image to be decoded in any order the data is required. For example, in three-dimensional texture mapping only portions of the texture may be required and these portions will generally be required in some non-sequential order. Thus, the present invention increases processing efficiency and performance when processing only a portion or section of an image.

The present invention beneficially encodes, or compresses, the size of an original image **310** from 24-bits per pixel to an aggregate 4-bits per pixel and then decodes, or decompresses the encoded image data **385** to get a representation of the original image **310**. Further, the claimed invention uses, for example, two base points or codewords from which additional colors are derived so that extra bits are not necessary to identify a pixel **270** color.

Moreover, the present invention advantageously accomplishes the data compression on an individual block basis with the same number of bits per block so that the compression rate can remain fixed. Further, because the blocks are of fixed size with a fixed number of pixels **270**, the present invention beneficially allows for random access to any particular pixel **270** in the block. The present invention provides for an efficient use of system resources because entire blocks of data are not retrieved and decoded to display data corresponding to only a few pixels **270**.

In addition, the use of a fixed-rate 64-bit data blocks in the present invention provides the advantage of having simplified header information that allows for faster processing of individual data blocks. Also, a 64-bit data block allows for data blocks to be processed rapidly, e.g., within one-clock cycle, as the need to wait until a full data string is assembled is eliminated. Further, the present invention also reduces the microchip space necessary for a decoder system because the decoder system only needs to decode each pixel to a set of colors determined by, e.g., the two codewords.

While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and components disclosed herein and that various modifications, changes and variations which will be apparent to those skilled in the art may be made in the arrangement, operation and details of the method and apparatus of the present invention disclosed herein without departing from the spirit and scope of the invention as defined in the appended claims.

What is claimed is:

1. A system for encoding an image, comprising:

an image decomposer, coupled to receive an image, for breaking the image into one or more image blocks, each image block having a set of colors;

at least one block encoder for receiving each image block and for compressing each image block to generate an encoded image block, wherein each block encoder

includes a color quantizer for receiving each image block and for generating at least one codeword from which at least one quantized color is derived, the color quantizer having a selection module for computing a set of parameters from the set of colors, the at least one codeword derived from the set of parameters; and

an encoded image composer for receiving and ordering the encoded image blocks into a data file.

2. The system of claim 1, further comprising a header converter, coupled to the image decomposer and the encoded image composer, for receiving a header from the image, modifying the header, and outputting the modified header with the data file.

3. The system of claim 1, wherein each block encoder comprises:

a bitmap construction module for mapping the colors of an image block to one of the at least one quantized colors.

4. The system of claim 3, wherein the color quantizer further comprises:

a block type module, coupled to receive the image block, for selecting a block type for the image block; and

a codeword generation module for generating the least one codeword from the set of parameters generated by the selection module.

5. A system for decoding a compressed image, comprising:

an encoded image decomposer, coupled to receive encoded image data file having at least one compressed image block, for breaking the encoded image data file into individual compressed image blocks, each compressed image block having at least one associated codeword, each codeword generated by computing a set of parameters, partitioning the set of parameters into a plurality of partitions, and computing each codeword from one of the partitions;

at least one block decoder for decompressing the compressed image blocks into decompressed image blocks; and

an image composer for ordering the decompressed image blocks in an output file.

6. The system of claim 5, further comprising a header converter, coupled to the encoded image decomposer and the image composer, for receiving a modified header associated with the encoded image data file, generating an output header, and outputting the output header with the output file.

7. The system of claim 6, wherein each block decoder further comprises:

a block type detector for selecting a block type for each compressed image block received from the encoded image decomposer;

at least one decoder unit for decompressing each compressed image block based on the block type selected by the block type detector; and

an output selector for outputting the image block from the decoder unit in response to the block type selected by the block type detector.

8. A method for generating an encoded image of an original image having a header, comprising:

converting the header to a modified header;

decomposing the original image into image blocks, each image block having a set of colors;

encoding each image block to generate an encoded image block for each image block by computing a set of codewords from the set of colors, computing a set of computed colors using the set of codewords, and mapping each original color to one of the computed colors or one of the codewords to produce an index for each original color; and

composing the modified header and each encoded image block in a file to generate the encoded image.

9. The method of claim 8, wherein computing the set of codewords further comprises:

selecting a block type for each image block, wherein the goemetric element is computed using the block type;

partitioning the set of parameters into a plurality of partitions;

computing a set of codewords for each partition in the plurality of partitions;

computing an error for each computed set of codewords; and

outputting the block type and set of codewords producing the minimum computed error for each computed set of codewords.

10. A method for generating an original image from an encoded image including a modified header and at least one encoded image block, comprising:

receiving the encoded image data;

decomposing the encoded image into the modified header and the individual encoded image blocks;

reading the modified header to generate an output header;

decoding each individual encoded image block to generate a decoded image block, each individual encoded image block having a set of codewords and a set of indices;

calculating at least one quantized color level for the encoded image block using the set of codewords;

mapping at least one index from the set of indices to one of the calculated quantized color levels or to a codeword from the set of codewords; and

composing the output header and the individual decoded image blocks to generate an output file of the original image.

11. A system for processing any identified pixel from an encoded image data file having header information, including at least once codeword computed from a set of parameters, the set of parameters computed from a set of colors within an original image block, and an encoded image block portion including at least one encoded image block, the system comprising:

a block address computation module, coupled to receive each codeword from the header information, for computing an address of an encoded image block having the identified pixel;

a block fetching module, coupled to receive the encoded image block portion and the computed address, for fetching the encoded image block having the identified pixel; and

a block decoder, coupled to receive the fetched encoded image block, for decoding the image block to generate a quantized color associated with the identified pixel.

12. A method for processing any identified pixel of an encoded image data file having a header, including at least once codeword computed from a set of parameters, the set of parameters computed from a set of colors within an original image block, and an encoded image block portion including at least one encoded image block, the method comprising:

computing an address for an encoded image block having the identified pixel, the address computed from the at least one codeword for the encoded image block;

fetching the encoded image block using the computed address;

computing quantized color levels for the fetched encoded image block; and selecting a color of the identified pixel from the quantized color levels to output.

13. A method of compressing an original image block having a first set of color points defined within a selected color space, comprising:

fitting a geometric element to the first set of color points so that the geometric element includes a second set of color points having a minimal moment of inertia when fitted to the center of gravity of the first set of color points;

computing a set of codewords from the second set of color points;

computing a set of computed colors using the set of codewords;

mapping each of the first set of color points to one of the computed colors or one of the codewords to produce an index for each of the first set of color points; and

using the indices produced by the mapping each of the first set of color points and the set of codewords to represent the first set of color points.

14. The method of claim 13, wherein the set of parameters defines at least two color points in the selected color space.

15. The method of claim 13, further including generating an encoded image block having the set of codewords and the indices produced in mapping the first set of color points.

16. The method of claim 13, wherein mapping further includes mapping a first set color point to a predefined index, if the first set color point represents an alpha value.

17. The method of claim 13, wherein mapping further includes mapping a first set color point to a predefined index, if the first set color point represents a color key value.

18. A method of compressing an original image having a set of pixel parameters, each pixel parameter including a color point parameter defined within an RGB color space, comprising:

dividing the original image into at least one block of pixel parameters;

identifying a block type of the at least one block of pixel parameters;

computing a center of gravity for a set of color point parameters associated with the block of pixel parameters;

fitting a geometric element to the set of color point parameters associated with the block of pixel parameters so that the geometric element includes a subset of color point parameters having a minimal moment of inertia when fitted to the center of gravity;

computing a set of codewords from the subset of color point parameters;

computing a set of computed color point parameters using the set of codewords;

mapping each of the pixel parameters within the block of pixel parameters to one of the computed color point parameters or to one of the codewords to produce an index for each of the pixel parameters within the block of pixel parameters; and

representing the block of pixel parameters by using the set of codewords, and the block type, and each index produced by mapping.

19. The method of claim 18, wherein mapping further includes mapping a pixel parameter within the block of pixel parameters to a predefined index, if the pixel parameter represents a transparency identifier.

20. The method of claim 18, wherein mapping further includes mapping a pixel parameter within the block of pixel parameters to a predefined index, if the pixel parameter represents an alpha value.

21. The method of claim 18, wherein mapping further includes mapping a pixel parameter within the block of pixel parameters to a predefined index, if the pixel parameter represents a color key value.

22. A method of reducing a number of original colors in an image block to at least three different colors and a bitmap table, the method comprising:

selecting a geometric element;

fitting the geometric element to the original colors so that the geometric element includes a set of colors having a minimal moment of inertia when fitted to the center of gravity of the original colors;

computing a set of codewords from the set of colors;

computing a set of computed colors using the set of codewords; and

generating the bitmap table by mapping each original color to one of the at least three different colors.

* * * * *

Exhibit 9

US006683978B1

(12) **United States Patent**
Iourcha et al.

(10) **Patent No.: US 6,683,978 B1**
(45) **Date of Patent: Jan. 27, 2004**

(54) **FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES**

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(73) Assignee: **S3 Graphics Co., Ltd.**, Grand Cayman (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/442,114**

(22) Filed: **Nov. 17, 1999**

Related U.S. Application Data

(63) Continuation of application No. 09/351,930, filed on Jul. 12, 1999, which is a continuation of application No. 08/942,860, filed on Oct. 2, 1997, now Pat. No. 5,956,431.

(51) **Int. Cl.**[7] **G06K 9/00**

(52) **U.S. Cl.** 382/166; 382/232; 725/146

(58) **Field of Search** 382/166, 239, 382/253, 232; 345/550; 725/146; 358/462, 1.15; 348/63

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,821,208 A	*	4/1989	Ryan et al.	345/550
4,887,151 A		12/1989	Wataya	358/539
5,734,744 A		3/1998	Wittenstein et al.	382/166
5,742,892 A	*	4/1998	Chaddha	725/146
5,748,904 A		5/1998	Huang et al.	345/544
5,787,192 A		7/1998	Takaichi et al.	382/166
5,822,465 A		10/1998	Normile et al.	382/253
5,956,425 A		9/1999	Yoshida	382/234
5,956,431 A		9/1999	Iourcha et al.	382/253
6,075,619 A		6/2000	Iizuka	382/166

FOREIGN PATENT DOCUMENTS

JP	405216993	8/1993	G06F/15/70

OTHER PUBLICATIONS

A. Schilling et al., "Texram: A Smart Memory for Texturing", IEEE Computer Graphics & Applications, May 1996, 16(3), pp. 9–19.

G. Knittel et al., "Hardware and Software for Superior Texture Performance"In 10, Eurographics Hardware Workshop, Maastricht, NL, Aug. 28–29 1995, pp. 1–8.

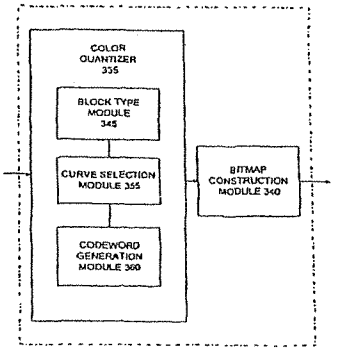
(List continued on next page.)

Primary Examiner—Anh Hong Do
(74) *Attorney, Agent, or Firm*—Carr & Ferrell LLP

(57) **ABSTRACT**

An image processing system includes an image encoder system and a image decoder system that are coupled together. The image encoder system includes a block decomposer and a block encoder that are coupled together. The block encoder includes a color quantizer and a bitmap construction module. The block decomposer breaks an original image into blocks. Each block is then processed by the block encoder. Specifically, the color quantizer selects some number of base points, or codewords, that serve as reference pixel values, such as colors, from which quantized pixel values are derived. The bitmap construction module then maps each pixel colors to one of the derived quantized colors. The codewords and bitmap are output as encoded image blocks. The decoder system includes a block decoder. The block decoder includes a block type detector, one or more decoder units, and an output selector. Using the codewords of the encoded data blocks, the comparator and the decoder units determine the quantized colors for the encoded image block and map each pixel to one of the quantized colors. The output selector outputs the appropriate color, which is ordered in an image composer with the other decoded blocks to output an image representative of the original image. A method for encoding an original image and for decoding the encoded image to generate a representation of the original image is also disclosed.

29 Claims, 16 Drawing Sheets



OTHER PUBLICATIONS

G. Campbell et al., "Two Bit/Pixel Full Color Encoding", Computer Graphics (Proc. SIGGRAPH '86), Aug. 18–22, 1986, vol. 20, No. 4, Dallas, TX, pp. 215–219.

Yang, Ching Yung et al., "Hybrid Adaptive Block Truncation Coding for Image Compression," Optical Engineering, Soc. of Photo–Optical Instrumentation Engineers, Apr. 1, 1997, p. 1021–1027, vol. 36, No. 4, Bellingham, WA, USA.

Kugler, A. "High–Performance Texture Decompression Hardware," Visual Computer, Springer–Verlag, 1997, p. 51–63, vol. 13, No. 2, Berlin, Germany.

Nasiopoulos, Panos, et al., "Adaptive Compression Coding," IEEE Transactions on Communications, IEEE Inc., Aug. 1, 1991, p. 1245–1254, vol. 39, No. 8, New York, USA.

Knittel, G. et al., "Hardware for Superior Texture Performance," Eurographics Workshop on Graphics Hardware, Jul. 28, 1995, p 33–40.

Campbell, G. et al., "Two Bit/Pixel Full Color Encoding," Computer Graphics, Aug. 1986, p. 215–219, vol. 20, No. 4, New York, New York, USA.

Delp E. J. et al., "Image Compression Using Block Truncation Coding," IEEE Transactions on Communcations, Sep. 1979, p. 1335–1342, vol. COM–27, No. 9, IEEE Inc., New York, USA.

Yang, Ching Yung et al., "Use of Radius Weighted Mean to Cluster Two–Class Data," Electronics Letters, May 12, 1994, p. 757–759, vol. 30, No. 10, IEE Stevenage, Great Britain.

Russ, J. C., "Optimal Grey Scale Images From Multiplane Color Images," Journal of Computer–Assisted Microscopy, Dec. 1995, p. 221–223, vol. 7, No. 4, Plenum, USA.

Knittel, G., et al., "Hardware and Software for Superior Texture Performance," Eurographics Hardware Wokshop '95, Aug. 28–29, 1995, pp. 1–8, Masstricht, NL.

Schilling, A., et al., "Texram: A Smart Memory for Texturing," IEEE Computer Graphics & Applications, May 1996, pp. 9–19, vol. 16, No. 3.

Feng et al., "A Dynamic Address Vector Quantization Algorithm Based on Inter–Block and Inter–Color Correction for Color Image Coding," IEEE International conference on Acoustics, Speech, and Signal Processing, May 1989, pp. 1755–1758, vol. 3.

* cited by examiner

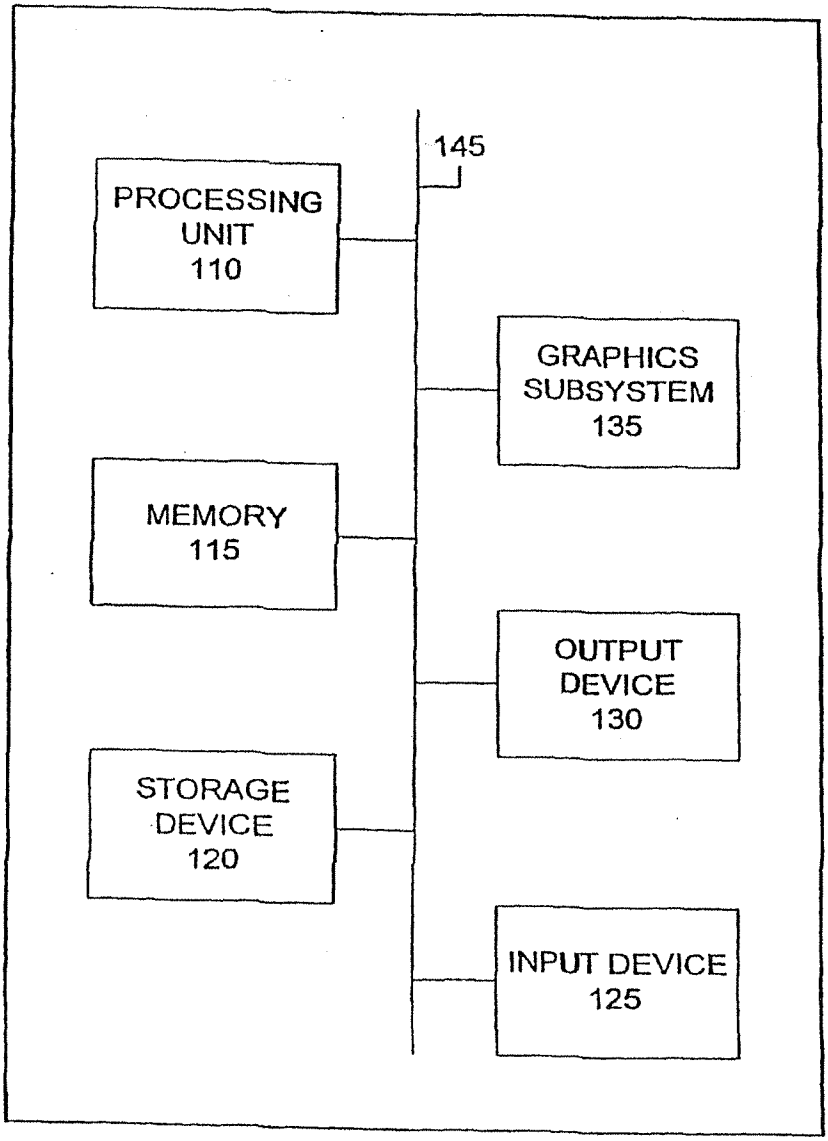


FIG. 1 105

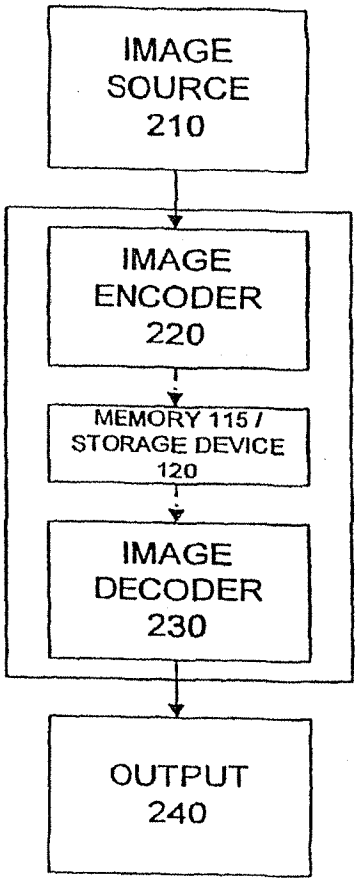


FIG. 2A

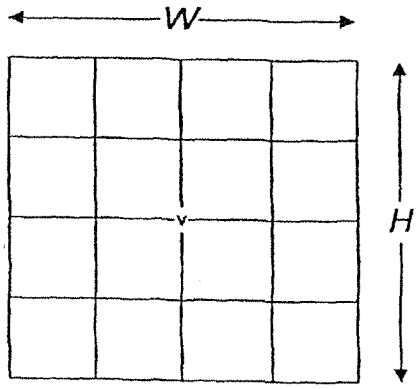


FIG. 2B

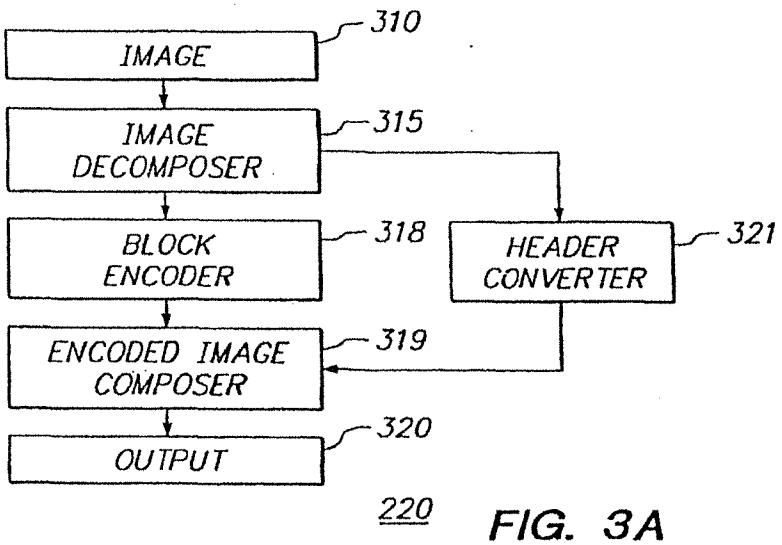


FIG. 3A

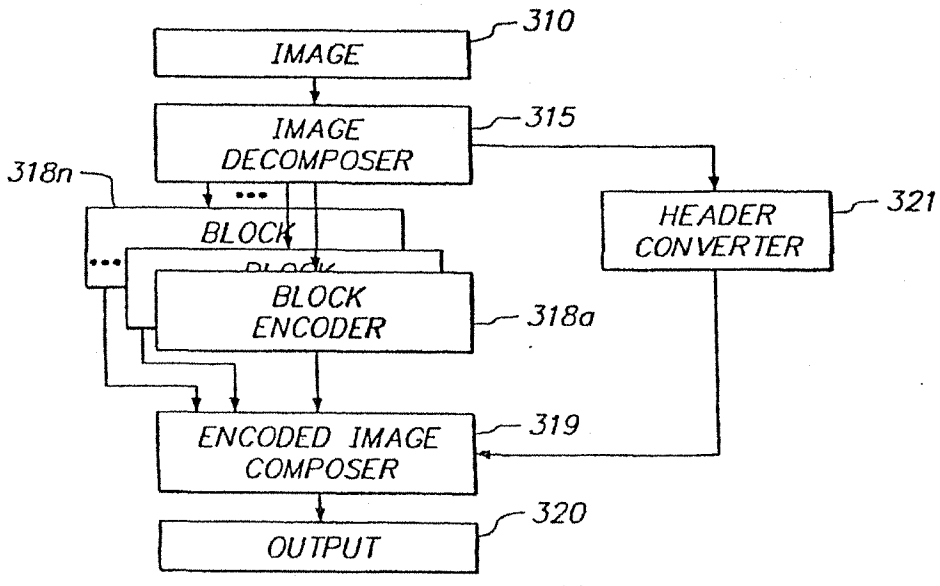


FIG. 3B

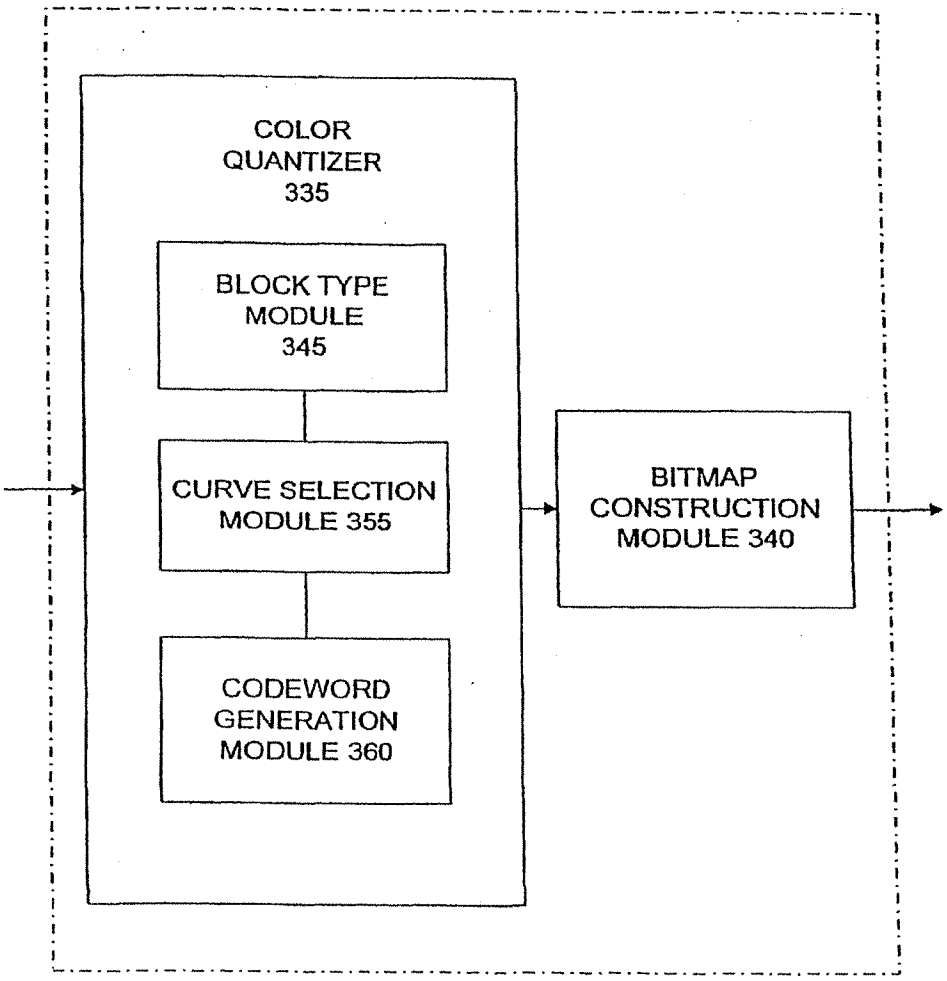


FIG. 3C

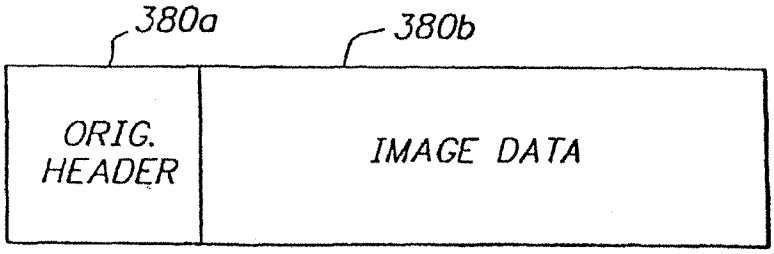


FIG. 3D

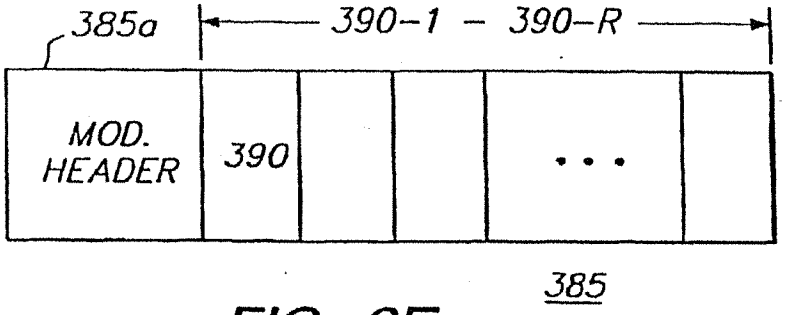


FIG. 3E

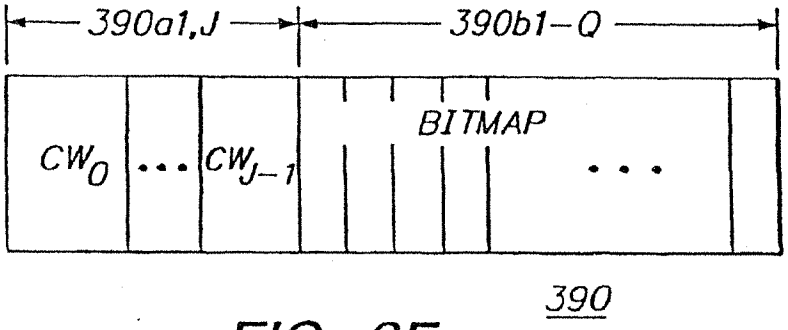


FIG. 3F

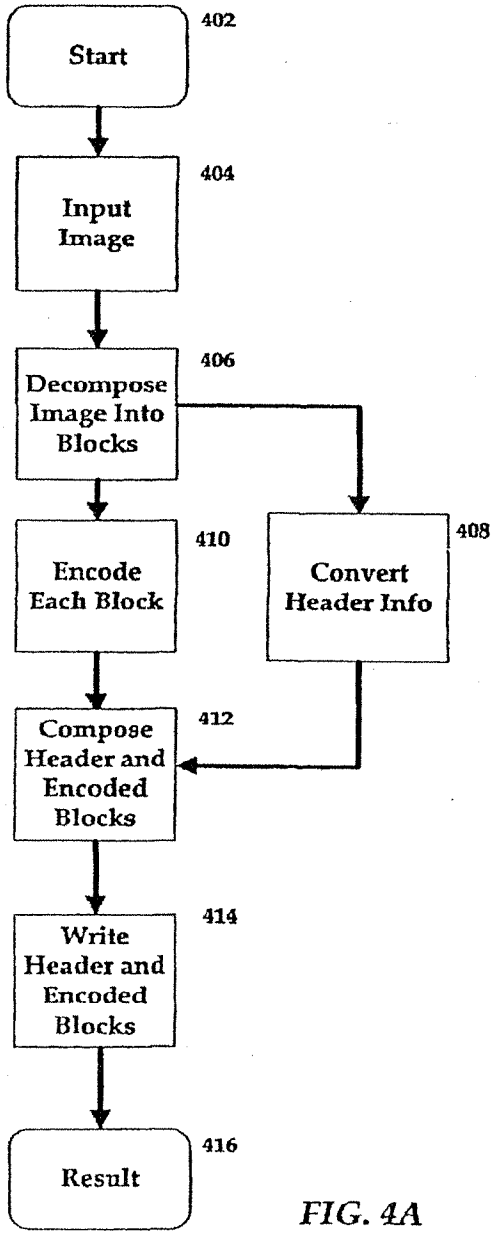


FIG. 4A

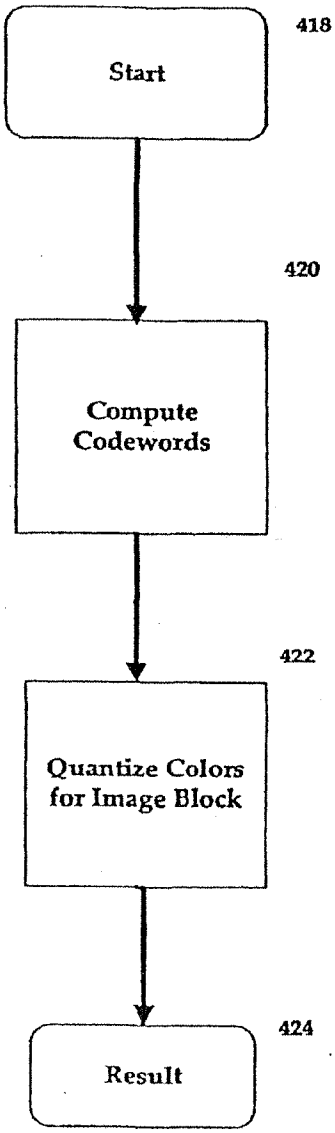


FIG. 4B

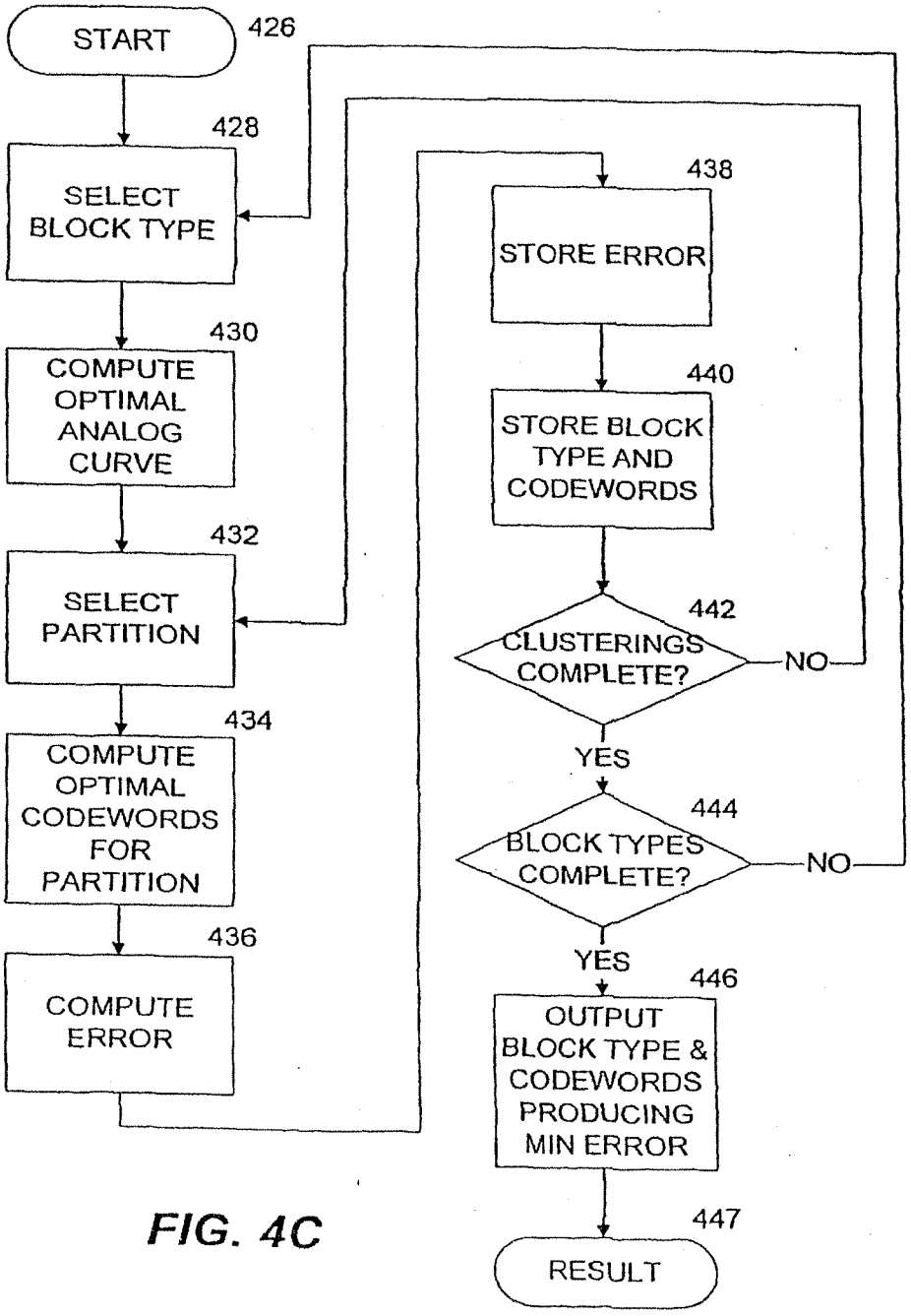


FIG. 4C

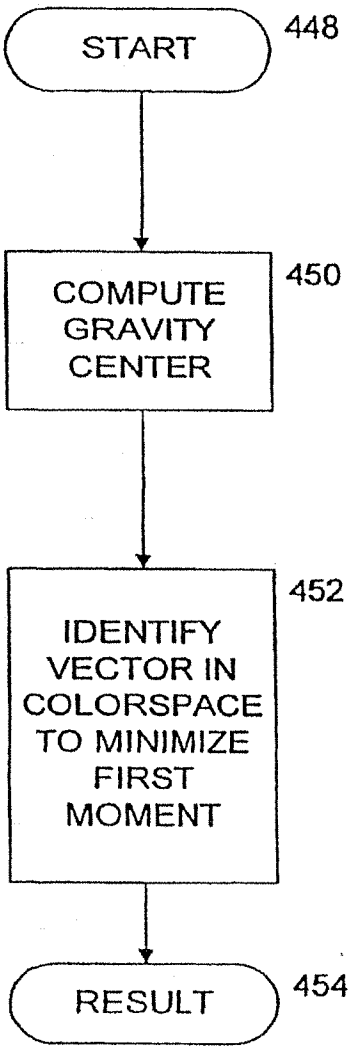


FIG. 4D

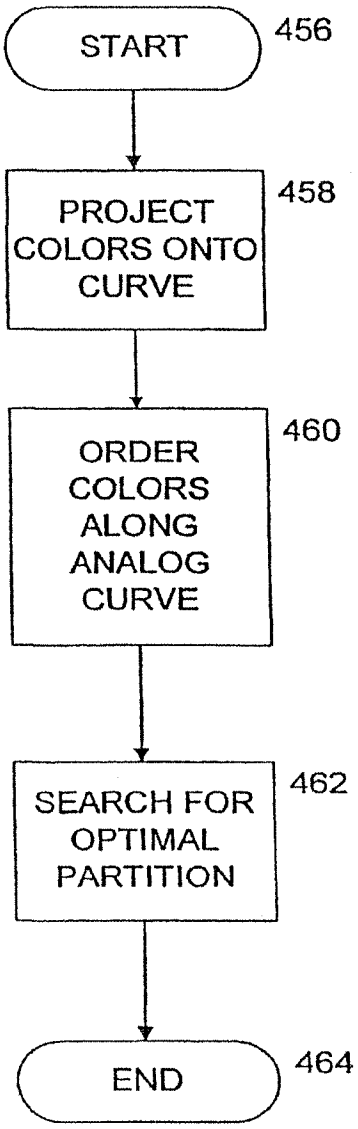


FIG. 4E

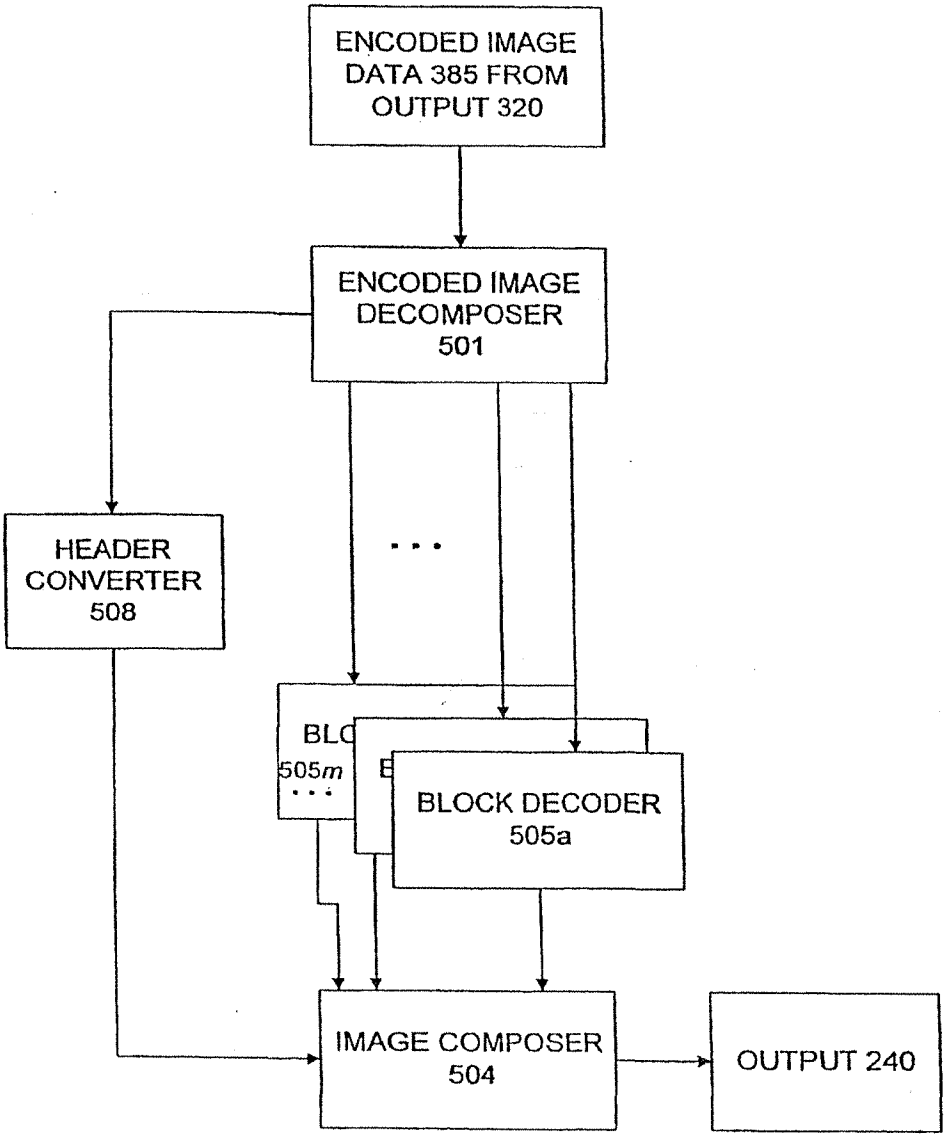


FIG. 5A

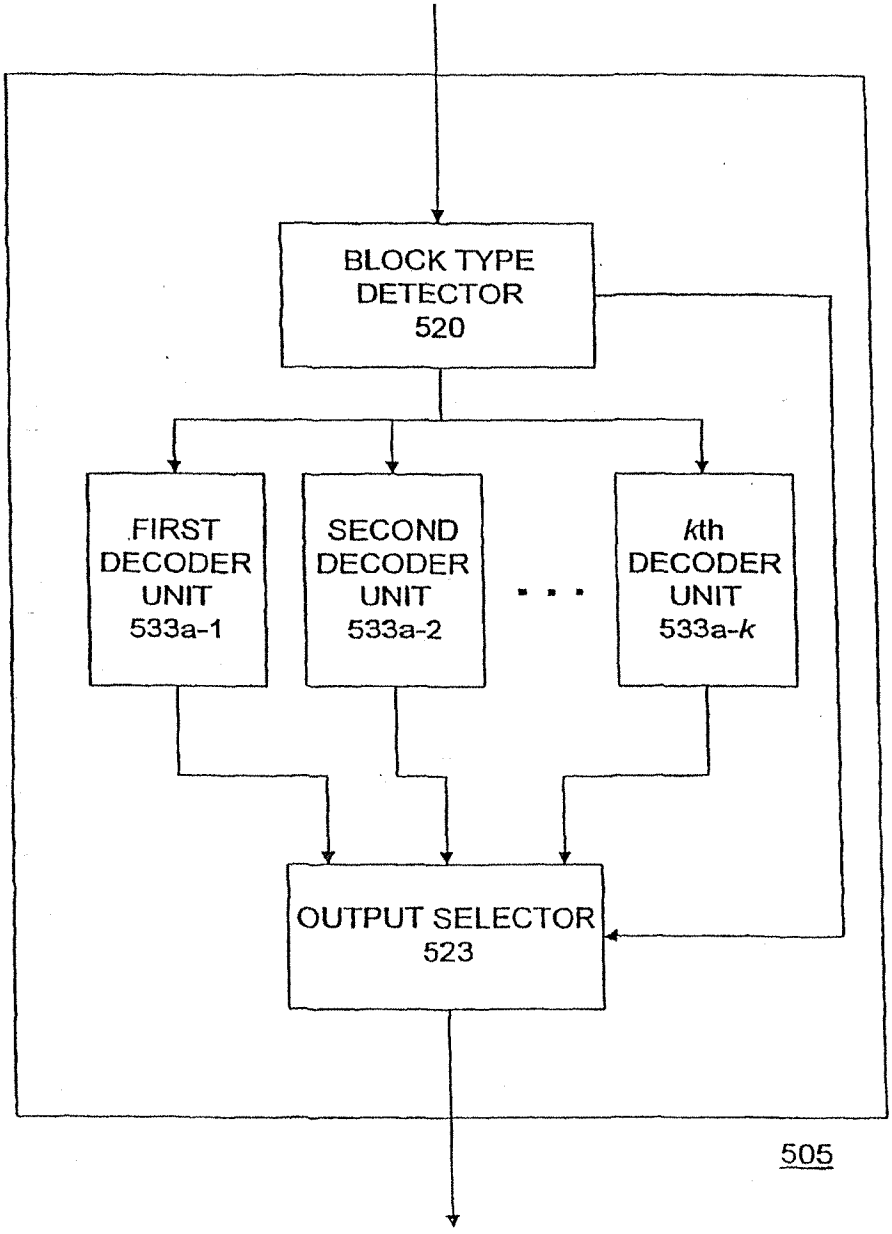


FIG. 5B

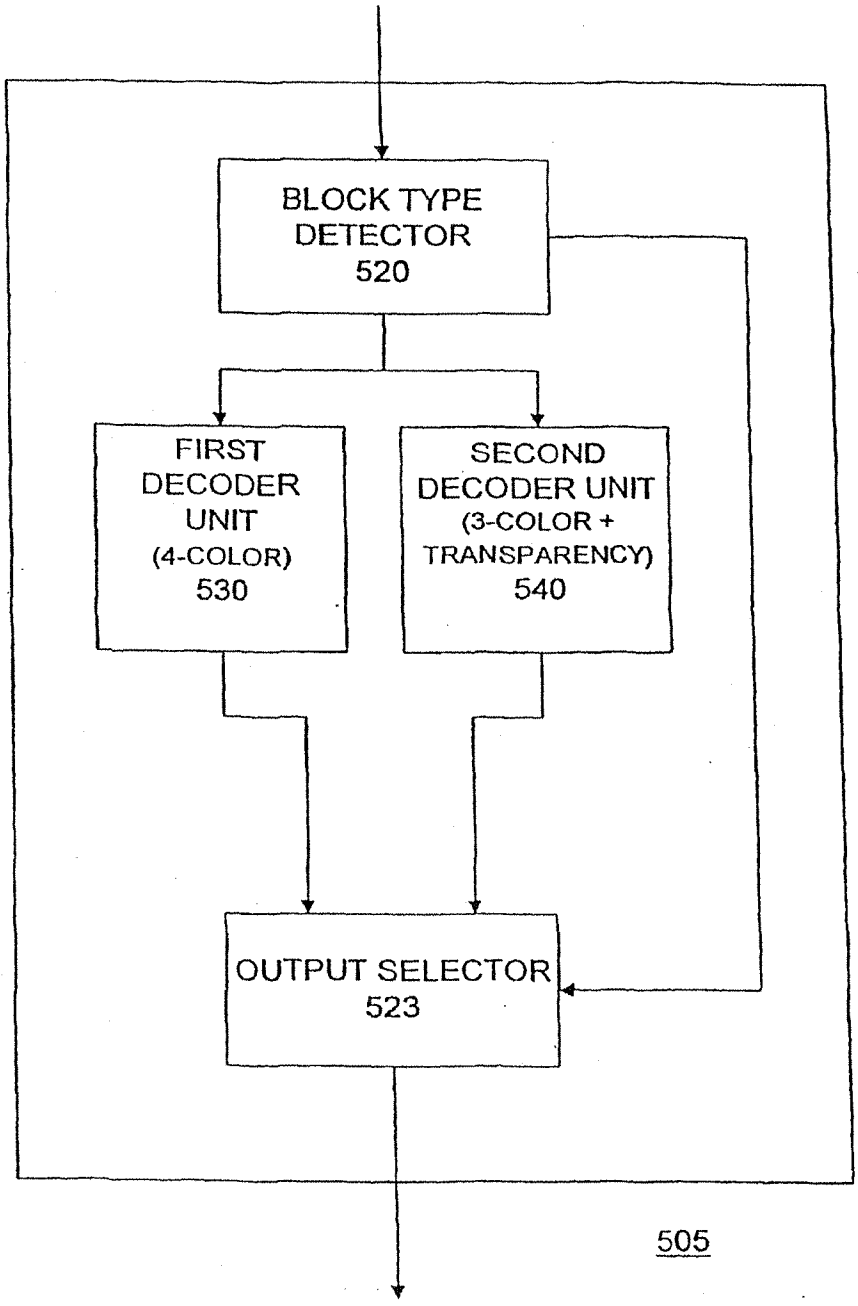


FIG. 5C

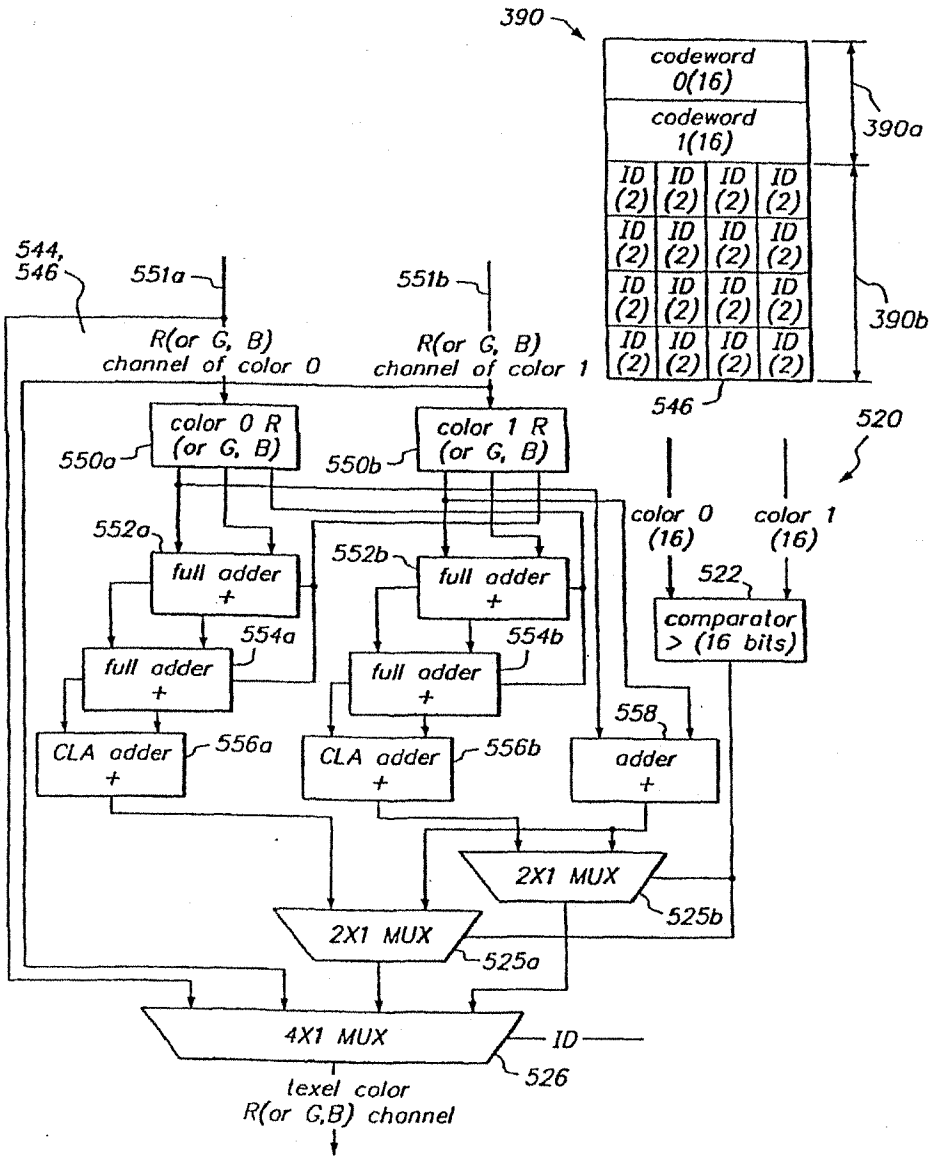


FIG. 5D

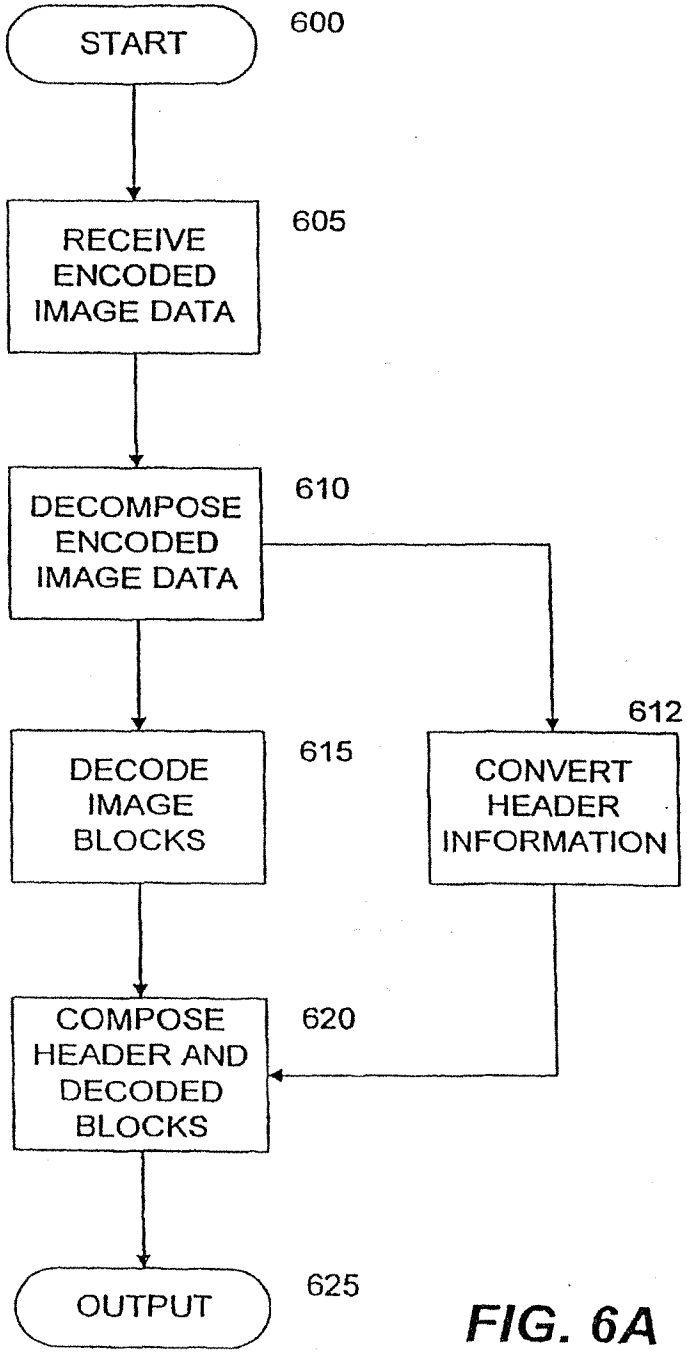


FIG. 6A

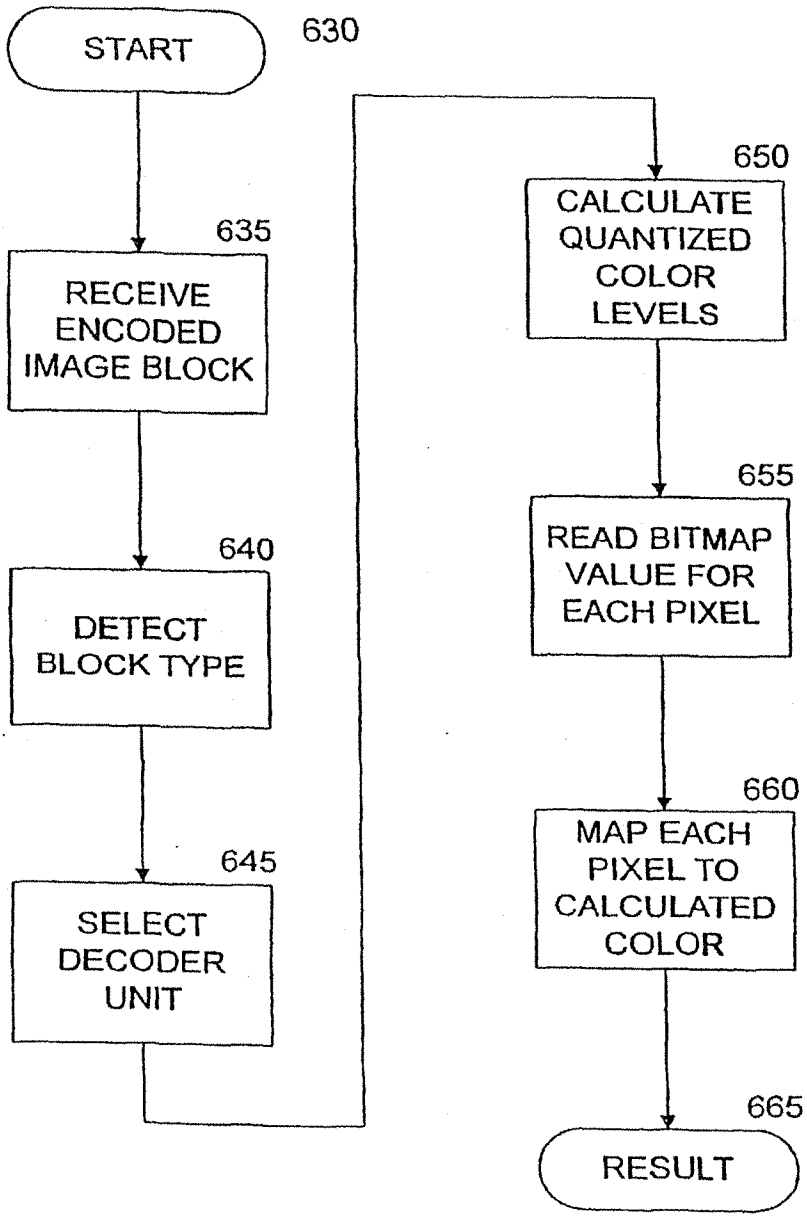


FIG. 6B

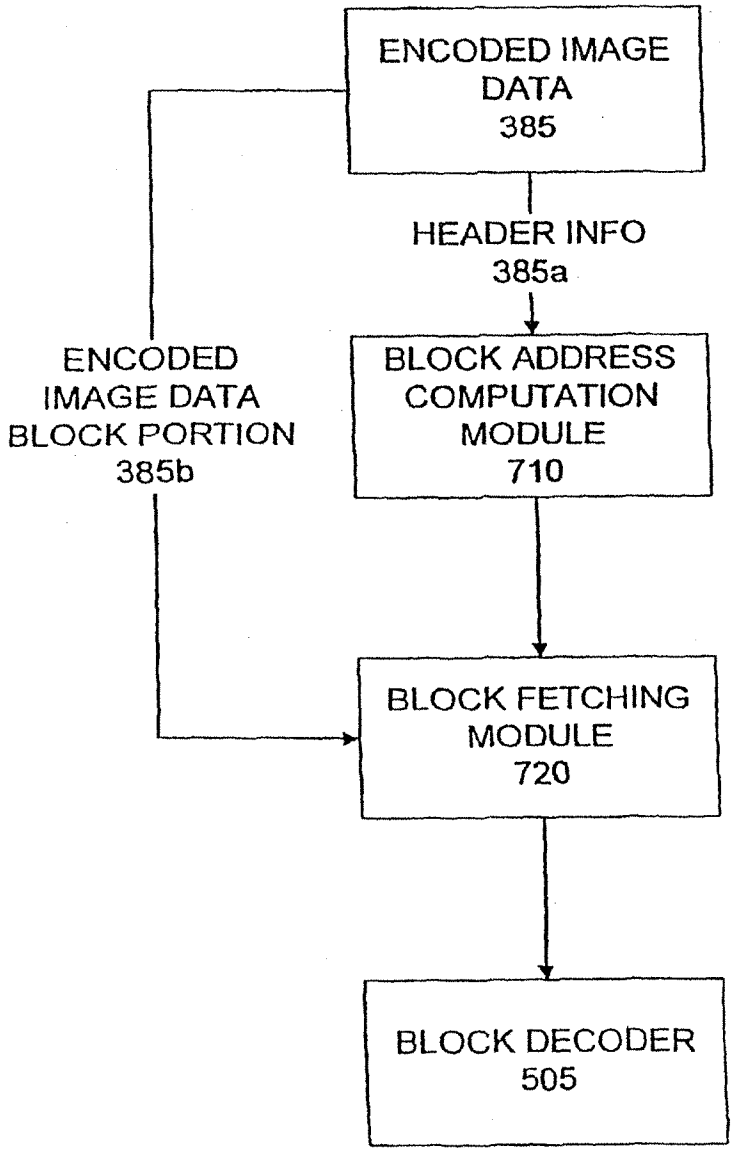


FIG. 7A

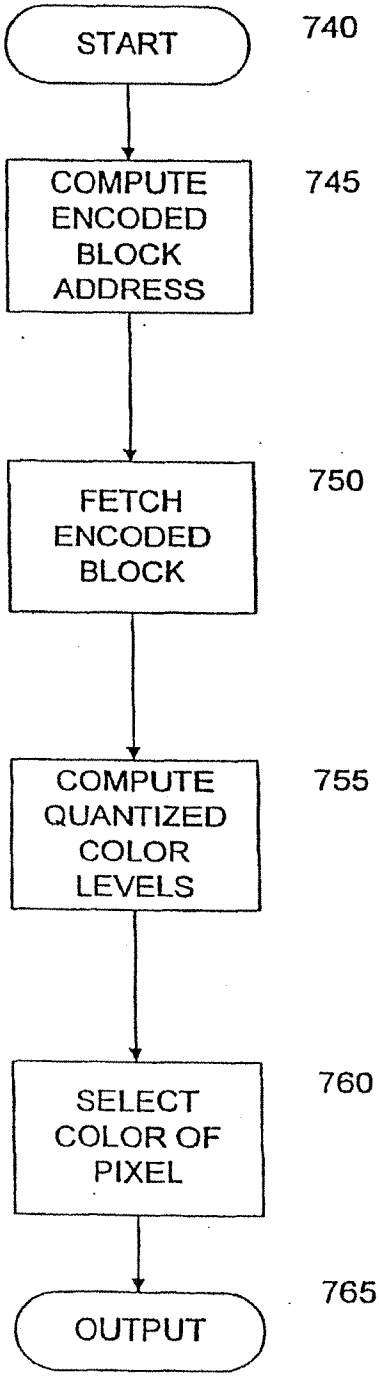


FIG. 7B

FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES

This application is a continuation of application Ser. No. 09/351,930 filed Jul. 12, 1999, which is a continuation of application Ser. No. 08/942,860 filed Oct. 2, 1997, now U.S. Pat. No. 5,956,431 issued Sep. 21, 1999.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to image processing systems, and more specifically, to three-dimensional rendering systems using fixed-rate image compression for textures.

2. Description of the Related Art

The art of generating images, such as realistic or animated graphics on a computer is known. To generate such images requires tremendous memory bandwidth and processing power on a graphics subsystem. To reduce the bandwidth and processing power requirements, various compression methods and systems were developed. These methods and systems included Entropy or lossless encoders, discrete cosine transform or JPEG type compressors, block truncation coding, color cell compression, and others. Each of these methods and systems, however, have numerous drawbacks.

Entropy or lossless encoders include Lempel-Ziv encoders and are used for many different purposes. Entropy coding relies on predictability. For data compression using Entropy encoders, a few bits are used to encode the most commonly occurring symbols. In stationary systems where the probabilities are fixed, Entropy coding provides a lower bound for the compression than can be achieved with a given alphabet of symbols. A problem with Entropy coding is that it does not allow random access to any given symbol. The part of the compressed data preceding a symbol of interest must be first fetched and decompressed to decode the symbol which takes considerable processing time and resources as well as decreasing memory throughput. Another problem with existing Entropy methods and systems is that they do not provide any guaranteed compression factor which makes this type of encoding scheme impractical where the memory size is fixed.

Discrete Cosine Transform ("DCT") or JPEG-type compressors, allow users to select a level of image quality. With DCT, uncorrelated coefficients are produced so that each coefficient can be treated independently without loss of compression efficiency. The DCT coefficients can be quantized using visually-weighted quantization values which selectively discard the least important information.

DCT, however, suffers from a number of shortcomings. One problem with DCT and JPEG-type compressors is that they require usually bigger blocks of pixels, typically 8×8 or 16×16 pixels, as a minimally accessible unit in order to obtain a reasonable compression factor and quality. Access to a very small area, or even a single pixel involves fetching a large quantity of compressed data, thus requiring increased processor power and memory bandwidth. A second problem with DCT and JPEG-type compressors is that the compression factor is variable, therefore requiring a complicated memory management system that, in turn, requires greater processor resources. A third problem with DCT and JPEG-type compression is that using a large compression factor significantly degrades image quality. For example, the image may be considerably distorted with a form of a ringing around the edges in the image as well as noticeable color shifts in areas of the image. Neither artifact can be removed with subsequent low-pass filtering.

A fourth problem with DCT and JPEG-type compression is that such a decompressor is complex and has a significant associated hardware cost. Further, the high latency of the decompressor results in a large additional hardware cost for buffering throughout the system to compensate for the latency. Finally, a fifth problem with DCT and JPEG-type compressors is that it is not clear whether a color keyed image can be compressed with such a method and system.

Block truncation coding ("BTC") and color cell compression ("CCC") use a local one-bit quantizer on 4×4 pixel blocks. The compressed data for such a block consists of only two colors and 16-bits that indicate which one of the two colors is assigned to each of the 16 pixels. Decoding a BTC/CCC image consists of using a multiplexer with a look-up table so that once a 16-texel-block (32-bits) is retrieved from memory, the individual pixels are decoded by looking up the two possible colors for that block and selecting the color according to the associated bit from the 16 decision bits.

The BTC/CCC methods quantize each block to just two color levels resulting in significant image degradation. Further, a two-bit variation of CCC stores the two colors as eight-bit indices into a 256-entry color lookup table. Thus, such pixel blocks cannot be decoded without fetching additional information that can consume additional memory bandwidth.

The BTC/CCC methods and systems can use a three-bit per pixel scheme which store the two colors as 16-bit values (not indices into a table) resulting in pixel blocks of six bytes. Fetching such units, however, decreases system performance because of additional overhead due to memory misalignment. Another problem with BTC/CCC is that when it is used to compress images that use color keying to indicate transparent pixels, there will be a high degradation of image quality.

Therefore, there is a need for a method and system that maximizes the accuracy of compressed images while minimizing storage, memory bandwidth requirements, and decoding hardware complexities, while also compressing image data blocks into convenient sizes to maintain alignment for random access to any one or more pixels.

SUMMARY OF THE INVENTION

An image processing system includes an image encoder system and an image decoder system that are coupled together. The image encoder system includes a block decomposer and a block encoder that are coupled together. The block encoder includes a color quantizer and a bitmap construction module. The block decomposer breaks an original image into image blocks, each having a plurality of pixel values (e.g. colors) or equivalent color points. Each image block is then processed by the block encoder. Specifically, the color quantizer computes some number of base points, or codewords, that serve as reference pixel values, such as colors, from which computed or quantized pixel values are derived. The bitmap construction module then maps at least one pixel value in the image block to one of the computed or quantized colors or one of the codewords. The codewords and bitmap are output as encoded image blocks.

The decoder system includes a block decoder having one or more decoder units and an output selector. The block decoder may also include a block type detector for determining the block type of an image block. The block type determines the number of computed colors to use for map-

ping each pixel color from an image block. Using the codewords of the encoded data blocks, the comparator and the decoder units determine the computed colors for the encoded image block and map each pixel to one of the computed colors. The output selector outputs the appropriate color, which is ordered in an image composer with the other decoded blocks to output an image representative of the original image.

The present invention also includes a method of compressing an original image block having a set of original colors. The method includes: computing a set of codewords from the set of original colors; computing a set of computed colors using the set of codewords; and mapping each original color to one of the computed colors or one of the codewords to produce an index for each original color.

The compressed or encoded image block, which has a first set of indices and a set of codewords, where a set is equal to or greater than one, is decoded by: computing at least one computed color using the set of codewords; and mapping an index within the first set of indices to one of the computed colors or one of the codewords.

Those of ordinary skill in the art will readily recognize that the present invention may be practiced using any general purpose computer system, such as the computer system described below, or any "hardwired" device specifically designed to perform the method, such as but not limited to devices implemented using ASIC or FPGA technology and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a data processing system in accordance with the present invention;

FIG. 2A is a block diagram of an image processing system in accordance with the present invention;

FIG. 2B is a graphical representation of an image block in accordance with the present invention;

FIG. 3A is a block diagram of a first embodiment an image encoder system in accordance with the present invention;

FIG. 3B is a block diagram of a second embodiment of an image encoder system in accordance with the present invention;

FIG. 3C is a block diagram of an image block encoder in accordance with the present invention;

FIG. 3D is a data sequence diagram of an original image in accordance with the present invention;

FIG. 3E is a data sequence diagram of encoded image data of the original image output from the image encoder system in accordance with the present invention;

FIG. 3F is a data sequence diagram of an encoded image block from the image block encoder in accordance with the present invention;

FIGS. 4A–4E are flow diagrams illustrating an encoding process in accordance with the present invention;

FIG. 5A is a block diagram of an image decoder system in accordance with the present invention;

FIG. 5B is a block diagram of a first embodiment of a block decoder in accordance with the present invention;

FIG. 5C is a block diagram of a second embodiment of a block decoder in accordance with the present invention;

FIG. 5D is a logic diagram illustrating a first embodiment of a decoder unit in accordance with the present invention;

FIGS. 6A–6B are flow diagrams illustrating a decoding process in accordance with the present invention;

FIG. 7A is a block diagram of a subsystem for random access to a pixel or an image block in accordance with the present invention; and

FIG. 7B is a flow diagram illustrating random access to a pixel or an image block in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** is a block diagram of a data processing system **105** constructed in accordance with the present invention. The data processing system **105** includes a processing unit **110**, a memory **115**, a storage device **120**, an input device **125**, an output device **130**, and a graphics subsystem **135**. In addition, the data processing system **105** includes a data bus **145** that couples each of the other components **110**, **115**, **120**, **125**, **130**, **135** of the data processing system **105**.

The data bus **145** is a conventional data bus and while shown as a single line it may be a combination of a processor bus, a PCI bus, a graphical bus, and an ISA bus. The processing unit **110** is a conventional processing unit such as the Intel Pentium processor, Sun SPARC processor, or Motorola PowerPC processor, for example. The processing unit **110** processes data within the data processing system **105**. The memory **115**, the storage device **120**, the input device **125**, and the output device **130** are also conventional components as recognized by those skilled in the art. The memory **115** and storage device **120** store data within the data processing system **105**. The input device **125** inputs data into the system while the output device **130** receives data from the data processing system **105**.

FIG. 2A is a block diagram of an image processing system **205** constructed in accordance with the present invention. In one embodiment, the image processing system **205** runs within the data processing system **105**. The image processing system **205** includes an image encoder system **220** and an image decoder system **230**. The image processing system **205** may also include a unit for producing an image source **210** from which images are received, and an output **240** to which processed images are forwarded for storage or further processing. The image encoder system **220** is coupled to receive an image from the image source **210**. The image decoder system **230** is coupled to output the image produced by the image processing system **205**. The image encoder system **220** is coupled to the image decoder system **230** through a data line and may be coupled via a storage device **120** and/or a memory **115**, for example.

Within the image encoder system **220**, the image is broken down into individual blocks and processed before being forwarded to, e.g., the storage device **140**, as compressed or encoded image data. When the encoded image data is ready for further data processing, the encoded image data is forwarded to the image decoder system **230**. The image decoder system **230** receives the encoded image data and decodes it to generate an output that is a representation of the original image that was received from the image source **210**.

FIGS. 3A and 3B are block diagrams illustrating two separate embodiments of the image encoder system **220** of the present invention. The image encoder system **220** includes an image decomposer **315**, a header converter **321**, one or more block encoders **318** (**318***a*–**318***n*, where n is the nth encoder, n being any positive integer), and an encoded image composer **319**. The image decomposer **315** is coupled to receive an original image **310** from a source, such as the image source **210**. The image decomposer **315** is also coupled to the one or more block encoders **318** and to the

header converter **321**. The header converter **321** is also coupled to the encoded image composer **319**. Each block encoder **318** is also coupled to the encoded image composer **319**. The encoded image composer **319** is coupled to the output **320**.

The image decomposer **315** receives the original image **310** and forwards information from a header of the original image **310** to the header converter **321**. The header converter **321** modifies the original header to generate a modified header, as further described below. The image decomposer **315** also breaks, or decomposes, the original image **310** into R number of image blocks, where R is some integer value. The number of image blocks an original image **310** is broken into may depend on the number of image pixels. For example, in a preferred embodiment an image **310** comprised of A image pixels by B image pixels will typically be (A/4)*(B/4) blocks, where A and B are integer values. For example, where an image is 256 pixels by 256 pixels, there will be 64×64 blocks. In other words, the image is decomposed such that each image block is 4 pixels by 4 pixels (16 pixels). Those skilled in the art will recognize that the number of pixels or the image block size may be varied, for example m×n pixels, where m and n are positive integer values.

Briefly turning to FIG. 2B, there is illustrated an example of a single image block **260** in accordance with the present invention. The image block **260** is comprised of pixels **270**. The image block **260** may be defined as an image region W pixels **270** in width by H pixels **270** in height, where W and H are integer values. In a preferred embodiment, the image block **260** is comprised of W=4 pixels **270** by H=4 pixels **270** (4×4).

Turning back to FIGS. **3A** and **3B**, each block encoder **318** receives an image block **260** from the image decomposer **315**. Each block encoder **318** encodes or compresses each image block **260** that it receives to generate an encoded or compressed image block. Each encoded image block is received by the encoded image composer **319** which orders the encoded blocks in a data file. The data file from the encoded image composer **319** is concatenated with a modified header from the header converter **321** to generate an encoded image data file that is forwarded to the output **320**. Further, it is noted that having more than one block encoder **318***a*–**318***n* allows for encoding multiple image blocks simultaneously, one image block per block encoder **318***a*–**318***n*, within the image encoder system **220** to increase image processing efficiency and performance.

The modified header and the encoded image blocks together form the encoded image data that represents the original image **310**. The function of each element of the image encoder system **220**, including the block encoder **318**, will be further described below with respect to FIGS. 4A–4E.

The original image **310** may be in any one of a variety of formats including red-green-blue ("RGB"), YUV **420**, YUV **422**, or a proprietary color space. It may be useful in some cases to convert to a different color space before encoding the original image **310**. It is noted that in one embodiment of the present invention, each image block **260** is a 4×4 set of pixels where each pixel **270** is 24-bits in size. For each pixel **270** there are 8-bits for a Red(R)-channel, 8-bits for a Green(G)-channel, and 8-bits for a Blue(B)-channel in a red-green-blue ("RGB") implementation color space. Further, each encoded image block is also a 4×4 set of pixels, but, each pixel is only 2-bits in size and has an aggregate size of 4-bits as will be further described below.

FIG. **3C** is a block diagram illustrating a block encoder **318** of the present invention in greater detail. The block encoder **318** includes a color quantizer **335** and a bitmap construction module **340**. The color quantizer **335** is coupled to the bitmap construction module **340**. Further, the color quantizer **335** further emphasizes a block type module **345**, a selection module **355**, and a codeword generation module **360**. The block type module **345** is coupled to the selection module **355**. The selection module **355** is coupled to the codeword generation module **360**.

Each image block **260** of the decomposed original image **310** is received and initially processed by the color quantizer **335** before being forwarded to the bitmap construction module **340** for further processing. The bitmap construction module **340** outputs encoded image blocks for the encoded image composer **319** to order. The bitmap construction module **340** and the color quantizer **335**, including the block type module **345**, the selection module **355**, and the codeword generation module **360**, are further discussed below in FIGS. 4A–4E.

Briefly, FIG. **3D** is a diagram of a data sequence or string **380** representing the original image **310** that is received by the block decomposer **315**. The data string **380** of the original image **310** includes an a-bit header **380***a* and a b-bit image data **380***b*, where a and b are integer values. The header **380***a* may include information such as the pixel width of the image **310**, the pixel height of the image **310**, and the format of the image **310**, e.g., the number of bits to the pixel in RGB or YUV format, for example, as well as other information. The image data is the data **380***b* representing the original image **310** itself.

FIG. **3E** is a diagram of a data sequence or string **385** representing encoded image data **385** that is generated and output **320** by the image encoder system **220**. The data string for the encoded image data **385** includes a modified header portion **385***a* and an encoded image block portion **390**-**1**–**390**-R. The modified header portion **385***a* is generated by the header converter **321** from the original header **380***a* for the original image **310**. The modified header generated by the header converter **321** includes information about file type, a number of bits per pixel of the original image **310**, addressing into the original image **310**, other miscellaneous encoding parameters, as well as the width and height information indicating the size of that original image **310**. The encoded image block portion **390**-**1**-R includes the encoded image blocks **390**-**1**–**390**-R from the block encoders **318**, where R is an integer value that is the number of blocks resulting from the decomposed original image **310**.

FIG. **3F** is a diagram of a data sequence or string **390** representing an encoded image block in accordance with the present invention. It is understood that the data string **390** representing the encoded image block may be similar to any one of the encoded image blocks **390**-**1**–**390**-R shown in the encoded image data string **385**.

The data string **390** of the encoded image block includes a codeword section **390***a* which includes J codewords, where J is an integer value, and a bitmap section **390***b*. The codeword section **390***a* includes J codewords **390***a* that are used to compute the colors indexed by the bitmap **390***b*. A codeword is a n-bit data string, where n is an integer value, that identifies a pixel property, for example a color component. In a preferred embodiment, there are two 16-bit codewords **390***a*, CW0, CW1 (J=2). The bitmap is a Q-bit data portion and is further discussed below in FIG. **4B**.

Further, in a preferred embodiment, each encoded image block is 64-bits, which includes two 16-bit codewords and

a 32-bit (4×4×2 bit) bitmap **395**. Encoding the image block **260** as described provides greater system flexibility and increased data processing efficiency as will be further discussed below.

FIGS. 4A–4E describe the operation of the image encoder system **220**. FIG. 4A describes the general operation of the image encoder system **220**. At the start **402** of operation, data string **380** of the original image **310**, that includes the a-bit header **380***a* and the b-bit image data **380***b*, is input **404** into the block decomposer **315** from the image source **210**. The block decomposer **315** decomposes **406** the original image **310** to extract the a-bit header **380***a* and it to the header converter **321**. The block decomposer also **315** decomposes, **406** the original image **310** into image blocks. Each image block **260** is independently compressed, or encoded, **410** in the one or more block encoders **318**.

The header converter **321** converts **408** the a-bit header to generate a modified header **385***a*. The modified header **385***a* is forwarded to the encoded image composer **319**. Simultaneous with the header converter **321** converting **408** the a-bit header, each image block is encoded **410** by the one or more image encoders **318***a*–**318***n* to generate the encoded image blocks **390**-1–**390**-R. Again, it is noted that each image block **260** may be processed sequentially in one block encoder **318**a or multiple image blocks **260** may be processed in parallel in multiple block encoders **318***a*–**318***n*.

The encoded image blocks **390** are output from the block encoders **318** and are placed into a predefined order by the encoded image composer **319**. In a preferred embodiment, the encoded image blocks **390** are ordered in a file from left to right and top to bottom in the same. order in which they were broken down by the block decomposer **315**. The image encoder system **220** continues by composing **412** the modified header information **385***a* from the header converter **321** and the encoded image blocks **390**. Specifically, the modified header **385***a* and the ordered encoded image blocks **390** are concatenated to generate the encoded image data file **385**. The encoded image data file **385** is written **414** as encoded output **320** to the memory **115**, the storage device **120**, or the output device **130**, for example.

FIG. 4B shows the encoding process **410** for the encoder system **220** described above in FIG. 2. At the start **418** of operation, codewords are computed **420**. As discussed above in FIG. 3F, in a preferred embodiment there are two codewords **390***a*, CW0, CW1. The process for computed codewords is further described below in FIG. 4C.

Once the codewords are computed **420** pixel values or properties, such as colors, for the image block **260** are computed or quantized **422**. Specifically, the codewords **390***a* provide points in a pixel space from which M quantized pixel values may be inferred, where M is an integer value. The M quantized pixel values are a limited subset of pixels in a pixel space that are used to represent the current image block. The process for quantizing pixel values, and more specifically colors, will be described below in FIGS. 4D and 4E. Further, it is noted that the embodiments will now be described with respect to colors of a pixel value although one skilled in the art will recognize that in general any pixel value may be used with respect to the present invention.

In a preferred embodiment, each pixel is encoded with two bits of data which can index one of M quantized colors (M=4). Further, in a preferred embodiment the four quantized colors are derived from the two codewords **390***a* where two colors are the codewords themselves and the other two colors are inferred from the codewords, as will be described below. It is also possible to use the codewords **390***a* so that there is one index to indicate a transparent color and three indices to indicate colors, of which one color is inferred.

In a preferred embodiment, the bitmap **390***b* is a 32-bit data string.

The bitmap **390***b* and codewords **390***a* are output **424** as a 64-bit data string representing an encoded image block **390**. Specifically, the encoded image block **390** includes the two 16-bit codewords **390***a* (n=16) and a 32-bit bitmap **390***b*. Each codeword **390***a* CW**0**, CW**1** that is a 16-bit data string includes a 5-bit red-channel, 6-bit green-channel, and 5-bit blue-channel.

Each of the encoded image blocks **390** is placed together **390***a***1**–**390***a*R, and concatenated with header information **385***a* derived from the original header **380***a* of the original image **310**. The resulting **424** output is the encoded image data **385** representing the original image **310**.

FIG. 4C describes the process for computing the codewords for the image blocks **260** in more detail. At the start **426** of the process, the color quantizer **335** uses the block type module **345** to select **428** the first block type for the image block **260** that is being processed. For example, one block type selected **428** may be a four-color and another block type selected **428** may be a three-color plus transparency, where the colors within the particular block type have equidistant spacing in a color space.

Those of ordinary skill in the art will readily recognize that selecting a block type for each image is not intended to be limiting in any way Instead, the present invention may be limited to processing image blocks that are of a single block type. This eliminates the need to distinguish between different block types, such as the three and four color block types discussed above. Consequently, the block type module **345** in FIG. 3B and reference number **428** in FIG. 4C are optional and are not intended to limit the present invention in any way.

Once the block type is selected **428**, the process computes **430** an optimal analog curve for the block type. Computation **430** of the optimal analog curve **430** will be further described below in FIG. 4D. The analog curve is used to simplify quantizing of the colors in the image block. After computing **430** the optimal analog curve, the process selects **432** a partition of the points along the analog curve. A partition may be defined as a grouping of indices {1 . . . (W×H)} into M nonintersecting sets. In a preferred embodiment, the indices (1 . . . 16) are divided into three or four groups, or clusters, (M=3 or 4) depending on the block type.

Once a partition is selected **432**, the optimal codewords for that particular partition are computed **434**. Computation **434** of the optimal codewords is further described below in FIG. 4E. In addition to computing **434** the codewords, an error value (squared error as describe below) for the codewords is also computed **436**. Computation **436** of the error values is further described below with respect to FIG. 4E also. If the computed **436** error value is the first error value it is stored. Otherwise, the computed **436** error value is stored **438** only if it is less than the previously stored error value. For each stored **438** error value, the corresponding block type and codewords are also stored **440**. It is noted that the process seeks to find the block type and codewords that minimize the error function.

The process continues by determining **442** if the all the possible partitions are complete. If there are more partitions possible, the process selects **432** the next partition and once again computes **434** the codewords, computes **436** the

associated error value, and stores **438** the error value and stores **440** associated block type and codewords only if the error value is less than the previously stored error value.

After all the possible partitions are completed, the process determines **444** whether all the block types have been selected. If there are more block types, the process selects **428** the next block type. Once again, the process will compute **430** the optimal analog curve, select **432**, **442** all the possible partitions, for each partition it will compute **434**, **436** the codewords and associated error value, and store **438**, **440** the error value and associated block type and codeword only if the error value is less than the previously stored error value. After the last block type is processed, the process outputs **446** a result **447** of the block type and codewords **390***a* having the minimum error.

In an alternative embodiment, the optimal analog curve may be computed **430** before searching the block type. That is, the process may compute **430** the optimal analog curve before proceeding with selecting **428** the block type, selecting **432** the partition, computing **434** the codewords, computing **436** the error, storing **438** the error, and storing **440** the block type and codeword. Computing **430** the optimal analog curve first is useful if all the, block types use the same analog curve and color space because the analog curve does not need to be recomputed for each block type.

FIG. **4D** further describes the process of identifying the optimal analog curve. The selection module **355** starts **448** the process by computing a center of gravity **450** for pixel **270** colors of an image block **260**. Computing **450** the center of gravity includes averaging the pixel **270** colors of the image block **260**. Once the center of gravity is computed **450**, the process identifies **452** a vector in color space to minimize the first moment of the pixel **270** colors of the image block **260**.

Specifically, for identifying **452** the vector the process fits a straight line to a set of data points, which are the original pixel **270** colors of the image block **260**. A straight line is chosen passing through the center of gravity of the set of points such that it minimizes the "moment of inertia" (the means square error). For example, for three pixel properties, to compute the direction of the line minimizing the moment of inertia, tensor inertia, T, is calculated from the individual colors as follows:

$$T = \sum_i \begin{matrix} C_{1i}^2 + C_{2i}^2 & -C_{0i}C_{1i} & -C_{0i}C_{2i} \\ -C_{0i}C_{1i} & C_{0i}^2 + C_{2i}^2 & -C_{1i}C_{2i} \\ -C_{0i}C_{2i} & -C_{2i}C_{1i} & C_{0i}^2 + C_{1i}^2 \end{matrix}$$

where C_0, C_1, and C_2 represent pixel properties, for example color components in RGB or YUV, relative to a center of gravity. In a preferred embodiment of an RGB color space, C_{0i} is the value of red, C_{1i} is the value of green, and C_{2i} is the value of blue for each pixel, i, of the image block. Further, i takes on integer values from 1 to W×H, so that if W=4 and H=4, i ranges from 1 to 16.

The eigenvector of tensor, T, with the smallest eigenvalue is calculated using conventional methods known to those skilled in the art. The eigenvector direction along with the calculated gravity center, defines the axis that minimizes the moment of inertia. This axis is used as the optimal analog curve, which in a preferred embodiment is a straight line. Those of ordinary skill in the art will readily recognize that the term optimal analog curve is not limited solely to a straight line but may include a set of parameters, such as pixel values or colors, that minimizes the moment of inertia or means square error when fitted to the center of gravity of the pixel colors in the image block. The set of parameters may define any geometric element, such as but not limited to a curve, a plane, a trapezoid, or the like.

FIG. **4E** illustrates the process undertaken by the codeword generation module **360** for selecting **432** the partitions, computing **434**, **436** the codewords for the partitions and the associated error, and storing **438**, **440** the error value, block type, and codeword if the error value is less than a previously stored error value. The process starts **456** with the codeword generation module **360** projecting **458** the W×H color values onto the previously constructed optimal analog curve. The value of W×H is the size in number of pixels **270** of an image block **260**. In a preferred embodiment, where W and H are both 4 pixels, W×H is 16 pixels.

Once the colors are projected **458** onto the analog curve, the colors are ordered **460** sequentially along that analog curve based on the position of the color on the one-dimensional analog curve. After the colors are ordered **460**, the codeword generation module **360** searches **462** for optimal partitions. That is, the codeword generation module **360** takes the W×H colors (one color associated with each pixel) that are ordered **460** along the analog curve and partitions, or groups, them into a finite number of clusters with a predefined relative spacing. In a preferred embodiment, where W=4 and H=4, so that W×H is 16, the 16 colors are placed in three or four clusters (M=3 or 4).

In conducting the search **462** for the optimal partition, the color selection module **360** finds the best M clusters for the W×H points projected onto the optimal curve, so that the error associated with the selection is minimized. The best M clusters are determined by minimizing the mean square error with the constraint that the points associated with each cluster are spaced to conform to the predefined spacing.

In a preferred embodiment, for a block type of four equidistant colors, the error may be defined as a squared error along the analog curve, such as

$$E^2=\Sigma_{cluster0}(x_i-p_0)^2+\Sigma_{cluster1}(x_i-((\tfrac{2}{3})p_0+((\tfrac{1}{3})p_1))^2+\Sigma_{cluster2}(x_i-((\tfrac{1}{3})p_0+(\tfrac{2}{3})p_1))^2+\Sigma_{cluster3}(x_i-p_1)^2$$

where E is the error for the particular grouping or clustering, p_0 and p_1 are the coded colors, and x_i are the projected points on the optimal analog curve.

In instances where the block type indicates three equidistant colors, the error may be defined as a squared error along the analog curve, such as

$$E^2=\Sigma_{cluster0}(x_i-p_0)^2+\Sigma_{cluster1}(x_i-((\tfrac{1}{2})p_0+(\tfrac{1}{2})p_1))^2+\Sigma_{cluster2}(x_i-p_1)^2$$

where, again, E is the error for the particular grouping or clustering, p_0 and p_1 are the coded colors, and x_i are the projected points on the optimal analog curve.

After the resulting **447** optimal codewords **390***a* are identified, they are forwarded to the bitmap construction module **340**. The bitmap construction module **340** uses the codewords **390***a* to identify the M colors that may be specified or inferred from those codewords **390***a*. In a preferred embodiment, the bitmap construction module **340** uses the codewords **390***a*, e.g., **CW0**, **CW1**, to identify the three or four colors that may be specified or inferred from those codewords **390***a*.

The bitmap construction module **340** constructs a block bitmap **390***b* using the codewords **390***a* associated with the image block **260**. Colors in the image block **260** are mapped to the closest color associated with one of the quantized colors specified by, or inferred from, the codewords **390***a*.

The result is a color index, referenced as ID, per pixel in the block identifying the associated quantized color.

Information indicating the block type is implied by the codewords **390***a* and the bitmap **390***b*. In a preferred embodiment, the order of the codewords **390***a* CW0, CW1, indicate the block type. If a numerical value of CW0 is greater than a numerical value of CW1, the image block is a four color block. Otherwise, the block is a three color plus transparency block.

As discussed above, in a preferred embodiment, there are two image block types. One image block type has four equidistant colors, while the other image block type has three equidistant colors with the fourth color index used to specify that a pixel is transparent. For both image block types the color index is two bits.

The output of the bitmap construction module **340** is an encoded image block **390** having the M codewords **390***a* plus the bitmap **390***b*. Each encoded image block **390** is received by the encoded image composer **319** that, in turn, orders the encoded image blocks **390** in a file. In a preferred embodiment, the encoded image blocks **390** are ordered from left to right and from top to bottom in the same order as the blocks were broken down by the block decomposer **315**. The ordered file having the encoded image blocks **390** is concatenated with the header information **385***a* that is derived from the header **380***a* of the original image **310** to generate the encoded image data **385** that is the image encoder system **220** output **320**. The image encoder system **220** output **320** may be forwarded to the memory **115**, the storage device **120**, or the output device **130**, for example.

The image encoder system **220** of the present invention advantageously reduces the effective data size of an image, for example, from 24-bits per pixel to 4-bits per pixel. Further, the present invention beneficially addresses transparency issues by allowing for codewords to be used with a transparency identifier.

FIG. **5**A is a block diagram of an image decoder system **230** in accordance with the present invention. The image decoder system **230** includes an encoded image decomposing unit **501**, a header converter **508**, one or more block decoders **505** (**505***a*–**505***m*, where m is any positive integer value representing the last block decoder), and an image composer **504**. The encoded image decomposer **501** is coupled to receive the encoded image data **385** that was output **320** from the image encoder system **220**. The encoded image decomposer **501** is coupled to the one or more block decoders **505***a*–**505***m*. The one or more block decoders **505***a*–**505***m* are coupled to the image composer **504** that, in turn, is coupled to the output [240].

The encoded image decomposer **501** receives the encoded image data **385** and decomposes, or breaks, it into its header **385***a* and the encoded image blocks **390-1**–**390-R**. The encoded image decomposer **501** reads the modified header **385***a* of the encoded image data **385** and forwards the modified header **385***a* to the header converter **508**. The encoded image decomposer **501** also decomposes the encoded image data **385** into the individual encoded image blocks **390-1**–**390-R** that are forwarded to the one or more block decoders **505***a*–**505***m*.

The header converter **508** converts the modified header **385***a* to an output header. Simultaneously, the encoded image blocks **390-1**–**390-R** are decompressed or decoded by the one or more block decoders **505***a*–**505***m*. It is noted that the each encoded image block **390** may be processed sequentially in one block decoder **505***a* or multiple encoded image blocks **390-1**–**390-R** may be processed in parallel with one block decoder **505***a*–**505***m* for each encoded image block **390-1**–**390-R**. Thus, multiple block decoders **505***a*–**505***m* allows for parallel processing that increases the processing performance and efficiency of the image decoder system **230**.

The image composer **504** receives each decoded image block from the one or more block decoders **505***a*–**505***m* and orders them in a file. Further, the image composer **504** receives the converted header from the header converter **508**. The converted header and the decoded image blocks are placed together to generate output **240** data representing the original image **310**.

FIG. **5**B is a block diagram of a first embodiment of a block decoder **505** in accordance with the present invention. Each block decoder **505***a*–**505***m* includes a block type detector **520**, one or more decoder units, e.g., **533***a*-**1** to **533***a*-k (k is any integer value), and an output selector **523**. The block type detector **520** is coupled to the encoded image decomposer **501**, the output selector **523**, and each of the one or more decoder units, e.g., **533***a*-**1**–**533***a*-k. Each of the decoder units, e.g., **533***a*-**1**–**533***a*-k, is coupled to the output selector **523** that, in turn, is coupled to the image composer **504**.

The block type detector **520** receives the encoded image blocks **390** and determines the block type for each encoded image block **390**. Specifically, the block type detector **520** passes a selector signal to the output selector **523** that will be used to select an output corresponding to the block type detected. The block type is detected based on the codewords **390***a*. After the block type is determined, the encoded image blocks **390** are passed to each of the decoder units, e.g., **533***a*-**1**–**533***a*-k The decoder units, e.g., **533***a*-**1**–**533***a*-k, decompress or decode each encoded image block **390** to generate the colors for the particular encoded image block **390**. The decoder units, e.g., **533***a*-**1**–**533***a*-k, may be c-channels wide (one channel for each color component (or pixel property) being encoded), where c is any integer value. Using the selector signal, the block type detector **520** enables the output selector **523** to output the color of the encoded image block **390** from one of the decoder units, e.g., **533***a*-**1**–**533***a*-k that corresponds with the block type detected by the block type detector **520**. Alternatively, using the selector signal, the appropriate decoder unit **533** could be selected so the encoded block is processed through that decoder unit only.

FIG. **5**C is a block diagram of a second embodiment of a block decoder **505** in accordance with the present invention. In a second embodiment, the block decoder **505** includes a block type detector **520**, a first and a second decoder unit **530**, **540**, and the output selector **523**. The block type detector **520** is coupled to receive the encoded image blocks **390** and is coupled to the first and the second decoder units **530**, **540** and the output selector **523**.

The block type detector **520** receives the encoded image blocks **390** and determines, by comparing the codewords **390***a* of the encoded image block **390**, the block type for each encoded image block **390**. For example, in a preferred embodiment, the block type is four quantized colors or three quantized colors and a transparency. Once the block type is selected and a selector signal is forwarded to the output selector **523**, the encoded image blocks **390** are decoded by the first and the second decoder units **530**, **540**. The first and the second decoder units **530**, **540** decode the encoded image block **390** to produce the pixel colors of each image block. The output selector **523** is enabled by the block type detector **520** to output the colors from the decoder unit **530**, **540** that corresponds to the block type selected.

FIG. **5**D is a logic diagram illustrating one embodiment of a decoder unit through a red-channel of the that decoder unit

in accordance with the present invention. Specifically, the decoder unit is similar to the decoder units **530**, **540** illustrated in FIG. 5C. Moreover, the functionality of each of those decoder units **530**, **540** is merged into the single logic diagram illustrated in FIG. 5D. Further, those skilled in the art will understand that although described with respect to the red-channel of the decoder units **530**, **540** the remaining channels, e.g., the green-channel and the blue-channel, in each decoder unit **530**, **540** are similarly coupled and functionally equivalent.

The logic diagram illustrating the decoder units **530**, **540** is shown to include portions of the block type detector **520**, for example a comparator unit **522**. The comparator unit **522** works with a first 2×1 multiplexer **525***a* and a second 2×1 multiplexer **525***b*. The comparator unit **522** is coupled to the first and the second 2×1 multiplexers **525***a*, **525***b*. Both 2×1 multiplexers **525***a*, **525***b* are coupled to a 4×1 multiplexer **526** that serves to select the appropriate color to output.

The red-channel **544**, **546** of the first decoder unit **530** includes a first and a second red-channel line **551***a*, **551***b* and a first and a second red-color block **550***a*, **550***b*. Along the path of each red-color block **550***a*, **550***b* is a first full adder **552***a*, **552***b*, a second full adder **554***a*, **554***b*, and a CLA ("carry-look ahead") adder **556***a*, **556***b*. The first and the second red-channel lines **551***a*, **551***b* are coupled to the first and the second red-color blocks **550***a*, **550***b*, respectively. Each red-color block **550***a*, **550***b* is coupled to the first full adder **552***a*, **552***b* associated with that red-color block **550***a*, **550***b*. Each first full adder **552***a*, **552***b* is coupled to the respective second full adder **554***a*, **554***b*. Each second full adder **554***a*, **554***b* is coupled to the respective CLA adder **556***a*, **556***b*.

The second decoder unit **540** comprises the first and the second red-channel lines **551***a*, **551***b* and the respective first and second red-color blocks **550***a*, **550***b* and an adder **558**. The first and the second channel lines **551***a*, **551***b* are coupled to their respective red-color blocks **550***a*, **550***b* as described above. Each red-color block **550***a*, **550***b* is coupled to the adder **558**.

The CLA adder **556***a* from the path of the first red-color block **550***a* of the first decoder unit **530** is coupled to the first 2×1 multiplexer **525***a* and the CLA adder **556***b* from the path of the second red-color block **550***b* of the first decoder unit **530** is coupled to the second 2×1 multiplexer **525***b*. The adder **558** of the second decoder unit **540** is coupled to both the first and the second 2×1 multiplexers **525***a*, **525***b*.

The 4×1 multiplexer **526** is coupled to the first and the second red-channel lines **551***a*, **551***b*, as well as to the first and the second 2×1 multiplexers **525***a*, **525***b*. The 4×1 multiplexer **526** is also coupled to receive a transparency indicator signal that indicates whether or not a transparency (no color) is being sent. The 4×1 multiplexer **526** selects a color for output based on the value of the color index, referenced as the ID signal, that references the associated quantized color for an individual pixel of the encoded image block **390**.

FIG. 6A is a flow diagram illustrating operation of the decoder system **230** in accordance with the present invention. For purposes of illustration only, the process for the decoder system **230** will be described with a single block encoder **505** having two decoding units, e.g., **530**, **540**. Those skilled in the art will recognize that the process is functionally equivalent for decoder systems having more than one block decoder **505** and more than one decoder units, e.g., **533***a*-1–**533***a*-k.

The process starts **600** with the encoded image decomposer **501** receiving **605** the encoded, or compressed, image data **385** from the encoder system **220**, for example, through the memory **115** or the storage device **120**. The encoded image decomposer **501** decomposes **610** the encoded image data **385** by forwarding the modified header **385***a* to the header converter **508**. In addition, the encoded image decomposer **501** also decomposes **610** the encoded image data **385** into the individual encoded image blocks **390**-1–**390**-R.

The header converter **508** converts **612** the header information to generate an output header that is forwarded to the image composer **504**. Simultaneously, the one or more block decoders **505***a*–**505***m* decodes **615** the pixel colors for each encoded image block **390**. It is again noted that each encoded image block **390** may be decoded **615** sequentially in one block decoder **505***a* or multiple encoded image blocks **390**-1–**390**-R may be PATENT decoded **615** in parallel in multiple block decoders **505***a*–**505***m*, as described above. The process for decoding the encoded image blocks **390** is further described in FIG. 6B. Each decoded **615** image block is then composed **620** into a data file with the converted **612** header information by the image composer **504**. The image composer **504** generates the data file as an output **625** that represents the original image **310**.

FIG. 6B is a flow diagram illustrating operation of the block encoder **505** in accordance with the present invention. Once the process is started **630**, each encoded image block **390** is received by the block decoder **505** and the block type for each encoded image block **390** is detected **640**. Specifically, for a preferred embodiment the first and the second codewords **390***a*, **CW0**, **CW1**, respectively, are received **635** by the block type detector **520** of the block decoder **505**. As discussed above, comparing the numerical values of CW0 and CW1 reveals the block type.

In addition, the first five bits of each codeword **390***a*, e.g., **CW0**, **CW1**, that represent the red-channel color are received by the red-channel **545** of each of the first and the second decoder units **530**, **540**, the second 6-bits of each codeword **390***a* **CW0**, **CW1** that represent the green-channel color are received by the green-channel of each of the first and the second decoder units **530**, **540**, and the last 5-bits of each codeword **390***a* **CW0**, **CW1** that represent the blue-channel color are received by the blue-channel of each of the first and the second decoder units **530**, **540**.

The block type detector **520** detects **640** the block type for an encoded image block **390**. Specifically, the comparator **522** compares the first and the second codewords **390***a*, **CW0**, **CW 1**, and generates a flag signal to enable the first 2×1 multiplexers **525***a* or the second 2×1 multiplexers **525***b* which, in turn, selects **645** either the first decoding unit **530** or the second decoding unit **540**, respectively. The process then calculates **650** the quantized color levels for the decoder units **530**, **540**.

To calculate **650** the quantized color levels, the first decoding unit **530** calculates the four colors associated with the two codewords **390***a*, **CW0**, **CW1**, using the following relationship:

$CW0$=first codeword=first color;

$CW1$=second codeword=second color;

$CW2$=third color=$(\frac{2}{3})CW0+(\frac{1}{3})CW1$;

$CW3$=fourth color=$(\frac{1}{3})CW0+(\frac{2}{3})CW1$.

In one embodiment, the first decoder unit **530** may estimate the above equations for CW2 and CW3, for example, as follows:

$CW2=(\frac{5}{8})CW0+(\frac{3}{8})CW1$; and

$CW3=(\frac{1}{4})CW0+(\frac{1}{4})CW1$.

The red-color blocks **550***a*, **550***b* serve as a one-bit shift register to get (½)CW0 or (½)CW1 and each full adder **552***a*, **552***b*, **554***a*, **554***b* also serves to shift the signal left by 1-it. Thus, the signal from the first full adders **552***a*, **552***b* is (¼)CW0 or (¼)CW1, respectively, because of a two-bit overall shift and the signal from the second full adders **554***a*, **554***b* is (⅛)CW0 or (⅛)CW1, respectively, because of a three-bit overall shift. These values allow for the above approximations for the color signals.

The second decoder unit **540** calculates **650** three colors associated with the codewords **390***a*, CW0, CW1, and includes a fourth signal that indicates a transparency is being passed. The second decoder unit **540** calculates colors, for example, as:

CW0=first codeword=first color;

CW1=second codeword=second color;

CW3=third color=(½)*CW0*+(½)*CW1*; and

T=Transparency.

In one embodiment the second decoder unit **540** has no approximation because the signals received from the red-color blocks **550***a*, **550***b* is shifted left by one-bit so that the color is already calculated to (½)CW0 and (½)CW1, respectively.

After the quantized color levels for the selected **645** decoder unit **530**, **540** have been calculated **650**, each bitmap value for each pixel is read **655** from the encoded image data block **385**. As each index is read **655** it is mapped **660** to one of the four calculated colors if the first decoder unit **530** is selected **645** or one of the three colors and transparency if the second decoder unit **540** is selected. The mapped **660** colors are selected by the 4x1 multiplexer **526** based on the value of the ID signal from the bitmap **390***b* of the encoded image block **390**. As stated previously, a similar process occurs for selection of colors in the green-channel and the blue-channel.

As the colors are output from the red-, green-, and blue-channels, the output is received by the image composer **504**. The image composer **504** orders the output from the block encoders **505** in the same order as the original image **310** was decomposed. The resulting **665** image that is output from the image decoder system **230** is the original image that is forwarded to an output source **240**, e.g., a computer screen, which displays that image.

The system and method of the present invention beneficially allows for random access to any desired image block **260** within an image, and any pixel **270** within an image block **260**. FIG. **7**A is a block diagram of a subsystem **700** that provides random access to a pixel **270** or an image block **260** in accordance with the present invention. PATENT The random access subsystem **700** includes a block address computation module **710**, a block fetching module **720**, and the one or more block decoders **505**. The block address computation module **710** is coupled to receive the header information **385***a* of the encoded image data **385**. The block address computation module **710** is also coupled to the block fetching module **720**. The block fetching module **720** is coupled to receive the encoded image block portion **390-1-R** of the encoded image data **385**. The block fetching module **720** is also coupled to the block decoders **505**.

FIG. **7**B is a flow diagram illustrating a process of random access to a pixel **270** or an image block **260** using the random access subsystem **700** in accordance with the present invention. When particular pixels **270** have been identified for decoding, the process starts **740** with the image decoder system **230** receiving the encoded image data **385**. The modified header **385***a* of the encoded image data **385** is forwarded to the block address computation module **710** and the encoded image block portion **390-1-R** of the encoded image data **385** is forwarded to the block fetching module **720**.

The block address computation module **710** reads the modified header **385***a* to compute **745** the address of the encoded image block portion **390-1-R** having the desired pixels **270**. The address computed **745** is dependent upon the pixel coordinates within an image. Using the computed **745** address, the block fetching module **720** identifies the encoded image block **390** of the encoded image block portion **390-1-R** that has the desired pixels **270**. Once the encoded image block **390** having the desired pixels **270** has been identified, only the identified encoded image block **390** is forwarded to the block decoders **505** for processing.

Similar to the process described above in FIG. **6**B, the block decoders **505** compute **755** the quantized color levels for the identified encoded image blocks **390** having the desired pixels. After the quantized color levels have been computed **755**, the color of the desired pixel is selected **760** and output **765** from the image decoder system **230**.

Random access to pixels **270** of an image block **260** advantageously allows for selective decoding of only needed portions or sections of an image. Random access also allows the image to be decoded in any order the data is required. For example, in three-dimensional texture mapping only portions of the texture may be required and these portions will generally be required in some non-sequential order. Thus, the present invention increases processing efficiency and performance when processing only a portion or section of an image.

The present invention beneficially encodes, or compresses, the size of an original image **310** from 24-bits per pixel to an aggregate 4-bits per pixel and then decodes, or decompresses the encoded image data **385** to get a representation of the original image **310**. Further, the claimed invention uses, for example, two base points or codewords from which additional colors are derived so that extra bits are not necessary to identify a pixel **270** color.

Moreover, the present invention advantageously accomplishes the data compression on an individual block basis with the same number of bits per block so that the compression rate can remain fixed. Further, because the blocks are of fixed size with a fixed number of pixels **270**, the present invention beneficially allows for random access to any particular pixel **270** in the block. The present invention provides for an efficient use of system resources because entire blocks of data are not retrieved and decoded to display data corresponding to only a few pixels **270**.

In addition, the use of a fixed-rate 64-bit data blocks in the present invention provides the advantage of having simplified header information that allows for faster processing of individual data blocks. Also, a 64-bit data block allows for data blocks to be processed rapidly, e.g., within one-clock cycle, as the need to wait until a full data string is assembled is eliminated. Further, the present invention also reduces the microchip space necessary for a decoder system because the decoder system only needs to decode each pixel to a set of colors determined by, e.g., the two codewords.

While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and components disclosed herein and that vari-

ous modifications, changes and variations which will be apparent to those skilled in the art may be made in the arrangement, operation and details of the method and apparatus of the present invention disclosed herein without departing from the spirit and scope of the invention as defined in the appended claims.

What is claimed is:

1. A data format for representing an original image block having a pixel color set, comprising:

a codeword portion for storing at least two codewords;

a bitmap portion for storing a set of indices, the bitmap portion constructed by a bitmap construction module utilizing the codeword portion associated with the bitmap portion; and

wherein said codewords define at least three colors that approximate the pixel color set, and said indices map the pixel color set to at least one of said at least three colors.

2. The data format of claim 1, wherein said set of indices includes a predefined index.

3. The data format of claim 2, wherein said predefined index is for mapping a transparency identifier associated with the original image block.

4. The data format of claim 2, wherein said predefined index is for mapping an alpha value associated with the original image block.

5. The data format of claim 2, wherein said predefined index is for mapping a color key value associated with the original image block.

6. The data format of claim 1, wherein said codeword portion includes a first portion for storing a first codeword and a second portion for storing a second codeword; and wherein said first codeword and said second codeword are used to indicate a block type for the original image block.

7. The data format of claim 1, wherein said codeword portion includes a first portion for storing a first codeword and a second portion for storing a second codeword; and wherein said at least three colors includes at least two computed colors if said first codeword is greater than said second codeword.

8. The data format of claim 1, wherein said codeword portion includes a first portion for storing a first codeword and a second portion for storing a second codeword; and wherein said at least three colors includes at least one computed color and said set of indices includes a predefined index if said first codeword is less than said second codeword.

9. The data format of claim 1, wherein said at least three colors are computed using a geometric element fitted to said pixel color set so that said geometric element has a minimal moment of inertia.

10. The data format of claim 1, wherein said at least three colors includes one of said at least two codewords.

11. A data format for representing an original image block having a pixel color set, comprising:

a codeword portion for storing at least one codeword;

a bitmap portion for storing a set of indices, said set of indices includes an available index for representing a transparency identifier, the bitmap portion constructed by a bitmap construction module utilizing the codeword portion associated with the bitmap portion; and

wherein said codeword defines a set of colors that approximate the pixel color set, and said indices map the pixel color set to at least one color in said set of colors.

12. The data format of claim 11, wherein said set of colors includes said at least one codeword and a computed color.

13. The data format of claim 11, wherein said set of colors includes at least three colors.

14. A data format for representing an original image block having a pixel color set, comprising:

a codeword portion for storing at least one codeword;

a bitmap portion for storing a set of indices;

wherein said at least one codeword defines a set of colors that approximate the pixel color set, and said indices map the pixel color set to at least one color in said set of colors; and

wherein said set of colors are computed using a geometric element fitted to said pixel color set so that said geometric element has a minimal moment of inertia.

15. An encoded image data format for representing an original image partitioned into at least two image blocks, said image blocks each having a corresponding pixel color set, the data format comprising:

at least two encoded image block portions, one of said encoded image block portions having a codeword portion for storing at least two codewords, and a bitmap portion for storing a set of indices, the bitmap portion constructed by a bitmap construction module utilizing the codeword portion associated with the bitmap portion; and

wherein said at least two codewords define at least three colors that approximate the pixel color set of one of the original image blocks, and said indices map the pixel color set to at least one of said at least three colors.

16. The data format of claim 15, further including a header portion.

17. The data format of claim 15, wherein said set of indices includes a predefined index.

18. The data format of claim 17, wherein said predefined index is for mapping a transparency identifier associated with the original image block.

19. The data format of claim 17, wherein said predefined index is for mapping an alpha value associated with the original image block.

20. The data format of claim 17, wherein said predefined index is for mapping a color key value associated with the original image block.

21. The data format of claim 15, wherein said set of colors are computed using a geometric element fitted to said pixel color set so that said geometric element has a minimal moment of inertia.

22. The data format of claim 15, wherein said at least three colors includes one of said at least two codewords.

23. An encoded image data format for representing an original image partitioned into at least a first image block having a first pixel color set and a second image block having a second pixel color set, the data format comprising:

a first encoded image block having a first portion for storing a first codeword, a second codeword, and a first bitmap portion for storing a first set of indices;

a second encoded image block having a second portion for storing a third codeword, a fourth codeword, and a second bitmap portion for storing a second set of indices;

wherein said first and second codewords define a first set of colors that approximate the first pixel color set, and said first set of indices map the first set of colors to the first pixel color set; and

wherein said third and fourth codewords define a second set of colors that approximate the second pixel color

set, and said second set of indices map the second set of colors to the second pixel color set.

24. The encoded image data format of claim 23, wherein said first set of colors includes at least three colors.

25. The data format of claim 23, wherein said first set of colors includes at least said first codeword.

26. The data format of claim 23, wherein said first set of colors includes said second codeword.

27. The data format of claim 23, wherein said second set of colors includes at least three colors.

28. The data format of claim 23, wherein said second set of colors includes said third codeword.

29. The data format of claim 23, wherein said second set of colors includes said fourth codeword.

* * * * *

Exhibit 10

US006775417B2

(12) **United States Patent**
Hong et al.

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(45) **Date of Patent: Aug. 10, 2004**

(54) **FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 165 days.

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(51) **Int. Cl.**[7] **G06K 9/38**

(52) **U.S. Cl.** **382/253**; 382/232; 725/146

(58) **Field of Search** 382/166, 162, 382/232, 253; 725/146; 345/549, 550; 358/539

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,821,208	A	4/1989	Ryan et al.	345/550
4,887,151	A	12/1989	Wataya	358/539
5,734,744	A	3/1998	Wittenstein et al.	382/166
5,742,892	A	4/1998	Chaddha	725/146
5,748,904	A	5/1998	Huang et al.	345/544
5,787,192	A	7/1998	Takaichi et al.	382/166
5,822,465	A	10/1998	Normile et al.	382/253
5,956,425	A	9/1999	Yoshida	382/234
5,956,431	A	9/1999	Iourcha et al.	382/253
6,075,619	A	6/2000	Iizuka	382/166

FOREIGN PATENT DOCUMENTS

JP	401284188	A *	11/1989	H04N/7/137
JP	405216993		8/1993	G06F/15/70

OTHER PUBLICATIONS

Feng et al., "A Dynamic Address Vector Quantization Based on Inter-Block and Inter-Color Correction for Color Image Coding," IEEE International Conference on Acoustics, Speech and Signal Processing, vol. 3, May 1989, pp. 1755–1758.

Schilling et al., "Texram: A Smart Memory for Texturing," IEEE Computer Graphics & Applications, May 1996, vol. 16, No. 3, pp. 9–19.

(List continued on next page.)

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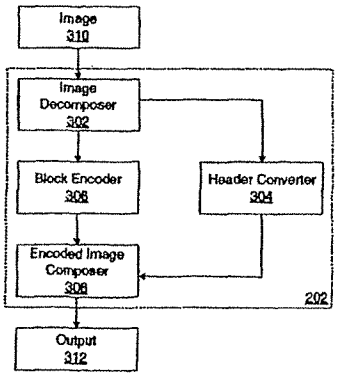
(57) **ABSTRACT**

An image processing system including an image encoder and image decoding system is provided. The image encoder system includes an image decomposer, a block encoder, and an encoded image composer. The image decomposer decomposes the image into blocks. The block encoder which includes a selection module, a codeword generation module and a construction module, processes the blocks. Specifically, the selection module computes a set of parameters from image data values of a set of image elements in the image block. The codeword generation module generates codewords which the construction module uses to derive a set of quantized image data values. The construction module then maps each of the image element's original image data values to an index to one of the derived image data values. The image decoding system reverses this process to reorder decompressed image blocks in an output data file.

30 Claims, 16 Drawing Sheets



OTHER PUBLICATIONS

Knittel et al., "Hardware and Software for Superior Texture Performance," In 10: Eurographics Hardware Workshop 1995, Maastricht, The Netherlands, Aug. 28–29, 1995, pp. 1–8.

Campbell et al., "Two Bit/Pixel Full Color Encoding," Computer Graphics (Proc. SIGPRAPH 1986), Aug. 18–22, 1986, vol. 20, No. 4, Dallas, TX, pp.215–219.

Yang et al., "Hybrid Adaptive Block Truncation Coding for Image Compression," Optical Engineering, Soc. of Photo–Optical Instrumentation Engineers, Bellingham, USA, Vo. 36, No. 4, Apr. 1, 1997, pp. 1021–1027.

Kugler, "High–Performance Texture Decompression Hardware," Visual Computer, Springer, Berlin, Germany, vol. 13, No. 2, 1997, pp. 51–63.

Panos Nasiopoulos et al., "Adaptive Compression Coding," IEEE Transactions on Communications, IEEE Inc., New York, USA, vol. 39, No. 8, Aug. 1, 1991, pp. 1245–1254.

Delp E.J. et al., "Image Compression Using Block Truncation Coding," IEEE Inc., New York, USA, vol. COM–27, No. 9, Sep. 1979, pp. 1335–1342.

Yang et al., "Use of Radius Weighted Mean to Cluster Two–Class Data," Electronics Letters, IEE Stevenage, Great Britain, vol. 30, No. 10, May 12, 1994, pp. 757–759.

Russ, J.C. et al., "Optimal Grey Scale Images from Multiplane Color Images," Journal of Computer–Assisted Microscopy, Dec. 1995, Plenum, USA, vol. 7, No. 4, pp. 221–233.

Knittel et al., "Hardware for Superior Texture Performance," Eurographics Workshop on Graphics Hardware, Jul. 28, 1995, pp. 33–40.

* cited by examiner

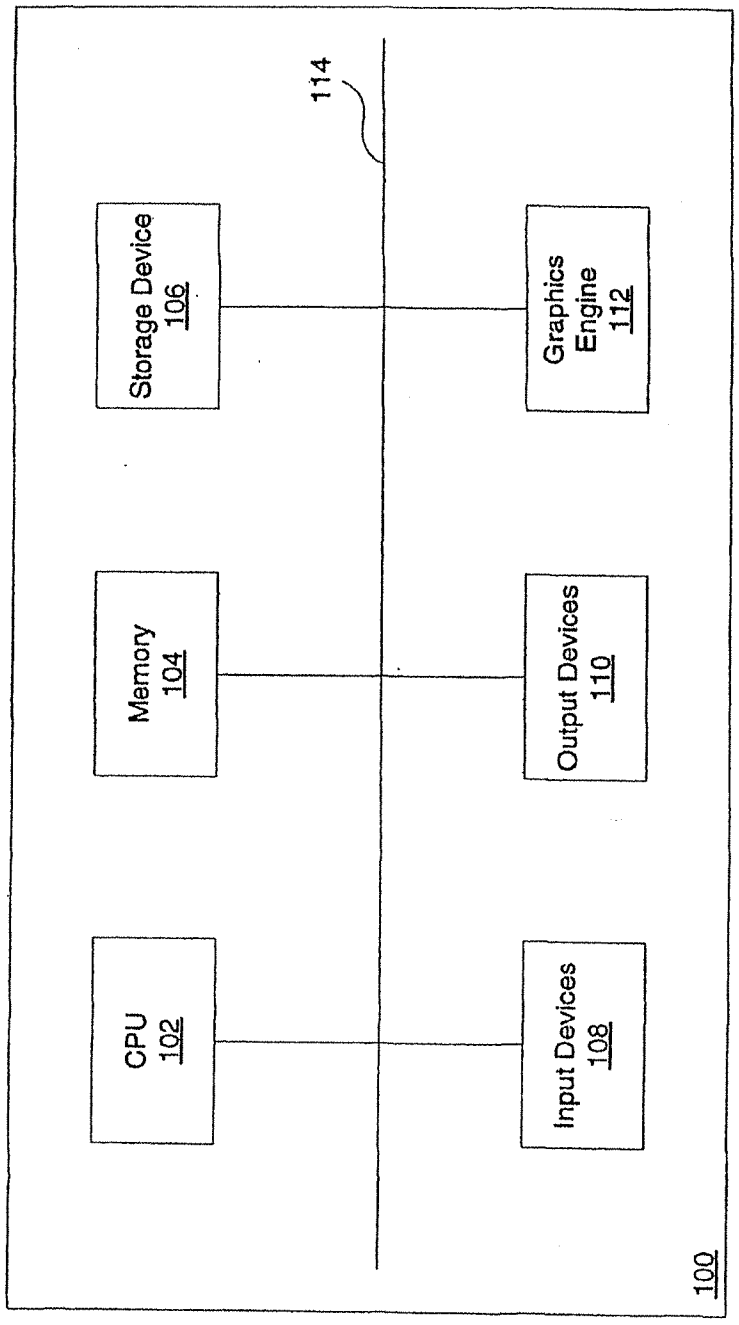


FIG. 1

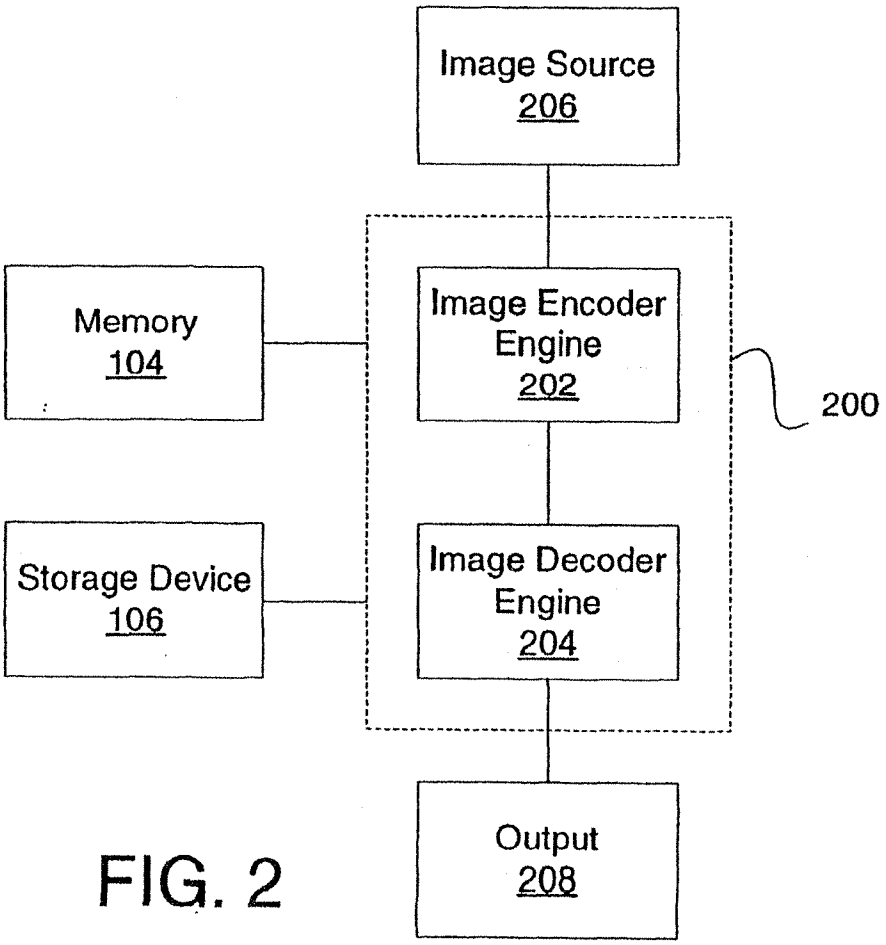


FIG. 2

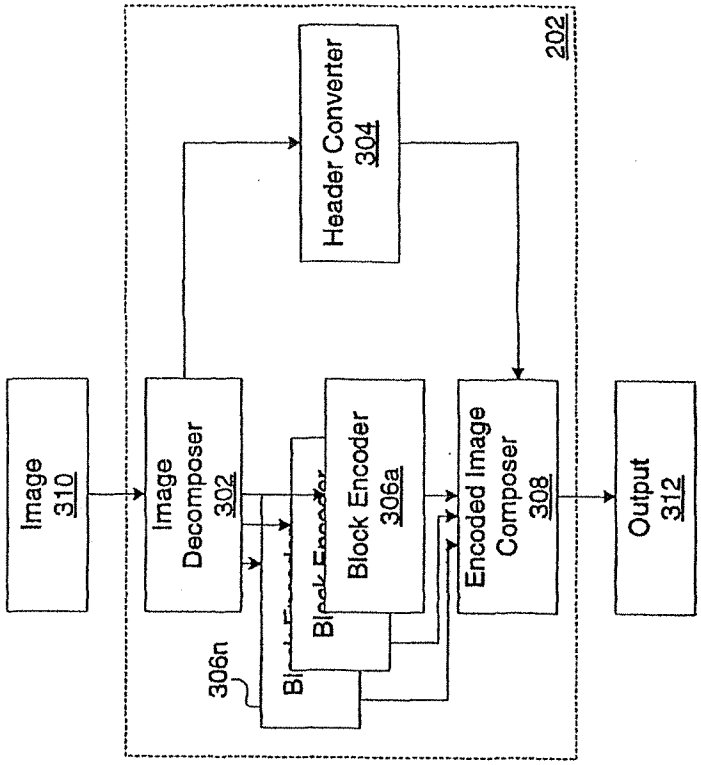


FIG. 3B

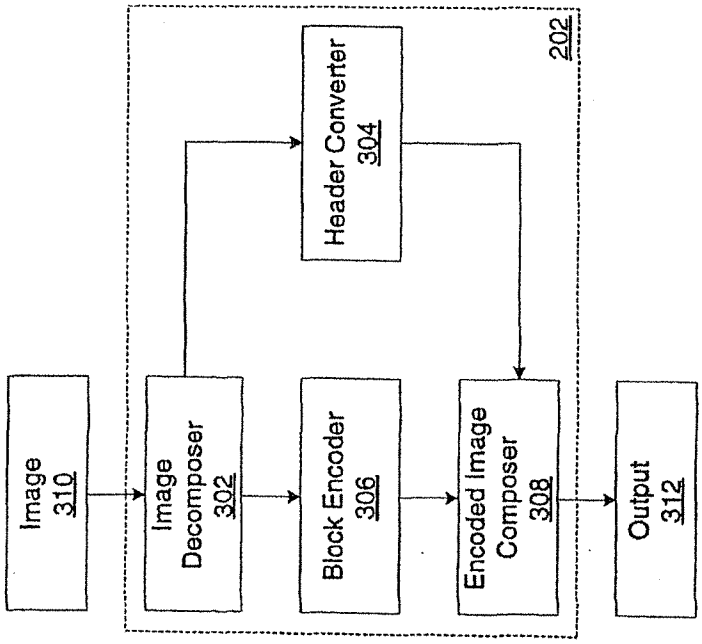


FIG. 3A

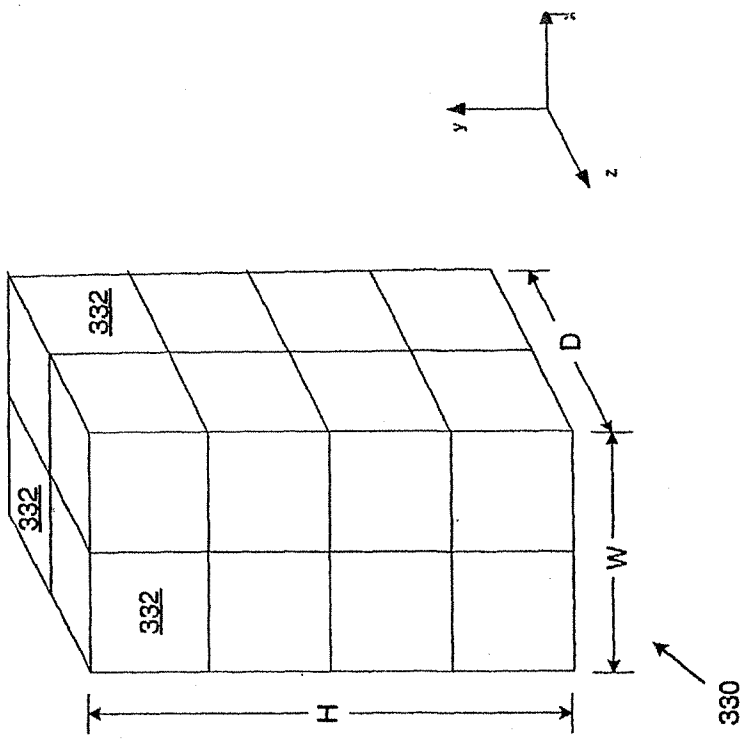


FIG. 3D

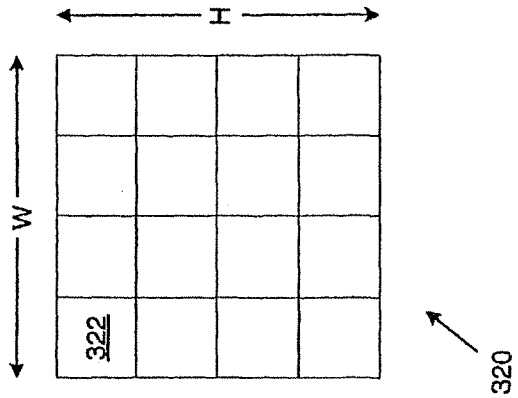


FIG. 3C

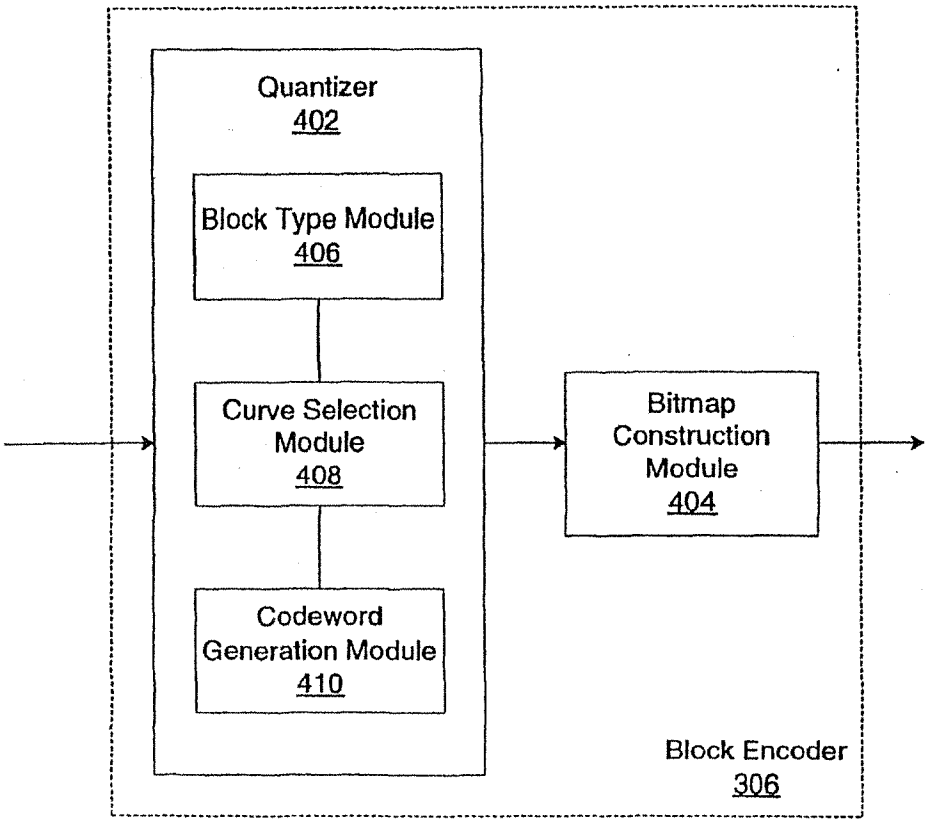


FIG. 4

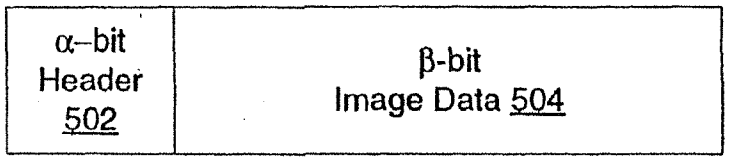


FIG. 5A

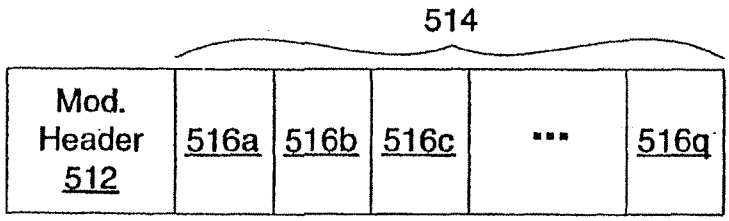


FIG. 5B

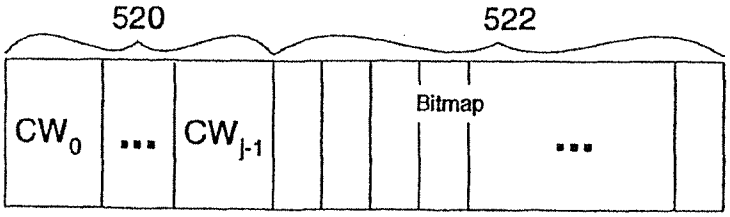


FIG. 5C

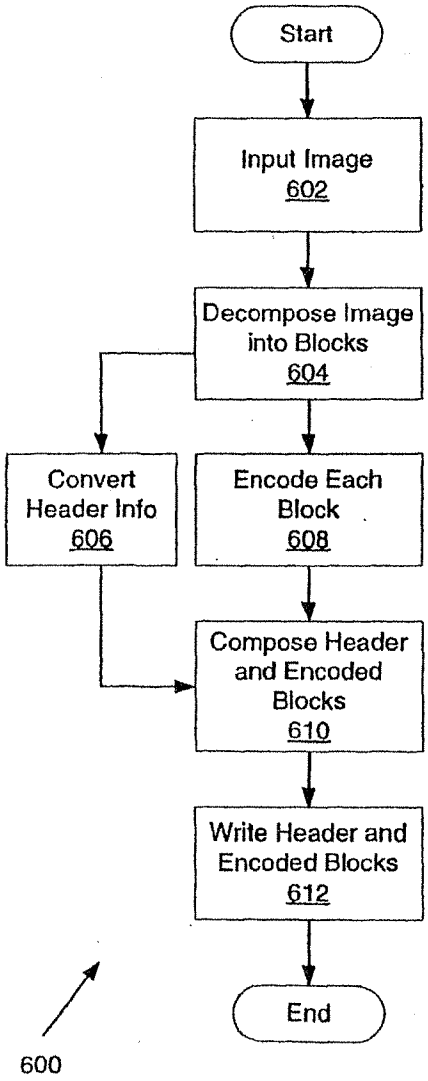


FIG. 6A

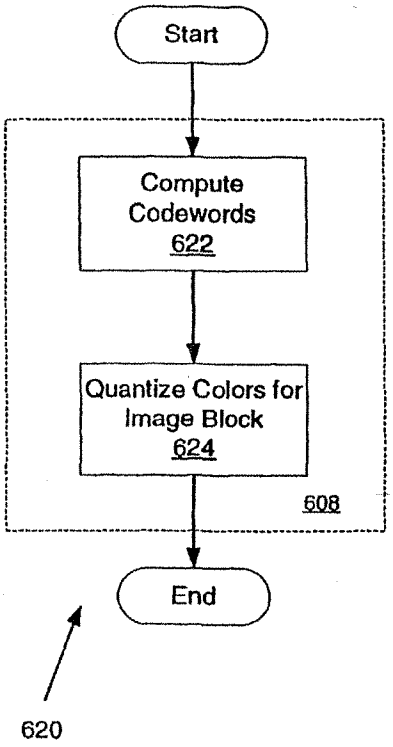


FIG. 6B

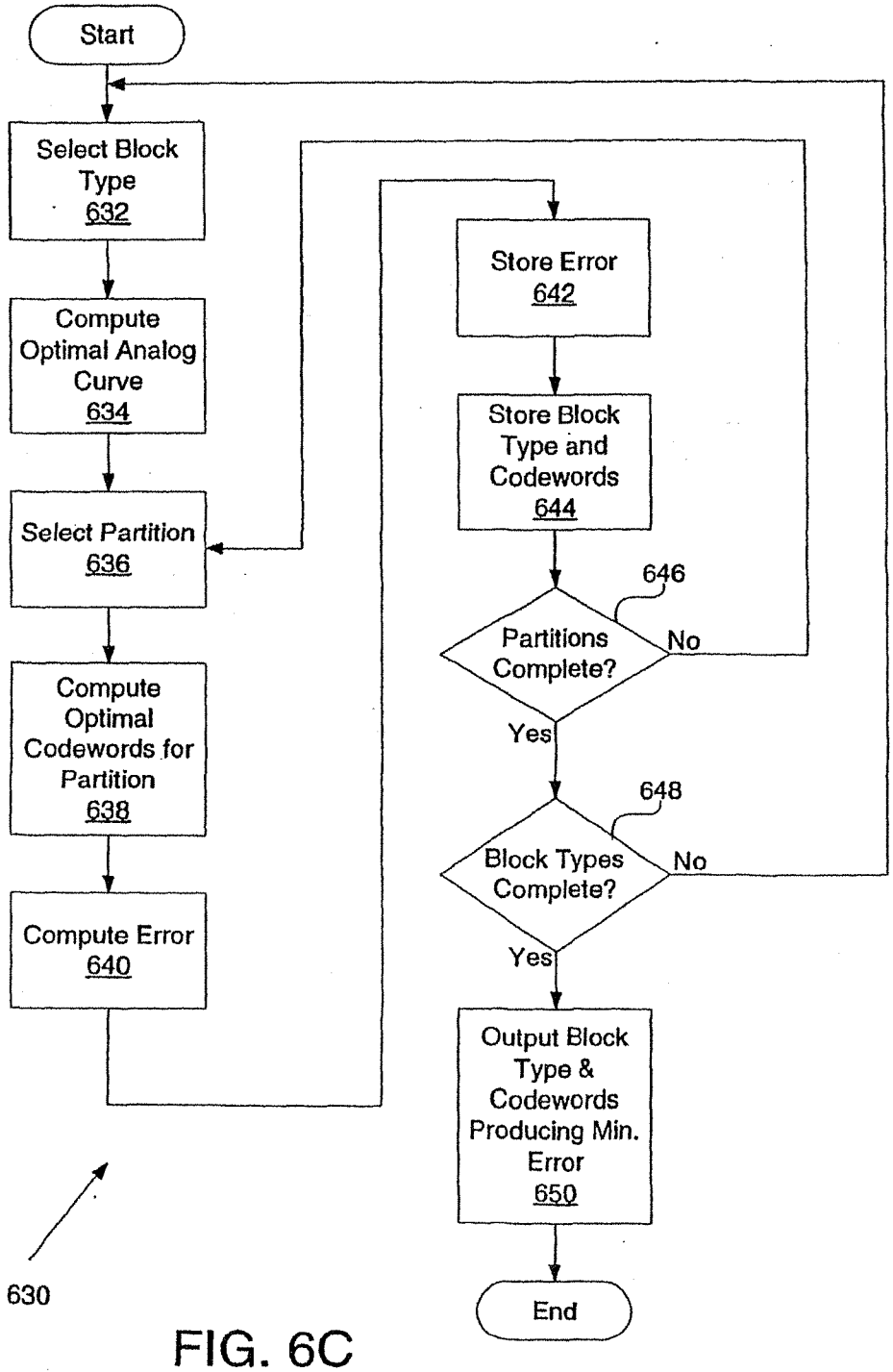


FIG. 6C

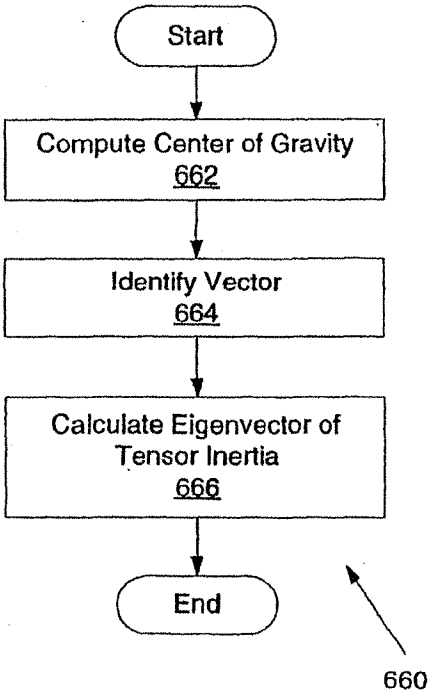


FIG. 6D

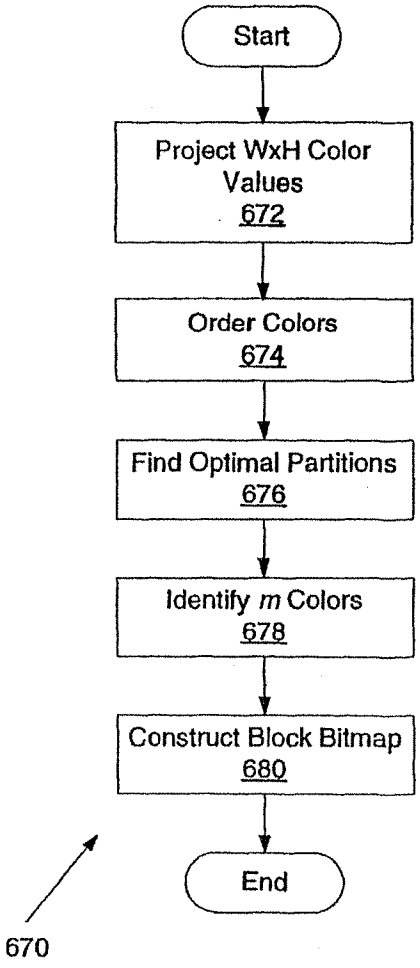


FIG. 6E

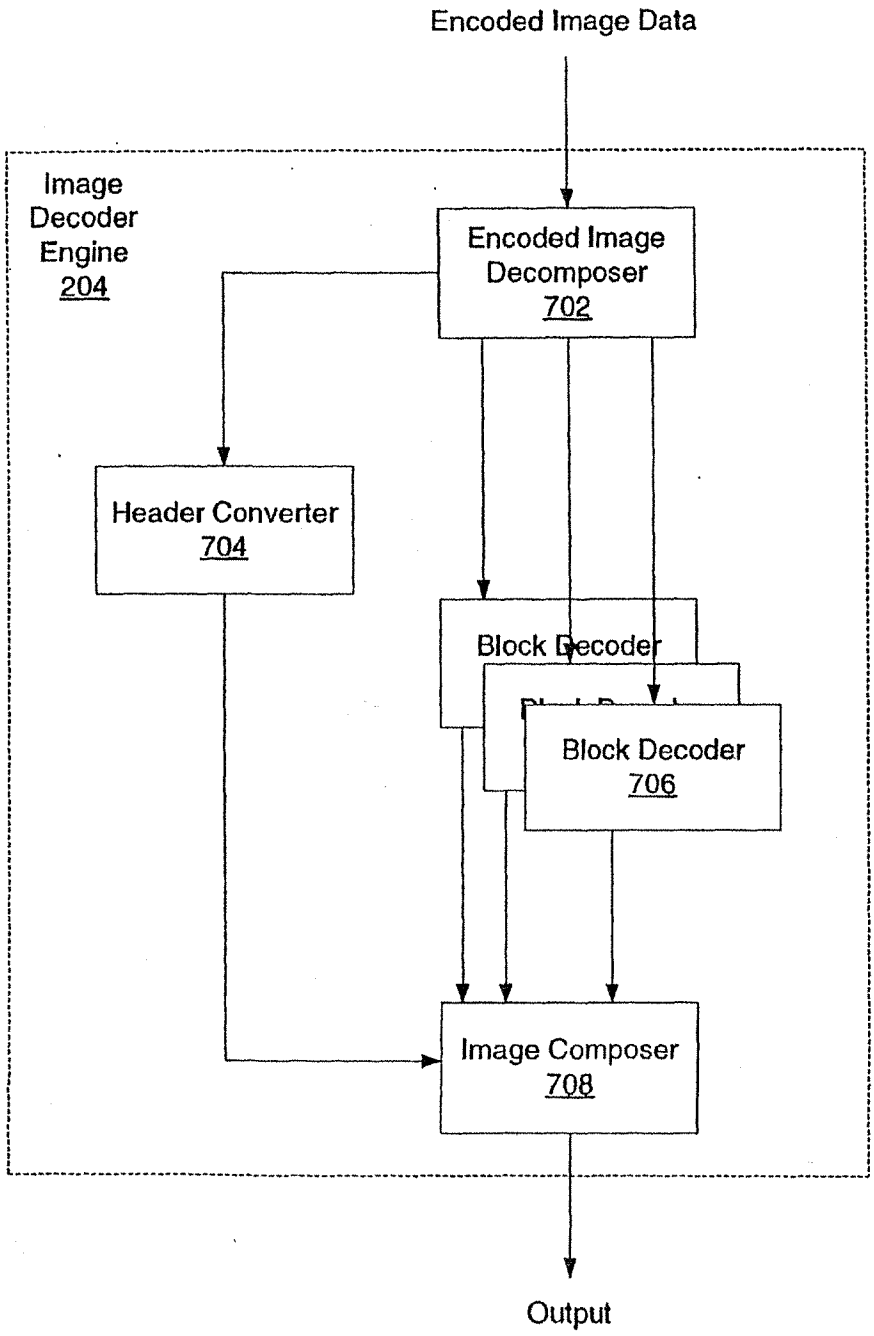


FIG. 7A

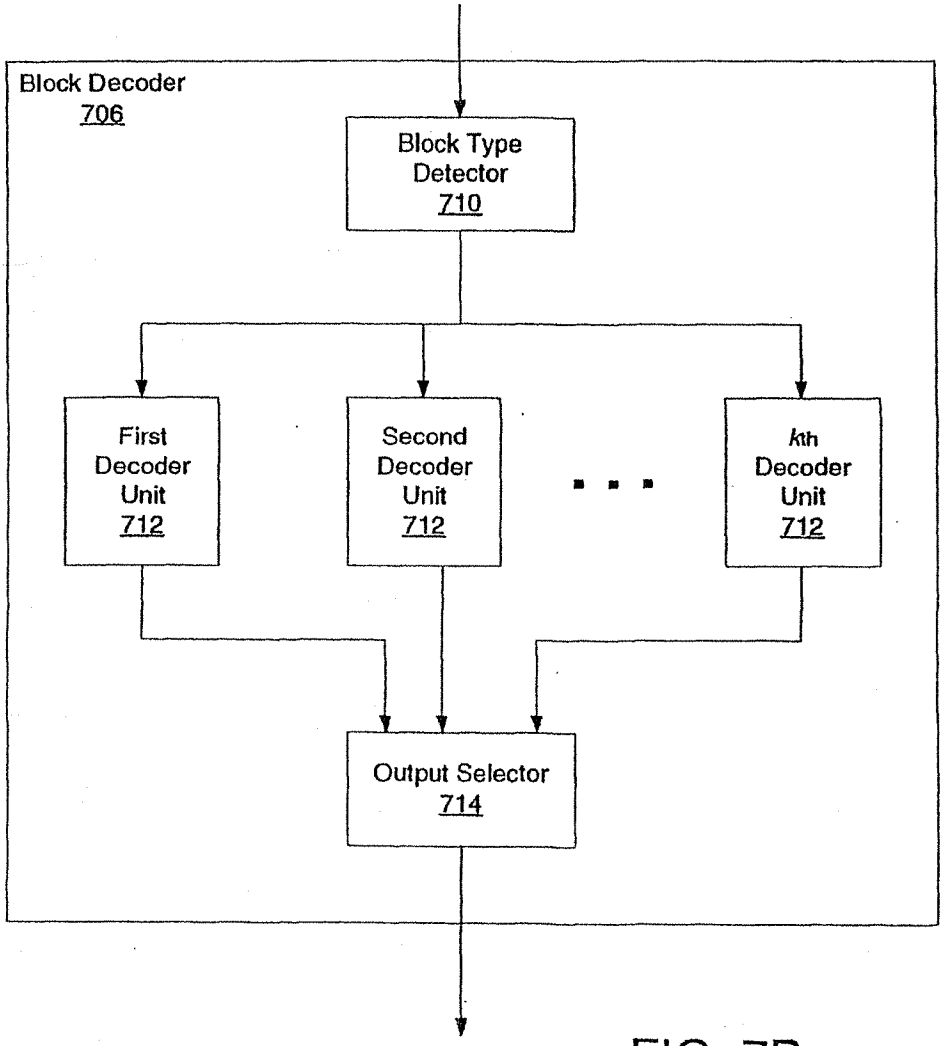


FIG. 7B

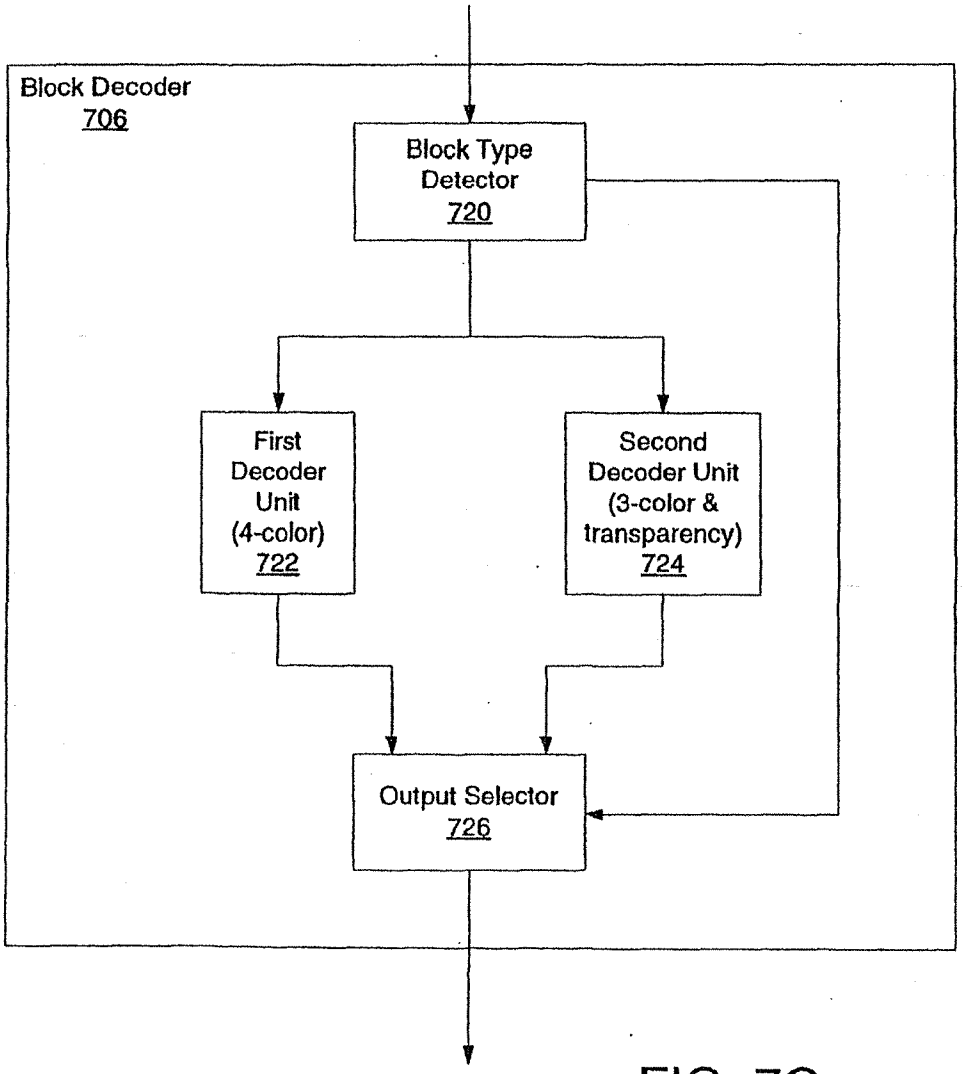


FIG. 7C

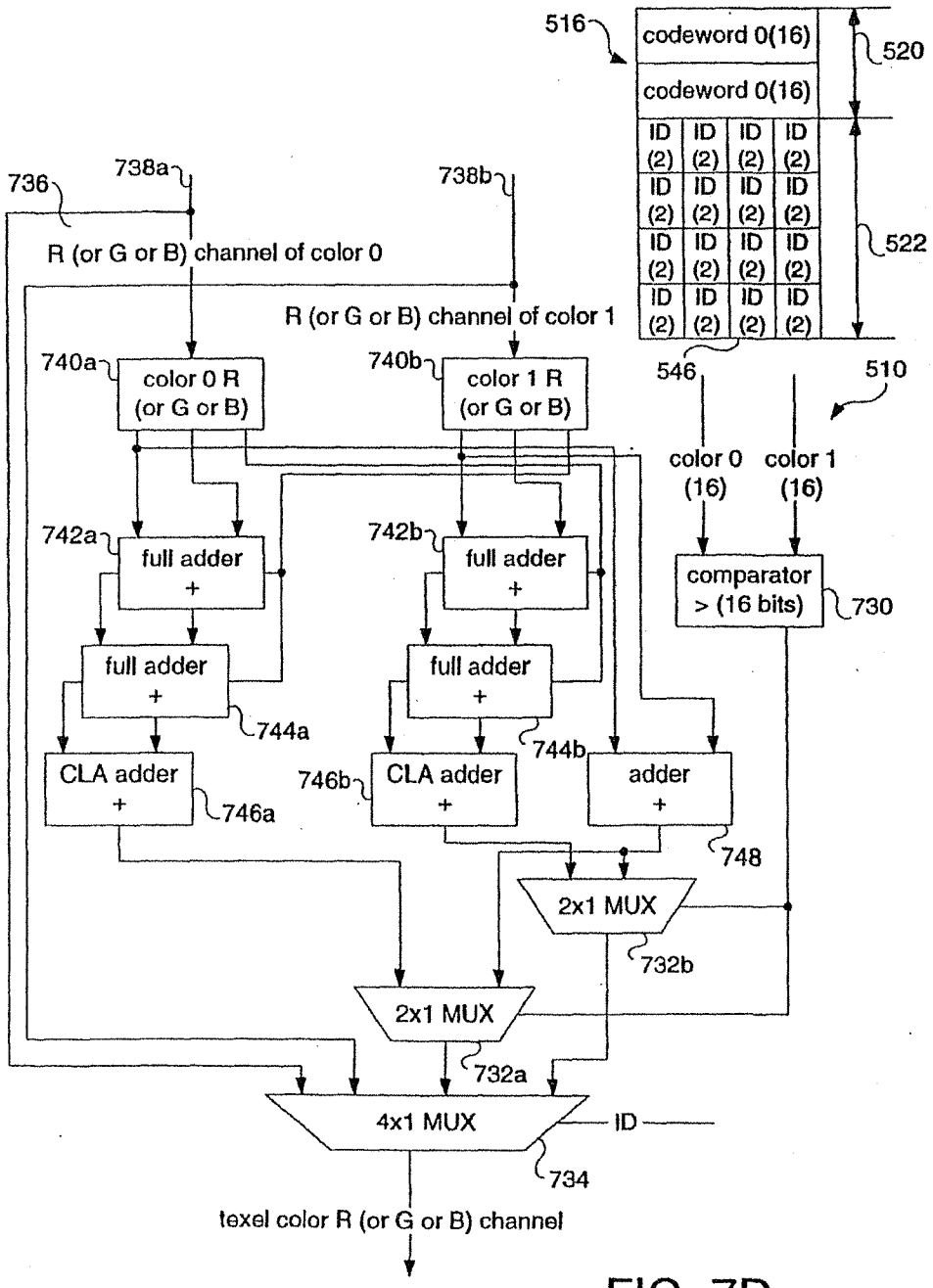


FIG. 7D

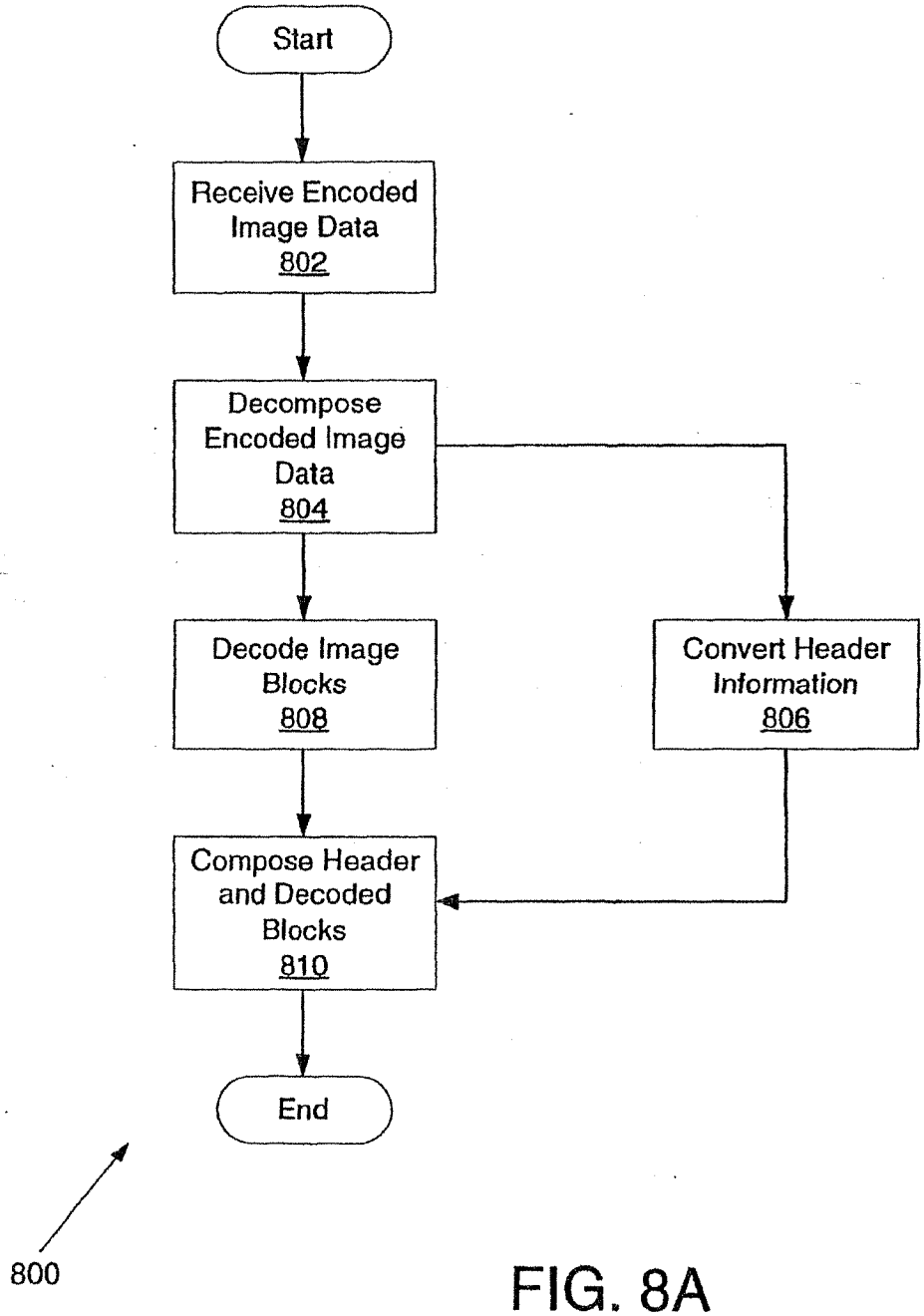


FIG. 8A

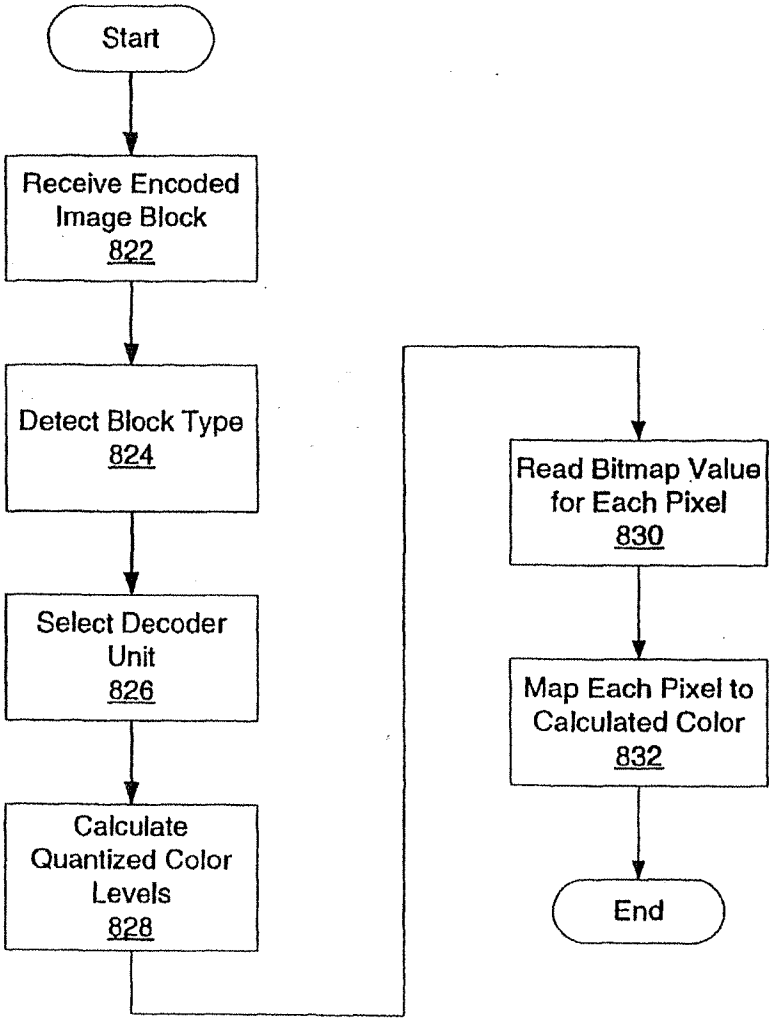


FIG. 8B

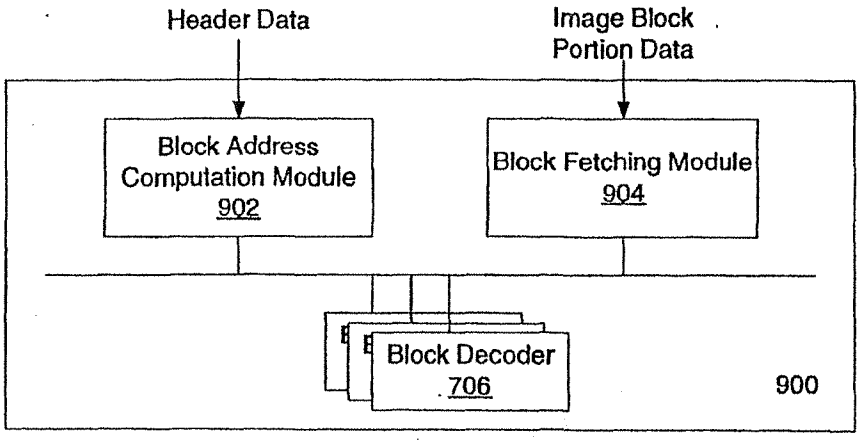


FIG. 9A

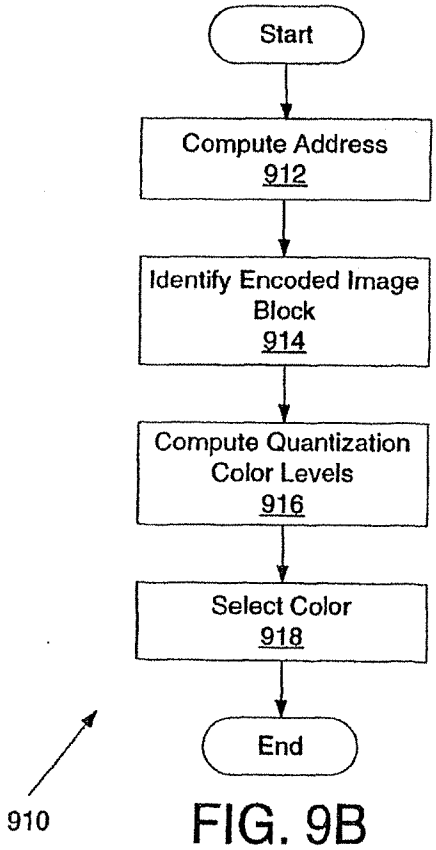


FIG. 9B

FIXED-RATE BLOCK-BASED IMAGE COMPRESSION WITH INFERRED PIXEL VALUES

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation-in-part application of Ser. No. 09/351,930 filed Jul. 12, 1999 now U.S. Pat. No. 6,658,146, which is a continuation of Ser. No. 08/942,860 filed Oct. 2, 1997, now U.S. Pat. No. 5,956,431 issued Sep. 21, 1999.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to image processing, and more particularly to three-dimensional rendering using fixed-rate image compression.

2. Description of Related Art

Conventionally, generating images, such as realistic and animated graphics on a computing device, required tremendous memory bandwidth and processing power on a graphics system. Requirements for memory and processing power are particularly true when dealing with three-dimensional images. In order to reduce bandwidth and processing power requirements, various compression methods and systems have been developed including Entropy or lossless encoders, Discrete Cosine Transform ("DCT") or JPEG type compressors, block truncation coding, and color cell compression. However, these methods and systems have numerous disadvantages.

Entropy or lossless encoders include Lempel-Ziv encoders which rely on predictability. For data compression using entropy encoders, a few bits are used to encode most commonly occurring symbols. In stationary systems where probabilities are fixed, entropy coding provides a lower bound for compression than can be achieved with a given alphabet of symbols. However, coding does not allow random access to any given symbol. Part of the compressed data preceding a symbol of interest must be first fetched and decompressed to decode the symbol, requiring considerable processing time and resources, as well as decreasing memory throughput. Another problem with existing Entropy methods and systems is that no guaranteed compression factor is provided. Thus, this type of encoding scheme is impractical where memory size is fixed.

Discrete Cosine Transform or JPEG-type compressors allow users to select a level of image quality. With DCT, uncorrelated coefficients are produced so that each coefficient can be treated independently without loss of compression efficiency. The DCT coefficients can be quantized using visually-weighted quantization values which selectively discard least important information.

DCT, however, suffers from a number of shortcomings. One problem with DCT and JPEG-type compressors is a requirement of large blocks of pixels, typically, 8×8 or 16×16 pixels, as a minimally accessible unit in order to obtain a reasonable compression factor and quality. Access to a very small area, or even a single pixel involves fetching a large quantity of compressed data; thus requiring increased processor power and memory bandwidth. A second problem is that the compression factor is variable, therefore requiring a complicated memory management system that, in turn, requires greater processor resources. A third problem with DCT and JPEG-type compression is that using a large compression factor significantly degrades image quality. For

example, an image may be considerably distorted with a form of ringing around edges in the image as well as noticeable color shifts in areas of the image. Neither artifact can be removed with subsequent low-pass filtering.

A further disadvantage with DCT and JPEG-type compression is the complexity and significant hardware cost for a compressor and decompressor ("CODEC"). Furthermore, high latency of a decompressor results in a large additional hardware cost for buffering throughout the system to compensate for the latency. Finally, DCT and JPEG-type compressors may not be able to compress a color keyed image.

Block truncation coding ("BTC") and color cell compression ("CCC") use a local one-bit quantizer on 4×4 pixel blocks. Compressed data for such a block consists of only two colors and 16-bits that indicate which of the two colors is assigned to each of 16 pixels. Decoding a BTC/CCC image consists of using a multiplexer with a look-up table so that once a 16-texel (or texture element, which is the smallest addressable unit of a texture map) block (32-bits) is retrieved from memory, the individual pixels are decoded by looking up the two possible colors for that block and selecting the color according to an associated bit from 16 decision bits.

Because the BTC/CCC methods quantize each block to just two color levels, significant image degradation may occur. Further, a two-bit variation of CCC stores the two colors as 8-bit indices into a 256-entry color lookup table. Thus, such pixel blocks cannot be decoded without fetching additional information which may consume additional memory bandwidth.

The BTC/CCC methods and systems can use a 3-bit per pixel scheme which stores the two colors as 16-bit values (not indices into a table) resulting in pixel blocks of six bytes. Fetching such units, however, decreases system performance because of additional overhead due to memory misalignment. Another problem associated with BTC/CCC methods is a high degradation of image quality when used to compress images that use color keying to indicate transparent pixels.

Therefore, there is a need for a system and method that maximizes accuracy of compressed images while minimizing storage, memory bandwidth requirements, and decoding hardware complexities. There is a further need for compressing image data blocks into convenient sizes to maintain alignment for random access to any one or more pixels.

SUMMARY OF THE INVENTION

The present invention provides for fixed-rate block based image compression with inferred pixel values. An image processing system includes an image encoder engine and an image decoder engine. The image encoder engine includes an image decomposer, at least one block encoder, and an encoded image composer. The block decomposer decomposes an original image into a header and a plurality of blocks which are composed of a plurality of image elements or pixels. The block encoder subsequently processes each block. The block encoder includes a selection module, a codeword generation module, and a construction module. Specifically, the selection module computes a set of parameters from image data values of each set of image elements. The codeword generation module then generates codewords which are reference image data values such as colors or density values. Subsequently, the construction module uses the codewords to derive a set of quantized image data values. The construction module then maps each of the image element's original image data values with an index to

one of the derived image data values. Finally, the codewords and indices are output as encoded image blocks.

Conversely, the image decoder engine includes an encoded image decomposer, at least one block decoder, and an image composer. The image decomposer takes the encoded image and decomposes the encoded image into a header and plurality of encoded image blocks. The block decoder uses the codewords in the encoded image blocks to generate a set of derived image data values. Subsequently, the block decoder maps the index values for each image element to one of the derived image data values. The image composer then reorders the decompressed image blocks in an output data file, which is forwarded to a display device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a data processing system, according to an embodiment of the present invention;

FIG. **2** is a block diagram of an image processing system;

FIG. **3A** is a block diagram of one embodiment of an image encoder system;

FIG. **3B** is a block diagram of an alternative embodiment of an image encoder system;

FIG. **3C** is a graphical representation of an image block;

FIG. **3D** is a graphical representation of a three-dimensional image block;

FIG. **4** is a block diagram of an image block encoder of FIG. **2A**, **3A**, or **3B**;

FIG. **5A** is a data sequence diagram of an original image;

FIG. **5B** is a data sequence diagram of encoded image data of an original image output from the image encoder system;

FIG. **5C** is a data sequence diagram of an encoded image block from the image block encoder of FIG. **4**;

FIGS. **6A–6E** are flowcharts illustrating encoding processes, according to the present invention;

FIG. **7A** is a block diagram of an image decoder system;

FIG. **7B** is a block diagram of one embodiment of a block decoder of FIG. **7A**;

FIG. **7C** is a block diagram of an alternative embodiment of a block decoder of FIG. **7A**;

FIG. **7D** is a logic diagram illustrating an exemplary decoder unit, according to the present invention;

FIG. **8A** is a flowchart illustrating a decoding process of the image decoder of FIG. **2**;

FIG. **8B** is a flowchart illustrating operations of the block encoder of FIG. **7A**;

FIG. **9A** is a block diagram of a subsystem for random access to a pixel or an image block; and

FIG. **9B** is a flowchart illustrating random access to a pixel or an image block.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **1** is a block diagram of a data processing system **100** for implementing the present invention. The data processing system **100** includes a CPU **102**, a memory **104**, a storage device **106**, input devices **108**, output devices **110**, and a graphics engine **112** all of which are coupled to a system bus **114**. The memory **104** and storage device **106** store data within the data processing system **100**. The input device **108** inputs data into the data processing system **100**, while the output device **110** receives data from the data processing system **100**. Although the data bus **114** is shown as a single line, alternatively, the data bus **114** may be a combination of a processor bus, a PCI bus, a graphic bus, or an ISA bus.

FIG. **2** is a block diagram of an exemplary image processing system **200**. In one embodiment, the image processing system **200** is contained within the graphics engine **112** (FIG. **1**). The image processing system **200** includes an image encoder engine **202** and an image decoder engine **204**. The image processing system **200** may also include, or be coupled to, an image source unit **206** which provides images to the image encoder engine **202**. Further, the image processing system **200** may include or be coupled to an output unit **208** to which processed images are forwarded for storage or further processing. Additionally, the image processing system **200** may be coupled to the memory **104** (FIG. **1**) and the storage device **106** (FIG. **1**). In an alternative embodiment, the image encoder engine **202** and the image decoder engine **204** are contained within different computing devices, and the encoded images pass between the two engines **202** and **204**.

Within the image encoder engine **202**, images are broken down into individual blocks and processed before being forwarded, for example, to the storage device **106** as compressed or encoded image data. When the encoded image data are ready for further processing, the encoded image data are forwarded to the image decoder engine **204**. The image decoder engine **204** receives the encoded image data and decodes the data to generate an output that is a representation of the original image that was received from the image source unit **206**.

FIGS. **3A** and **3B** are block diagrams illustrating two exemplary embodiments of the image encoder engine **202** of FIG. **2**. The image encoder engine **202** includes an image decomposer **302**, a header converter **304**, one or more block encoders **306** in FIG. **3A** (**306***a*–**306***n*, where n is the nth encoder in FIG. **3B**), and an encoded image composer **308**. The image decomposer **302** is coupled to receive an original image **310** from a source, such as the image source unit **206** (FIG. **2**), and forwards information from a header of the original image **310** to the header converter **304**. Subsequently, the header converter **304** modifies the original header to generate a modified header, as will be described further in connection with FIG. **5B**. The image decomposer **302** also breaks, or decomposes, the original image **310** into R numbers of image blocks, where R is any integer value. The number of image blocks the original image **310** is broken into may depend on the number of image pixels. In an exemplary embodiment, the image **310** having A image pixels by B image pixels will, typically, be (A/4)×(B/4) blocks. For example, an image that is 256 pixels by 256 pixels will be broken down into 64×64 blocks. In the present embodiment, the image is decomposed such that each image block is 4 pixels by 4 pixels (16 pixels). Those skilled in the art will recognize that the number of pixels or the image block size may be varied.

Briefly turning to FIG. **3C**, an example of a single image block **320** is illustrated. The image block **320** is composed of image elements (pixels) **322**. The image block **320** may be defined as an image region W pixels in width by H pixels in height. In the embodiment of FIG. **3C**, the image block **320** is W=4 pixels by H=4 pixels (4×4).

In an alternative embodiment, the original image **310** (FIG. **3A** or **3B**) may be a three-dimensional volume data set as shown in FIG. **3D**. FIG. **3D** illustrates an exemplary three-dimensional image block **330** made up of sixteen image elements (volume pixels or voxels) **332**. Image block **330** is defined as an image region W voxels in width, H voxels in height, and D voxels in depth.

The three-dimensional volume data set may be divided into image blocks of any size or shape. For example, the image may be divided along a z-axis into a plurality of xxyxz sized images, where z=1. Each of these xxyx1 images may be treated similarly with two-dimensional images, where each xxyx1 image is divided into two-dimensional image blocks, as described above with respect to FIG. 3C. However, decomposing the three-dimensional image into two-dimensional "slices" for compression does not fully utilize the graphical similarities that may exist in the z (depth) direction in a three-dimensional image. To utilize such similarities, the volume data may be decomposed into a plurality of three-dimensional image blocks. It will be understood that in alternative embodiments, other combinations of WxHxD are possible, and may be more desirable, depending on the data being compressed.

This type of three-dimensional image data is used, for example, in medical imaging applications such as ultrasound or magnetic resonance imaging ("MRI"). In such an application, a body part is scanned to produce a three-dimensional matrix of image elements (i.e., image block comprised of voxels **320**). The image is x voxels wide by y voxels high by z voxels deep. In this example, each voxel provides density data regarding characteristics of body tissue. In ultrasound applications, each voxel may be provided with a brightness level indicating the strength of echoes received during scanning.

In the embodiment of FIG. 3D, the original image **310** is a three-dimensional data volume where the image data are density values. In alternative embodiments, other scalar data types may be represented in the original image **310**, such as transparency or elevation data. In further embodiments, vector data, such as the data used for "bump maps", may be represented.

Referring back to FIGS. 3A and 3B, each block encoder **306** receives an image block **320** from the image decomposer **302**, and encodes or compresses each image block **320**. Subsequently, each encoded image block is forwarded to the encoded image composer **308** which orders the encoded image blocks in a data file. Next, the data file from the encoded image composer **308** is concatenated with the modified header from the header converter **304** to generate an encoded image data file that is forwarded to an output **312**. Thus, the modified header and the encoded image blocks together form the encoded image data that represent the original image **310**. Alternatively, having more than one block encoder **306***a*–**306***n*, as shown in FIG. 3B, allows for encoding multiple image blocks simultaneously, one image block per block encoder **306***a*–**306***n*, within the image encoder engine **202**. Advantageously, simultaneous encoding increases image processing efficiency and performance.

The image data associated with the original image **310** may be in any one of a variety of formats including red-green-blue ("RGB"), YUV **420** (YUV are color models representing luminosity and color difference signals), YUV **422**, or a propriety color space. In some cases, conversion to a different color space before encoding the original image **310** may be useful. In one embodiment, each image block **320** is a 4×4 set of pixels where each pixel **322** is 24-bits in size. For each pixel **322**, there are 8-bits for a Red("R")-channel, 8-bits for a Green("G")-channel, and 8-bits for a Blue("B")-channel in an RGB implementation color space. Alternatively, each encoded image block is also a 4×4 set of pixels with each pixel being only 2-bits in size and having an aggregate size of 4-bits as will be described further below.

FIG. **4** is a block diagram illustrating an exemplary block encoder **306** of FIGS. 3A and 3B. The block encoder **306** includes a quantizer **402** and a bitmap construction module **404**. Further, the quantizer **402** includes a block type module **406**, a curve selection module **408**, and a codeword generation module **410**.

Each image block **320** (FIG. 3C) of the decomposed original image **310** (FIGS. 3A and 3B) is received and initially processed by the quantizer **402** before being forwarded to the bitmap construction module **404**. The bitmap construction module **404** outputs encoded image blocks for the encoded image composer **308** (FIGS. 3A and 3B) to order. The bitmap construction module **404** and the modules of the quantizer **402** are described in more detail below.

Briefly, FIG. 5A is a diagram of a data sequencer or string **500** representing the original image **310** (FIGS. 3A and 3B) that is received by the block decomposer **302** (FIGS. 3A and 3B). The data string **500** includes an α-bit header **502** and a β-bit image data **504**. The header **502** may include information such as pixel width, pixel height, format of the original image **310** (e.g., number of bits to the pixel in RGB or YUV format), as well as other information. The image data **504** are data representing the original image **310**, itself.

FIG. 5B is a diagram of a data sequence or string **510** representing encoded image data that are generated by the image encoder engine **202** (FIG. 2). The encoded image data string **510** includes a modified header portion **512** and an encoded image block portion **514**. The modified header portion **512** is generated by the header converter **304** (FIGS. 3A and 3B) from the original α-bit header **502** (FIG. 5A) and includes information about file type, number of bits per pixel of the original image **310** (FIGS. 3A and 3B), addressing in the original image **310**, other miscellaneous encoding parameters, as well as the width and height information indicating size of the original image **310**. The encoded image block portion **514** includes encoded image blocks **516***a*–*q* from the block encoders **306** (FIGS. 3A and 3B) where q is the number of blocks resulting from the decomposed original image **310**.

FIG. 5C is a diagram of a data sequence or string **518** representing an encoded image block. The data string **518** may be similar to any one of the encoded image blocks **516***a*–*q* (FIG. 5B) shown in the encoded image data string **510** of FIG. 5B.

The encoded image block data string **518** includes a codeword section **520** and a bitmap section **522**. The codeword section **520** includes j codewords, where j is an integer value, that are used to compute colors of other image data indexed by the bitmap section **522**. A codeword is an n-bit data string that identifies a pixel property, such as color component, density, transparency, or other image data values. In one embodiment, there are two 16-bit codewords CW_0 and CW_1 (j=2). The bitmap section **522** is a Q-bit data portion and is described in more detail in connection with FIG. 6B.

In an alternative embodiment, each encoded image block is 64-bits, which includes two 16-bit codewords and a 32-bit (4×4×2 bit) bitmap **522**. Encoding the image block **320** (FIG. 3C) as described above provides greater system flexibility and increased data processing efficiency. In a further exemplary embodiment, each 32-bit bitmap section **522** may be a three-dimensional 32-bit bitmap.

FIGS. 6A–6E describe operations of the image encoder engine **202** (FIG. 2). In flowchart **600**, a general operation of the image encoder engine **202** is shown. In block **602**, a data string **500** (FIG. 5A) of the original image **310** (FIGS. 3A and 3B), which includes the α-bit header **502** (FIG. 5A) and the β-bit image data **504** (FIG. 5A), is input into the image

decomposer **302** (FIGS. 3A and 3B). The image decomposer **302** decomposes the image **310** into the α-bit header and a plurality of blocks in block **604**. The α-bit header **502** is then forwarded to the header converter **304** (FIGS. 3A and 3B). Subsequently, the header converter **304** generates a modified header **512** (FIG. 5B) from the α-bit header **502** in block **606**. The modified header **512** is then forwarded to the encoded image composer **308** (FIGS. 3A and 3B).

Simultaneous with the header conversion process, each image block **320** is encoded in block **608** by one or more of the block encoders **306***a*–**306***n* (FIGS. 3A and 3B) to generate the encoded image blocks **516** (FIG. 5B). Each image block **320** may be processed sequentially in one block encoder **306**, or multiple image blocks **320** may be processed in parallel in multiple block encoders **306***a*–**306***n*.

The encoded image blocks **516** are output from the block encoders **306**, and are placed into a predefined order by the encoded image composer **308**. In one embodiment, the encoded image blocks **516** are arranged in a file from left to right and top to bottom in the same order in which the encoded image blocks **516** were broken down by the image decomposer **302** (FIGS. 3A and 3B). The image encoder engine **202** subsequently composes the modified header information **512** from the header converter **304** and the encoded image blocks **516***a*–**516***q* in block **610**. Specifically, the modified header **512** and the ordered encoded image blocks **516** are concatenated to generate the encoded image data file **510** (FIG. 5B), which may be written as encoded output **312** (FIGS. 3A and 3B) to the memory **104**, storage device **106**, or any output device **110** (FIG. 1) in block **612**.

FIG. **6B** is a flowchart **620** showing the encoding process of block **608** (FIG. 6A) in more detail. In block **622**, codewords **520** (FIG. 5C) are computed by the codeword generation module **410** (FIG. 4). The process for computing these codewords **520** is described in more detail in connection with FIG. **6C**.

Once the codewords **520** have been computed, pixel values or properties, such as colors, for the image block **320** (FIG. 3C) are computed or quantized in block **624**. Specifically, the codewords **520** provide points in a pixel space from which m quantized pixel values may be inferred. The m quantized pixel values are a limited subset of pixels in a pixel space that are used to represent the current image block. The process for quantizing pixel values, and more specifically colors, will be described infra in connection with FIGS. **8A** and **8B**. Further, the embodiments will now be described with respect to colors of a pixel value although one skilled in the art will recognize that, in general, any pixel value may be used with respect to the present invention. Therefore, the image data which is quantized may be any form of scalar or vector data, such as density values, transparency values, and "bump map" vectors.

In an exemplary embodiment, each pixel is encoded with two bits of data which can index one or m quantized colors, where m=4 in this embodiment. Further, four quantized colors are derived from the two codewords **520** where two colors are the codewords **520**, themselves, and the other two colors are inferred from the codewords **520**, as will be described below. It is also possible to use the codewords **520** so that there is one index to indicate a transparent color and three indices to indicate colors, of which one color is inferred.

In another embodiment, the bitmap **522** (FIG. 5C) is a 32-bit data string. The bitmap **522** and codewords **520** are output in block **624** as a 64-bit data string representing an encoded image block **518**. Specifically, the encoded image block **514** (FIG. 5B) includes two 16-bit codewords **520** (n=16) and a 32-bit bitmap **522**. Every codeword **520** that is a 16-bit data string includes a 5-bit red-channel, 6-bit green-channel, and 5-bit blue-channel.

Each of the encoded image blocks **516** is placed together and concatenated with modified header information **512** derived from the original α-bit header **502** of the original image **310** (FIGS. 3A and 3B). A resulting output is the encoded image data **510** representing the original image **310**.

FIG. **6C** is a flowchart **630** illustrating a process for computing codewords for the image blocks **320** (FIG. 3C), and relates to color quantizing using quantizer **402** (FIG. 4). The process for computing codewords can be applied to all scalar and vector image data types. In select block type **632**, the quantizer **402** uses the block type module **406** (FIG. 4) to select a first block type for the image block **320** that is being processed. For example, a selected block type may be a four-color or a three-color plus transparency block type, where the colors within the particular block type have equidistant spacing in a color space. Those of ordinary skill in the art will readily recognize that selecting a block type for each image is not intended to be limiting in any way. Instead, the present invention processes image blocks that are of a single block type, which eliminates the need to distinguish between different block types, such as the three- and four-color block types discussed above. Consequently, the block type module **406** and select block type **632** are optional.

Once the block type is selected, the quantizer **402** computes an optimal analog curve for the block type in block **634**. Computation of the optimal analog curve will be further described in connection with FIG. **6D**. The analog curve is used to simplify quantizing of the colors in the image block. Subsequently in block **636**, the quantizer **402** selects a partition of points along the analog curve, which is used to simplify quantizing of the colors in the image block. A partition may be defined as a grouping of indices {1 . . . (W×H)} into m nonintersecting sets. In one embodiment, the indices (1 . . . 16) are divided into three or four groups or clusters (i.e., m=3 or 4) depending on the block type.

Once a partition is selected, optimal codewords for the particular partition are computed in block **638**. In addition to computing the codewords, an error value (square error as described infra) for the codeword is also computed in block **640**. Both computations will be described in more detail in connection with FIG. **6E**. If the computed error value is the first error value, the error value is stored in block **642**. Alternatively, the computed error value is stored if it is less than the previously stored error value. For each stored error value, corresponding block type and codewords are also stored in block **644**. The process of flowchart **630** seeks to find the block type and codewords that minimize the error function.

Next in block **646**, the code generation module **410** (FIG. 4) determines if all possible partitions are completed. If there are more partitions, the code generation module **410** selects the next partition, computes the codewords and associated error values, and stores the error values, associated block types, and codewords if the error value is less than the previously stored error value.

After all the possible partitions are completed, the codeword generation module **410** determines, in block **648**, whether all block types have been selected. If there are more block types, the codeword generation module **410** selects the next block type and computes the codeword and various

values as previously described. After the last block type has been processed, the codeword generation module **410** outputs a result of the block type and codewords **520** (FIG. 5C) having the minimum error in block **650**.

In an alternative embodiment, the optimal analog curve may be computed before selecting the block type. That is, the optimal analog curve is computed before the selection of the block type and partition, computation of the codewords and error values, and storage of the error value, block type, and codeword. Computing the optimal analog curve first is useful if all block types use the same analog curve and color space because the analog curve does not need to be recomputed for each block type.

FIG. 6D is a flowchart **660** describing a process of identifying the optimal analog curve. The curve selection module **408** (FIG. 4) first computes a center of gravity for pixel colors of an image block **320** (FIG. 3C) in block **662**. The center of gravity computation includes averaging the pixel colors. Once the center of gravity is computed, a vector in color space is identified in block **664** to minimize the first moment of the pixel colors of the image block **320**. Specifically for identifying a vector, a straight line is fit to a set of data points, which are the original pixel colors of the image block **320**. The straight line is chosen passing through the center of gravity of the set of data points such that it minimizes a "moment of inertia" (i.e., square error). For example, to compute a direction of a line minimizing the moment of inertia for three pixel properties, tensor inertia, T, is calculated from individual colors as follows:

$$T=\sum_{i=1}^{W\times H}\begin{bmatrix} C_{1i}^2+C_{2i}^2 & -C_{0i}C_{1i} & -C_{0i}C_{2i} \\ -C_{0i}C_{1i} & C_{0i}^2+C_{2i}^2 & -C_{1i}C_{2i} \\ -C_{0i}C_{2i} & -C_{2i}C_{1i} & C_{0i}^2+C_{1i}^2 \end{bmatrix}.$$

where C_0, C_1, and C_2 represent pixel properties (e.g., color components in RGB or YUV) relative to a center of gravity. In one embodiment of an RGB color space, C_{0i} is a value of red, C_{1i} is a value of green, and C_{2i} is a value of blue for each pixel, i, of the image block. Further, i takes on integer values from 1 to WxH, so that if W=4 and H=4, i ranges from 1 to 16.

An eigenvector of tensor inertia, T, with the smallest eigenvalue is calculated in block **666** using conventional methods. An eigenvector direction along with the calculated gravity center, defines an axis that minimizes the moment of inertia. This axis is used as the optimal analog curve, which in one embodiment, is a straight line. Those of ordinary skill in the art will readily recognize that the optimal analog curve is not limited to a straight line, but may include a set of parameters, such as pixel values or colors, that minimizes the moment of inertia or mean-square-error when fit to the center of gravity of the pixel colors in the image block. The set of parameters may define any geometric element, such as a curve, plate, trapezoid, or the like.

FIG. 6E is a flowchart **670** describing the process undertaken by the codeword generation module **410** (FIG. 4) for selecting the partitions, computing the codewords and associated error for the partitions, and storing the error value, block type, and codeword if the error value is less than a previously stored error value. In block **672**, the codeword generation module **410** projects the WxH color values onto the previously constructed optimal analog curve. The value of WxH is the size in number of pixels of an image block **320** (FIG. 3C). In one embodiment where W and H are both four pixels, WxH is 16 pixels.

Subsequently in block **674**, the colors are ordered sequentially along the analog curve based on a position of the color on a one-dimensional analog curve. After the colors are ordered, the codeword generation module **410** searches, in block **676**, for optimal partitions. Thus, the codeword generation module **410** takes the WxH colors (one color associated with each pixel) that are ordered along the analog curve and partitions and groups the colors into a finite number of clusters with a predefined relative spacing. In one embodiment where W=4 and H=4 (i.e., WxH is 16), the 16 colors are placed in three and four clusters (i.e., m=3 or 4).

In conducting the search for the optimal partition, a color selection module within the codeword generation module **410** finds the best m clusters from the WxH points projected onto the optimal curve, so that the error associated with the selection is minimized. The best m clusters are determined by minimizing the mean-square-error with the constraint that the points associated with each cluster are spaced to conform to the predefined spacing.

In one embodiment for a block type of four equidistant colors, the error may be defined as a square error along the analog curve, such as

$$E^2=\sum_{cluster\,0}(x_i-p_0)^2+\sum_{cluster\,1}\left[x_i-\left(\frac{2}{3}p_0+\frac{1}{3}p_1\right)\right]^2+\sum_{cluster\,2}\left[x_i-\left(\frac{1}{3}p_0+\frac{2}{3}p_1\right)\right]^2+\sum_{cluster\,3}(x_i-p_1)^2$$

where E is the error for the particular grouping or clustering, p_0 and p_1 are the coded colors, and x_i are the projected points on the optimal analog curve.

In instances where the block type indicates three equidistant colors, the error may be defined as a squared error along the analog curve, such as

$$E^2=\sum_{cluster\,0}(x_i-p_0)^2+\sum_{cluster\,1}\left[x_i-\left(\frac{1}{2}p_0+\frac{1}{2}p_1\right)\right]^2+\sum_{cluster\,2}(x_i-p_1)^2$$

After the resulting optimal codewords **520** are identified, the codewords **520** are forwarded to the bitmap construction module **404** (FIG. 4). The bitmap construction module **404** uses the codewords **520** to identify the m colors that may be specified or inferred from those codewords **520** in block **678**. In one embodiment, the bitmap construction module **404** uses the codewords **520** (e.g., CW_0 and CW_1) to identify the three or four colors that may be specified or inferred from those codewords **520**.

Next in block **680**, the bitmap construction module **404** constructs a block bitmap **522** (FIG. 5C) using the codewords **520** associated with the image block **320** (FIG. 3C). Colors in the image block **320** are mapped to the closest color associated with one of the quantized colors specified by, or inferred from, the codewords **520**. The result is a color index, referenced as ID, per pixel in the block identifying the associated quantized color.

Information indicating the block type is implied by the codewords **520** and the bitmap **522**. In one embodiment, the order of the codewords **520** indicate the block type. If a numerical value of CW_0 is greater than a numerical value of CW_1, the image block is a four-color block. Otherwise, the block is a three-color plus transparency block.

In one embodiment discussed above, there are two-color image block types. One color image block type has four equidistant colors, while the other color image block type has three equidistant colors with the fourth color index used to specify that a pixel is transparent. For both color image block types, the color index is two bits. In an embodiment

with density values in place of color values, each density image block type has four equidistant density values.

The output of the bitmap construction module **404** is an encoded image block **514** (FIG. 5B) having the m codewords **520** plus the bitmap **522**. Each encoded image block **516** is received by the encoded image composer **308** (FIGS. 3A and 3B) that, in turn, orders the encoded image blocks **516** in a file. In one embodiment, the encoded image blocks **516** are arranged from left to right and from top to bottom in the same order as the blocks were broken down by the image decomposer **302**. The ordered file having the encoded image blocks **516** is concatenated with the modified header information **512** that is derived from the α-bit header **502** of the original image **310** (FIGS. 3A and 3B) to generate the encoded image data **510** that is the output of the image encoder engine **202** (FIG. 2). The output may then be forwarded to the memory **104**, the storage device **106**, or the output device **110** (FIG. 1).

The exemplary embodiment of the image encoder engine **202** advantageously reduces the effective data size of an image from 24-bits per pixel to 4-bits per pixel. Further, the exemplary embodiment beneficially addresses transparency issues by allowing codewords to be used with a transparency identifier.

FIG. 7A is a block diagram of an exemplary image decoder engine **204** (FIG. 2). The image decoder engine **204** includes an encoded image decomposer **702**, a header converter **704**, one or more block decoders **706** (**706***a*–**706***p*, where p represents the last block decoder), and an image composer **708**. The encoded image decomposer **702** is coupled to received the encoded image data **514** (FIG. 5B) output from the image encoder engine **202** (FIG. 2). The encoded image decomposer **702** receives the encoded image data string **510** and decomposes, or breaks, the encoded image data string **510** into the header **512** (FIG. 5B) and the encoded image blocks **514** (FIG. 5B). Next, the encoded image decomposer **702** reads the modified header **512**, and forwards the modified header **512** to the header converter **704**. The encoded image decomposer **702** also decomposes the encoded image data string **510** into the individual encoded image blocks **516** (FIG. 5B) that are forwarded to the one or more block decoders **706**.

The header converter **704** converts the modified header **512** into an output header. Simultaneously, the encoded image blocks **516** are decompressed or decoded by the one or more block decoders **706**. Each encoded image block **516** may be processed sequentially in one block decoder **706**, or multiple encoded image blocks **514** may be processed in parallel with one block decoder **706** for each encoded image block **516**. Thus, multiple block decoders **706** allow for parallel processing that increases the processing performance and efficiency of the image decoder engine **204** (FIG. 2).

The image composer **708** receives each decoded image blocks from the one or more block decoders **706** and orders the decoded image block in a file. Further, the image composer **708** receives the converted header from the header converter **704**. The converted header and the decoded image blocks are placed together to generate output data representing the original image **310**.

FIG. 7B is a block diagram of an exemplary embodiment of a block decoder **706**. Each block decoder **706** includes a block type detector **710**, one or more decoder units **712**, and an output selector **714**. The block type detector **710** is coupled to the encoded image decomposer **702** (FIG. 7A), the output selector **714**, and each of the one or more decoder units **712**.

The block type detector **710** receives the encoded image blocks **514** and determines the block type for each encoded image block **516** (FIG. 5B). The block type is detected based on the codewords **520** (FIG. 5C). After the block type is determined, the encoded image blocks **514** are passed to each of the decoder units **712**, which decompress or decode each encoded image block **516** to generate colors for each particular encoded image block **516**. The decoder units **712** may be c-channels wide (e.g., one channel for each color component or pixel property being encoded), where c is any integer value. Using the selector signal, the block type detector **710** enables the output selector **714** to output the color of each encoded image block **516** from one of the decoder units **712** that corresponds with the block type detected by the block type detector **710**. Specifically, the block type detector **710** passes a selector signal to the output selector **714** that is used to select an output corresponding to the block type detected. Alternatively, using the selector signal, the appropriate decoder unit **712** could be selected so that the encoded block is only processed through the selected decoder unit.

FIG. 7C is a block diagram of an alternative embodiment of a block decoder **706**. In this embodiment, the block decoder **706** includes a block type detector **720**, a first decoder unit **722**, a second decoder unit **724**, and an output selector **726**. The block type detector **720** is coupled to receive each encoded image block **516** (FIG. 5B), and determine by comparing the codewords **520** (FIG. 5C) of the encoded image block, the block type for each encoded image block **516**. For example, the block type may be four quantized colors or three quantized colors and a transparency. Once the block type is selected and a selector signal is forwarded to the output selector **726**, the encoded image blocks **516** are decoded by the first and second decoder units **722** and **724**, respectively, to produce the pixel colors of each image block. The output selector **726** is enabled by the block type detector **720** to output the colors from the first and second decoder units **722** and **724** that correspond to the block type selected.

FIG. 7D is a logic diagram illustrating an exemplary embodiment of a decoder unit similar to the decoder units **722** and **724** of FIG. 7C. For simplicity, the functionality of each of the first and second decoder units **722** and **724** is merged into the single logic diagram of FIG. 7D. Those skilled in the art will recognize that although the diagram is described with respect to a red-channel of the decoder units, the remaining channels (i.e., the green-channel and the blue-channel) are similarly coupled and functionally equivalent.

The logic diagram illustrating the first and second decoder units **722** and **724** is shown including portions of the block type detector **710**, **720** (FIGS. 7B and 7C, respectively) such as a comparator unit **730**. The comparator unit **730** is coupled to and works with a first 2×1 multiplexer **732***a* and a second 2×1 multiplexer **732***b*. Both 2×1 multiplexers **732***a* and **732***b* are coupled to a 4×1 multiplexer **734** that serves to select an appropriate color to output. The 4×1 multiplexer **734** is coupled to receive a transparency indicator signal that indicates whether or not a transparency (e.g., no color) is being sent. The 4×1 multiplexer **734** selects a color for output based on the value of the color index, referenced as the ID signal, that references the associated quantized color for an individual pixel of the encoded image block **514** (FIG. 5B).

A red-channel **736** of the first decoder unit **722** includes a first and a second red-channel line **738***a* and **738***b* and a first and a second red-color block **740***a* and **740***b*. Along the

path of each red-color block **740***a* and **740***b* is a first full adder **742***a* and **742***b*, a second full adder **744***a* and **744***b*, and carry-look ahead ("CLA") adders **746***a* and **746***b*. The second decoder unit **724** contains similar components as the first decoder unit **722**.

The CLA adder **746***a* of the first red-color block **740***a* path of the first decoder unit **722** is coupled to the first 2×1 multiplexer **732***a*, while the CLA adder **746***b* of the second red-color block **740***b* path of the first decoder unit **722** is coupled to the second 2×1 multiplexer **732***b*. Further, adder **748** of the second decoder unit **724** is coupled to both the first and the second 2×1 multiplexers **732***a* and **732***b*.

FIG. **8**A is a flowchart **800** illustrating an operation of the decoder engine **204** (FIG. **2**) in accordance with an exemplary embodiment of the present invention. For purposes of illustration, the process for the decoder engine **204** will be described with a single block decoder **706** (FIG. **7**A) having two decoder units **722** and **724** as described earlier in connection with FIG. **7**C. Those skilled in the art will recognize that the process is functionally equivalent for decoder systems having more than one block decoder **706** and more than two decoder units **712**, as discussed in connection with FIG. **7**B.

In block **802**, the encoded image decomposer **702** (FIG. **7**A) receives the encoded or compressed image data **510** (FIG. **5**B) from the image encoder engine **202** (FIG. **2**), through the memory **104** (FIG. **1**) or the storage device **106** (FIG. **1**). Next, the encoded image decomposer **702** decomposes the encoded image data **510** by forwarding the modified header **512** (FIG. **5**B) to the header converter **704** (FIG. **7**A) in block **804**.

Subsequently in block **806**, the header converter **704** converts the header information to generate an output header that is forwarded to the image composer **708** (FIG. **7**A). Simultaneously, the one or more block decoders **706** (FIG. **7**A) decode pixel colors for each encoded image block **516** (FIG. **5**B) in block **808**. Each encoded image block **516** may be decoded sequentially in one block decoder **706** or multiple encoded image blocks **514** (FIG. **5**B) may be decoded in parallel in multiple block decoders **706** in block **808**. The process for decoding each encoded image block **516** is further described in connection with FIG. **8**B. Each decoded image block is then composed into a data file with the converted header information by the image composer **708** in block **810**. The image composer **708** then generates the data file as an output that represents the original image **310** (FIGS. **3**A and **3**B).

FIG. **8**B is a flowchart **820** illustrating an operation of the block decoder **706** (FIG. **7**A) in accordance with an exemplary embodiment of the present invention. Initially, each encoded image block **516** (FIG. **5**B) is received by the block decoder **706** in block **822**. Specifically, for one embodiment the first and the second codewords **520** (e.g., CW_0 and CW_1 of FIG. **5**C) are received by the block type detector **710**, **720** (FIGS. **7**B and **7**C, respectively) of the block decoder **706**. As discussed above, comparing the numerical values of CW_0 and CW_1 reveals the block type. The first five bits of each codeword **520** that represent the red-channel color are received by the red-channel of each of the first and second decoder units **722** and **724** (FIG. **7**C). Furthermore, the second 6-bits of each codeword **520** that represent the green-channel color are received by the green-channel of each of the first and the second decoder units **722** and **724**, while the last 5-bits of each codeword **520** that represent the blue-channel color are received by the blue-channel of each of the first and second decoder units **722** and **724**.

Next in block **824**, the block type detector **710** detects the block type for an encoded image block **514**. Specifically, the comparator **730** (FIG. **7**D) compares the first and the second codewords **520** (e.g., CW_0 and CW_1) and generates a flag signal to enable the first 2×1 multiplexer **732***a* or the second 2×1 multiplexer **732***b*. In block **826**, either the first decoder unit **722** or the second decoder unit **724** is selected.

Subsequently quantized color levels for the decoder units **722** and **724** are calculated in block **828**. The calculation of the quantized color levels will now be discussed in more detail. Initially, the first decoder unit **722** calculates the four colors associated with the two codewords **520** (e.g., CW_0 and CW_1) using the following exemplary relationship:

CW_0=first codeword=first color;

CW_1=second codeword=second color;

$$CW_2 = \text{third color} = \frac{2}{3}CW_0 + \frac{1}{3}CW_1; \text{ and}$$

$$CW_3 = \text{fourth color} = \frac{1}{3}CW_0 + \frac{2}{3}CW_1.$$

In one embodiment, the first decoder unit **722** may estimate the above equations for CW_2 and CW_3 as follows:

$$CW_2 = \frac{5}{8}CW_0 + \frac{3}{8}CW_1; \text{ and}$$

$$CW_3 = \frac{3}{8}CW_0 + \frac{5}{8}CW_1.$$

The red-color blocks **740***a* and **740***b* (FIG. **7**D) serve as one-bit shift registers to obtain

$$\frac{1}{2}CW_0 \text{ or } \frac{1}{2}CW_1.$$

Further, each full adder **742***a*, **742***b*, **744***a*, and **744***b* (FIG. **7**D) also serves to shift the signal left by 1-bit. Thus, the signal from the first full adders **742***a* and **742***b* is

$$\frac{1}{4}CW_0 \text{ or } \frac{1}{4}CW_1,$$

respectively, because of a 2-bit overall shift, while the signal from the second full adders **744***a* and **744***b* is

$$\frac{1}{8}CW_0 \text{ or } \frac{1}{8}CW_1,$$

respectively due to a 3-bit overall shift. These values allow for the above approximations for the color signals.

The second decoder unit **724** (FIG. **7**C) calculates three colors associated with the codewords **520** (e.g., CW_0 and CW_1), and includes a fourth signal that indicates a transparency is being passed. The second decoder unit **724** calculates colors using the following exemplary relationship:

CW_0=first codeword=first color;

CW_1=second codeword=second color;

$$CW_3 = \text{third color} = \frac{1}{2}CW_0 + \frac{1}{2}CW_1; \text{ and}$$

T=Transparency.

In one embodiment, the second decoder unit **724** has no approximation because the signals received from the red-

color blocks **740***a* and **740***b* are shifted left by 1-bit so that the color is already calculated to

$$\frac{1}{2}CW_0 \text{ or } \frac{1}{2}CW_1.$$

respectively.

After the quantized color levels for the decoder units **722** and **724** selected in block **826** have been calculated in block **828**, each bitmap value for each pixel is read from the encoded image data block **510** (FIG. 5A) in block **830**. As each index is read, it is mapped in block **832** to one of the four calculated colors if the first decoder unit **722** is selected. Alternatively, one of the three colors and transparency is mapped in block **832** if the second decoder unit **724** is selected. The mapped colors are selected by the 4x1 multiplexer **734** based on the value of the ID signal from the bitmap **522** (FIG. 5C) of the encoded image block **514**. As stated previously, a similar process occurs for selection of colors in the green-channel and the blue-channel.

As the color data are output from the red-channel, green-channel and blue-channel, the output is received by the image composer **708** (FIG. 7A). Subsequently, the image composer **708** arranges the output from the block encoders **706** in the same order as the original image **310** was decomposed. The resulting image is the original image **310**, which is then forwarded to an output unit **208** (FIG. 2; e.g., a computer screen) which displays the image.

This exemplary embodiment beneficially allows for random access to any desired image block **320** (FIG. 3C) within an image, and any pixel **322** (FIG. 3C) within an image block **320**. FIG. 9A is a block diagram of a subsystem **900** that provides random access to a pixel **322** or an image block **320** in accordance with one embodiment of the present invention.

The random access subsystem **900** includes a block address computation module **902**, a block fetching module **904**, and one or more block decoders **706** coupled to the block address computation module **902** and the block fetching module **904**. The block address computation module **902** receives the header information **512** (FIG. 5B) of the encoded image data string **510** (FIG. 5B), while the block fetching module **904** receives the encoded image block portion **514** (FIG. 5B) of the encoded image data string **510**.

FIG. 9B is a flowchart **910** of a process for random access to a pixel **322** (FIG. 3C) or an image block **320** (FIG. 3C) using the random access subsystem **900** of FIG. 9A. When particular pixels **322** have been identified for decoding, the image decoder engine **204** (FIG. 2) receives the encoded image data string **510** (FIG. 5B). The modified header **512** (FIG. 5B) of the encoded image data string **510** is forwarded to the block address computation module **902** (FIG. 9A), and the encoded image block portion **514** (FIG. 5B) of the encoded image data string **510** is forwarded to the block fetching module **904** (FIG. 9A).

In block **912**, the block address computation module **902** reads the modified header **512** to compute an address of the encoded image block portion **514** having the desired pixels **322**. The address computed is dependent upon the pixel coordinates within an image. Using the computed address, the block fetching module **904** identifies each encoded image block **516** (FIG. 5B) of the encoded image block portion **514** that contains the desired pixels **322** in block **914**. Once each encoded image block **516** having the desired pixels **322** has been identified, only the identified encoded image block **516** is forwarded to the block decoders **706** (FIG. 9A) for processing.

FIG. 9B is similar to the process described above in FIG. 8B, wherein the block decoders **706** compute quantized color levels for each identified encoded image blocks **516** having the desired pixels in block **916**. After the quantized color levels have been computed, the color of the desired pixel is selected in block **918** and output from the image decoder engine **204**.

Random access to pixels **322** of an image block **320** (FIG. 3C) advantageously allows for selective decoding of only needed portions or sections of an image. Random access also allows the image to be decoded in any order the data is required. For example, in three-dimensional texture mapping only portions of the texture may be required and these portions will generally be required in some non-sequential order. Thus, this embodiment of the present invention increases processing efficiency and performance when processing only a portion or section of an image. Further, the present invention beneficially encodes or compresses the size of an original image **310** (FIGS. 3A and 3B) from 24-bits per pixel to an aggregate 4-bits per pixel, and then decodes or decompresses the encoded image data string **510** (FIG. 5B) to get a representation of the original image **310**. Additionally, the exemplary embodiment uses two base points or codewords from which additional colors are derived so that extra bits are not necessary to identify a pixel **322** color.

Moreover, the exemplary embodiment advantageously accomplishes the data compression on an individual block basis with the same number of bits per block so that the compression rate can remain fixed. Further, because the blocks are of fixed size with a fixed number of pixels **322**, random access to any particular pixel **322** in the block is allowed. Additionally, an efficient use of system resources is provided because entire blocks of data are not retrieved and decoded to display data corresponding to only a few pixels **322**.

Finally, the use of fixed-rate 64-bit data blocks provides the advantage of having simplified header information that allows for faster processing of individual data blocks. A 64-bit data block allows for faster processing as the need to wait until a full data string is assembled is eliminated. Further, an imaging system in accordance with the present invention may also reduce the microchip space necessary for a decoder system because the decoder system only needs to decode each pixel **322** to a set of colors determined by, for example, the two codewords **520** (FIG. 5C).

The present invention has been described above with reference to specific embodiments. It will be apparent to those skilled in the art that various modifications may be made and other embodiments can be used without departing from the broader scope of the invention. Therefore, these and other variations upon the specific embodiments are intended to be covered by the present invention.

What is claimed is:

1. An image encoder engine for encoding an image, comprising:

an image decomposer for decomposing the image into a header and at least one image block, each image block having a set of image elements and each image element having an original image data value;

at least one block encoder for receiving each image block and for compressing each image block into an encoded image block by associating each original image data value of the image element with an index to a derived image data value in a set of quantized image date values; and

an encoded image composer coupled to the block encoder for ordering the encoded image blocks into a data file.

2. The image encoder engine of claim 1 further comprising a header converter coupled to the image decomposer for converting the header into a modified header.

3. The image encoder engine of claim 2 wherein the encoded image composer orders the encoded image block and the modified header into a data file.

4. The image encoder engine of claim 1 wherein the block encoder further comprises a selection module for computing a set of parameters from the image data values of the set of image elements.

5. The image encoder engine of claim 1 wherein the block encoder further comprises a codeword generation module for generating at least one codeword.

6. The image encoder engine of claim 1 wherein the block encoder further comprises a construction module for generating the set of quantized image data values including at least one codeword and at least one derived image data value.

7. The image encoder engine of claim 1 wherein the block encoder further comprises a block type module for selecting an identifiable block type for the image block.

8. An image decoder engine for decoding an encoded image data file, comprising:

an encoded image decomposer for decomposing the encoded image data file into a modified header and at least one compressed image block, each image block having at least one associated codeword and a plurality of image elements associated with an index value;

at least one block decoder coupled to the encoded image decomposer for decompressing the at least one compressed image block into at least one decompressed image block by generating a set of quantized image data values and mapping the index value to a quantized image data value from the set of quantized image data values; and

an image composer for ordering the at least one decompressed image blocks in an output data file.

9. The image decoder engine of claim 8 wherein the set of quanitized image data values include the at least one codeword and at least one image data value derived from the at least one codeword.

10. The image decoder engine of claim 8 further comprising a header converter coupled to the encoded image decomposer for converting the modified header into an output header.

11. The image decoder engine of claim 10 wherein the image composer orders the at least one decompressed image block and the output header into a data file.

12. The image decoder engine of claim 8 wherein the at least one block decoder further comprises a block type detector for selecting a block type for each of the at least one compressed image block.

13. The image decoder engine of claim 8 wherein the at least one block decoder further comprises a decoder for decompressing each of the at least one compressed image block based on a block type.

14. The image decoder engine of claim 8 wherein the at least one block decoder further comprises an output selector for outputting the at least one decompressed image block.

15. A method for fixed-rate block-based image compression of an original image, comprising the steps of:

decomposing the original image into a header and a plurality of image blocks each having a set of image elements with an original image data value;

computing at least one codeword from the original image data value for the set of image elements;

generating a set of quantized image data values including the at least one codeword and at least one image value derived from the at least one codeword; and

mapping the original image data value to one of the quantized image data values to produce an index value for each image element.

16. The method of claim 15 further comprising outputting an encoded image data file.

17. The method of claim 15 further comprising the step of converting the header into a modified header.

18. The method of claim 17 further comprising the step of composing the modified header and encoded image blocks into the encoded image data file.

19. A machine readable medium having embodied thereon a program being executable by a machine to perform method steps for fixed-rate block-based image compression of an original image, the method steps comprising:

decomposing the original image into a header and a plurality of image blocks each having a set of image elements with an original image data value;

computing at least one codeword from the original image data value for the set of image elements;

generating a set of quantized image data values including the at least one codeword and at least one image value derived from the at least one codeword; and

mapping the original image data value to one of the quantized image data values to produce an index value for each image element.

20. The machine readable medium of claim 19 further comprising the method of outputting an encoded image data file.

21. An image encoder system for encoding an original image, comprising:

means for decomposing the original image into a header and a plurality of image blocks each having a set of image elements with an original image data value;

means for computing at least one codeword from the original image data value for the set of image elements;

means for generating a set of quantized image data values including the at least one codeword and at least one image value derived from the at least one codeword; and

means for mapping the original image data value to one of the quantized image data values to produce an index value for each image element.

22. The image encoder system of claim 21 further comprising means for outputting an encoded image data file.

23. A method for fixed-rate block-based image decompression of an encoded image, comprising the steps of:

decomposing the encoded image of into a modified header and a plurality of encoded image blocks having at least one codeword and a plurality of image elements associated with an index value;

generating a set of quanitized image data values including the at least one codeword and at least one image value derived from the at least one codeword; and

mapping the index value for each image element to one of the quantized image data values.

24. The method of claim 23 further comprising outputting a decoded image data file.

25. The method of claim 23 further comprising the step of converting the modified header into an output header.

26. The method of claim 25 further comprising the step of composing the output header and decoded image blocks into the decoded image data file.

27. A machine readable medium having embodied thereon a program being executable by a machine to perform method steps for fixed-rate block-based image decompression of an encoded image, the method steps comprising:

decomposing the encoded image data file into a modified header and a plurality of encoded image blocks having at least one codeword and a plurality of image elements associated with an index value;

generating a set of quanitized image data values including the at least one codeword and at least one image value derived from the at least one codeword; and

mapping the index value for each image element to one of the quantized image data values.

28. The machine readable medium of claim 27 further comprising the method of outputting a decoded image data file.

29. An image decoder engine for decoding an encoded image data file, comprising means for decomposing the encoded image data file into a modified header and a plurality of encoded image blocks having at least one codeword and a plurality of image elements associated with an index value;

means for generating a set of quanitized image data values including the at least one codeword and at least one image value derived from the at least one codeword; and

means for mapping the index value for each image element to one of the quantized image data values.

30. The image decoder engine of claim 29 further comprising means for outputting a decoded image data file.

* * * * *

Exhibit 11

US007043087B2

(12) **United States Patent**
Hong et al.

(10) **Patent No.: US 7,043,087 B2**
(45) **Date of Patent: May 9, 2006**

(54) **IMAGE PROCESSING SYSTEM**

(75) Inventors: **Zhou Hong**, Cupertino, CA (US); **Konstantine I. Iourcha**, San Jose, CA (US); **Krishna S. Nayak**, Palo Alto, CA (US)

(73) Assignee: **S3 Graphics Co., Ltd.**, Grand Cayman (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/893,084**

(22) Filed: **Jul. 16, 2004**
(Under 37 CFR 1.47)

(65) **Prior Publication Data**

US 2004/0258321 A1 Dec. 23, 2004

Related U.S. Application Data

(63) Continuation of application No. 10/052,613, filed on Jan. 17, 2002, now Pat. No. 6,775,417, which is a continuation-in-part of application No. 09/351,930, filed on Jul. 12, 1999, now Pat. No. 6,658,146, which is a continuation of application No. 08/942,860, filed on Oct. 2, 1997, now Pat. No. 5,956,431.

(51) **Int. Cl.**
G06K 9/36 (2006.01)

(52) **U.S. Cl.** **382/233**; 382/166; 382/232; 382/253

(58) **Field of Classification Search** 382/253, 382/232, 233, 166, 162; 375/240.03, 240.16; 709/247; 370/394
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,821,208	A	4/1989	Ryan et al.	345/550
4,887,151	A	12/1989	Wataya	358/539
5,734,744	A	3/1998	Wittenstein et al.	382/166
5,742,892	A	4/1998	Chaddha	725/146
5,748,904	A	5/1998	Huang et al.	345/544
5,768,535	A *	6/1998	Chaddha et al.	709/247
5,787,192	A	7/1998	Takaichi et al.	382/166
5,822,465	A	10/1998	Normile et al.	382/253
5,956,425	A	9/1999	Yoshida	382/234

(Continued)

FOREIGN PATENT DOCUMENTS

JP 401 284 188 11/1989

(Continued)

OTHER PUBLICATIONS

A. Schilling, et al.; "Texram: A Smart Memory for Texturing"; IEEE Computer Graphics & Applications; May 1996; 16(3) pp. 9-19.

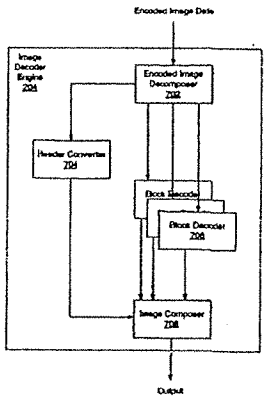
(Continued)

Primary Examiner—Anh Hong Do
(74) *Attorney, Agent, or Firm*—Carr & Ferrell LLP

(57) **ABSTRACT**

An image processing system including an image encoder and image decoding system is provided. The image encoder system includes an image decomposer, a block encoder, and an encoded image composer. The image decomposer decomposes the image into blocks. The block encoder, which includes a selection module, a codeword generation module and a construction module, processes the blocks. Specifically, the selection module computes a set of parameters from image data values of a set of image elements in the image block. The codeword generation module generates codewords, which the construction module uses to derive a set of quantized image data values. The construction module then maps each of the image element's original image data values to an index to one of the derived image data values. The image decoding system reverses this process to reorder decompressed image blocks in an output data file.

8 Claims, 16 Drawing Sheets



U.S. PATENT DOCUMENTS

5,956,431	A	9/1999	Iourcha et al.	382/253
6,075,619	A	6/2000	Iizuka	382/166
6,088,392	A *	7/2000	Rosenberg	375/240.03
6,658,146	B1	12/2003	Iourcha et al.	382/166
6,775,417	B1 *	8/2004	Hong et al.	382/253
2004/0258322	A1	12/2004	Hong et al.	382/253

FOREIGN PATENT DOCUMENTS

JP	405 216 993	8/1993

OTHER PUBLICATIONS

G. Knittel, et al.; "Hardware and Software for Superior Texture Performance": In 10; Eurographics Hardware Workshop '95; Maastricht, NL; Aug. 28-29, 1995; pp. 1-8.

G. Campbell, et al.; "Two Bit/Pixel Full Color Encoding"; Computer Graphics, (Proc. Siggraph '86); Aug. 18-22, 1986; vol. 20, No. 4, Dallas TX; pp. 215-219.

Feng et al., "A Dynamic Address Vector Quantization Algorithm . . . ", IEEE Int'l Conf. on Acoustics, Speech & Signal Proc., vol. 3, May 1989, pp. 1755-1758.

Yang et al., "Hybrid Adaptive Block Truncation Coding for Image Compression," Optical Eng., Soc. of Photo-Optical Instr. Eng., vol. 36, No. 4, Apr. 1, 1997 pp. 1021-1027.

Kugler, "High-Performance Texture Decompression Hardware," Visual Computer, Springer, Berlin, Germany, vol. 13, No. 2, 1997, pp. 51-63.

Panos Nasiopoulos et al., "Adaptive Compression Coding," IEEE Transactions on Communications, IEEE Inc., New York, USA, vol. 39, No. 8, Aug. 1, 1991, pp. 1245-1254.

Delp E.J. et al., "Image Compression Using Block Truncation Coding," IEEE Inc., New York, USA, vol. COM-27, No. 9, Sep. 1979, pp. 1335-1342.

Yang et al., "Use of Radius Weighted Mean to Cluster Two-Class Data," Electronics Letters, IEE Stevenage, Great Britain, vol. 30, No. 10, May 12, 1994, pp. 757-759.

Russ, J.C. et al., "Optimal Grey Scale Images from Multiplane Color Images," Journal of Computer-Assisted Microscopy, Dec. 1995, Plenum, USA, vol. 7, No. 4, pp. 221-233.

Knittel et al., "Hardware for Superior Texture Performance," Eurographics Workshop on Graphics Hardware, Jul. 28, 1995, pp. 33-40.

* cited by examiner

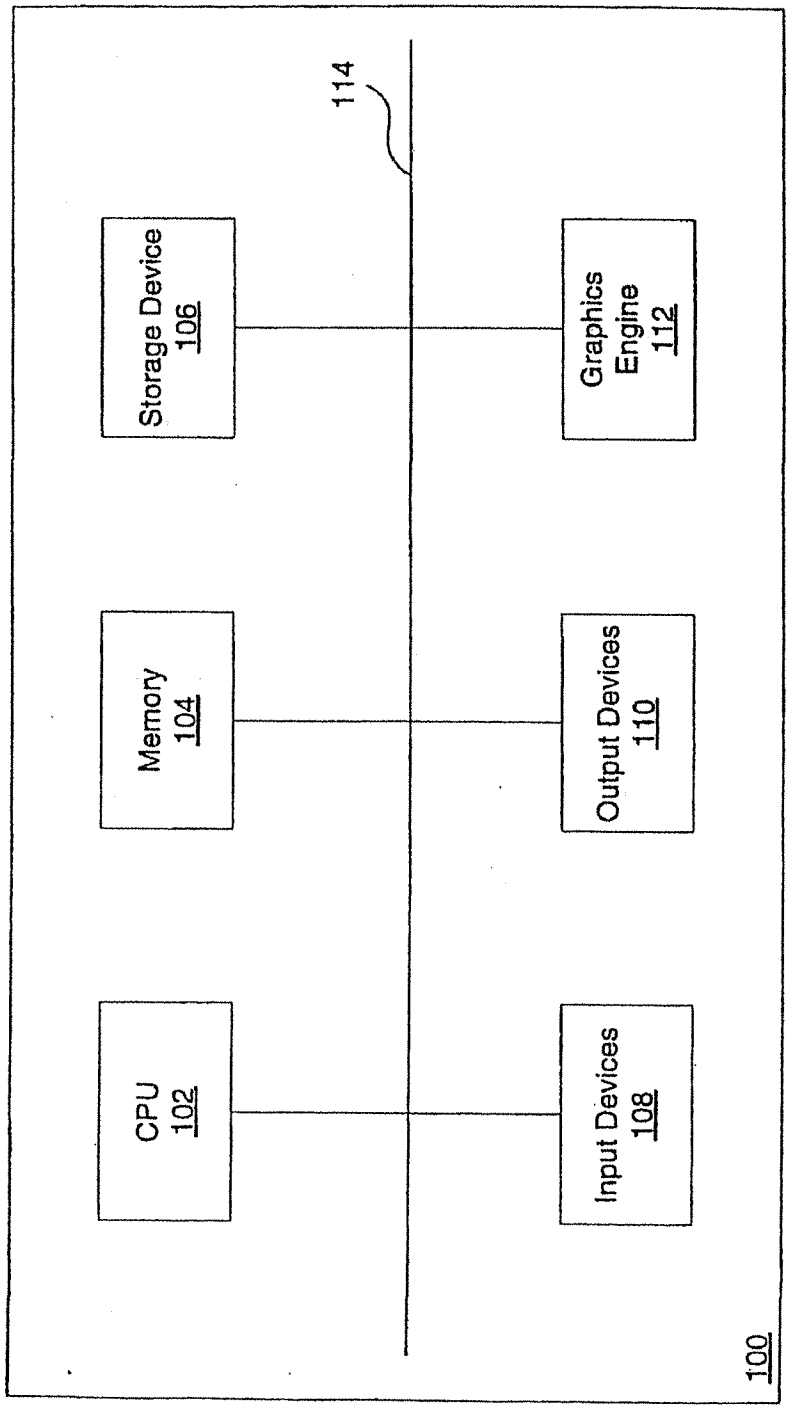


FIG. 1

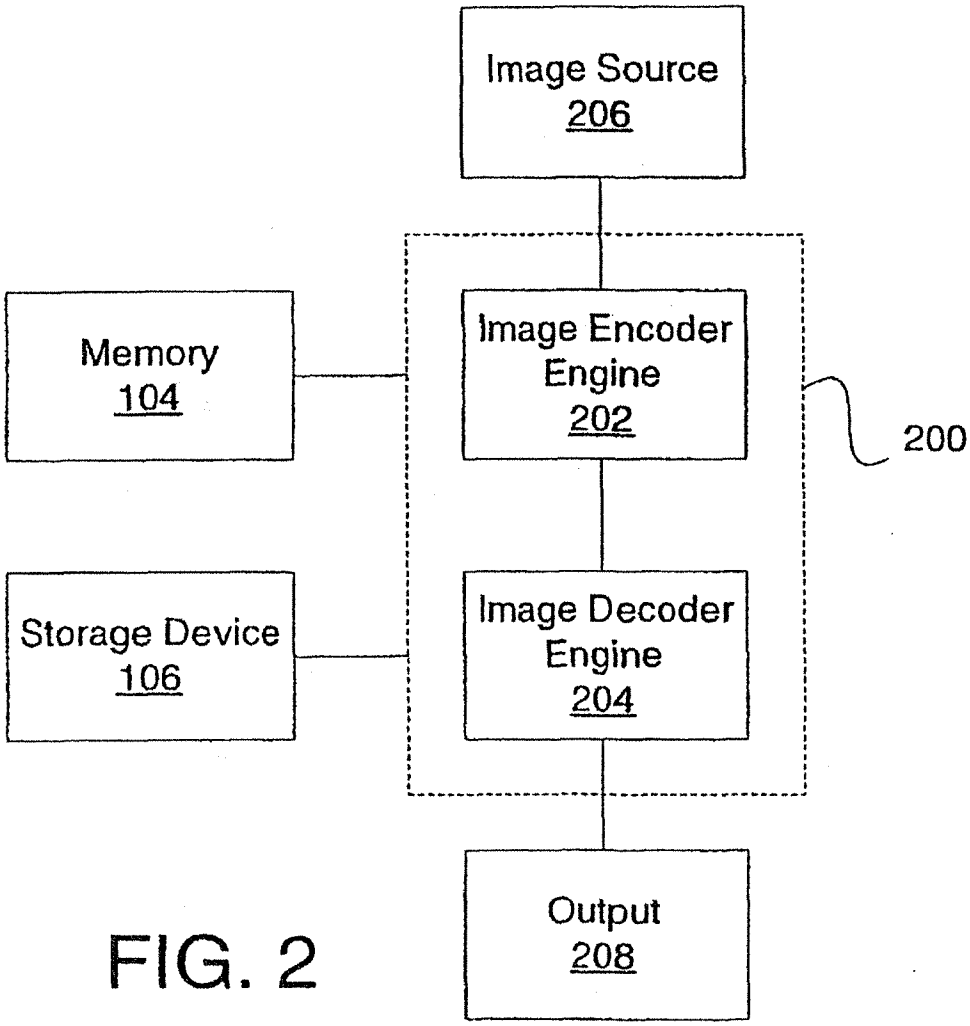


FIG. 2

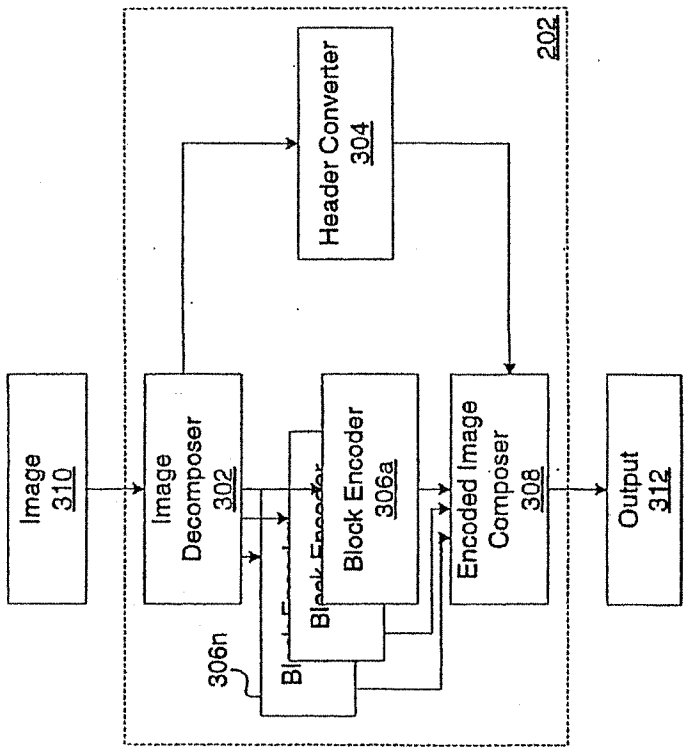


FIG. 3B

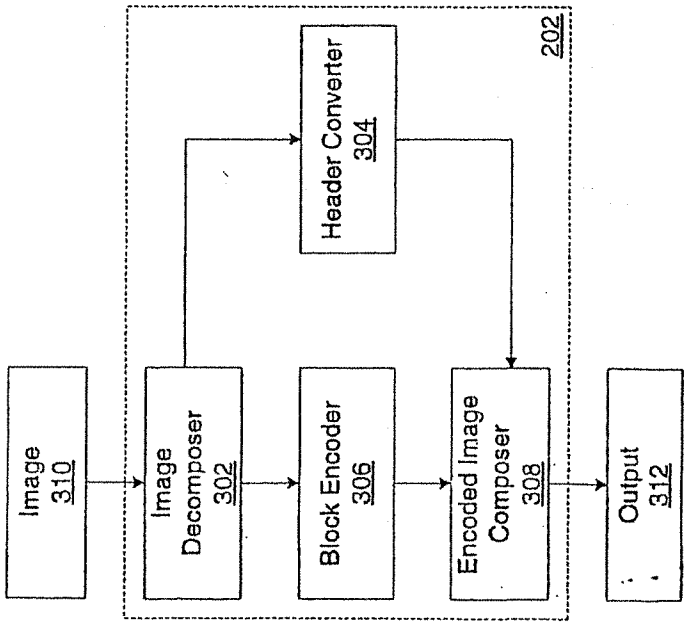


FIG. 3A

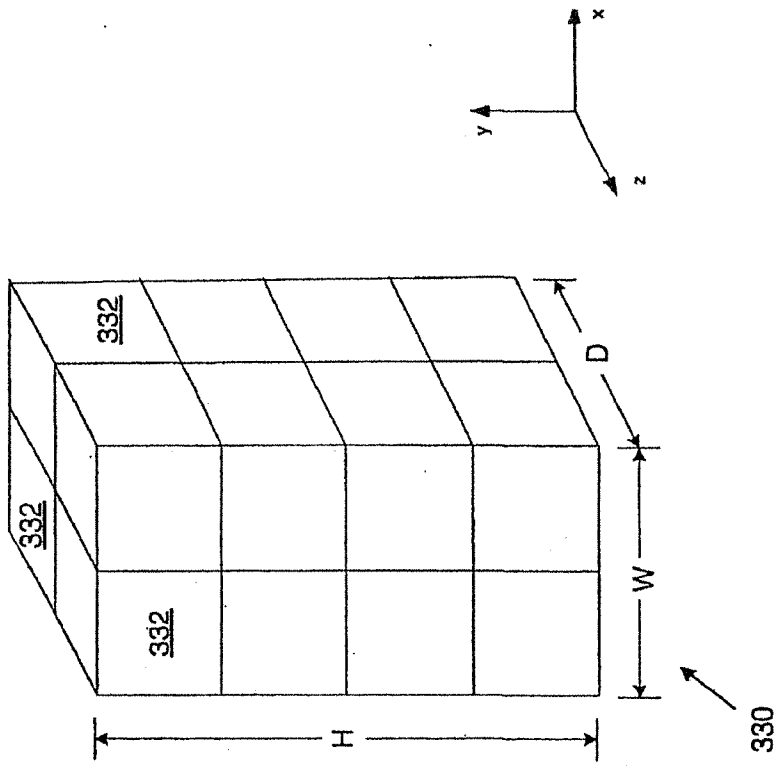


FIG. 3D

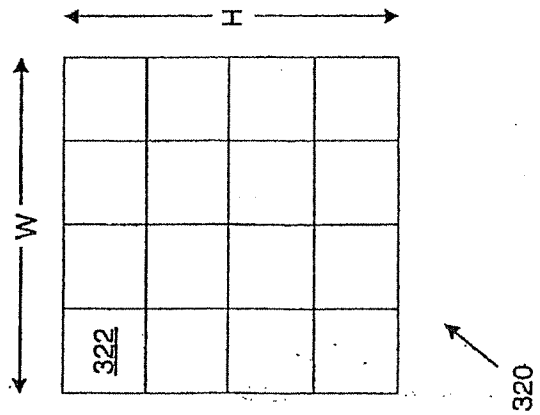


FIG. 3C

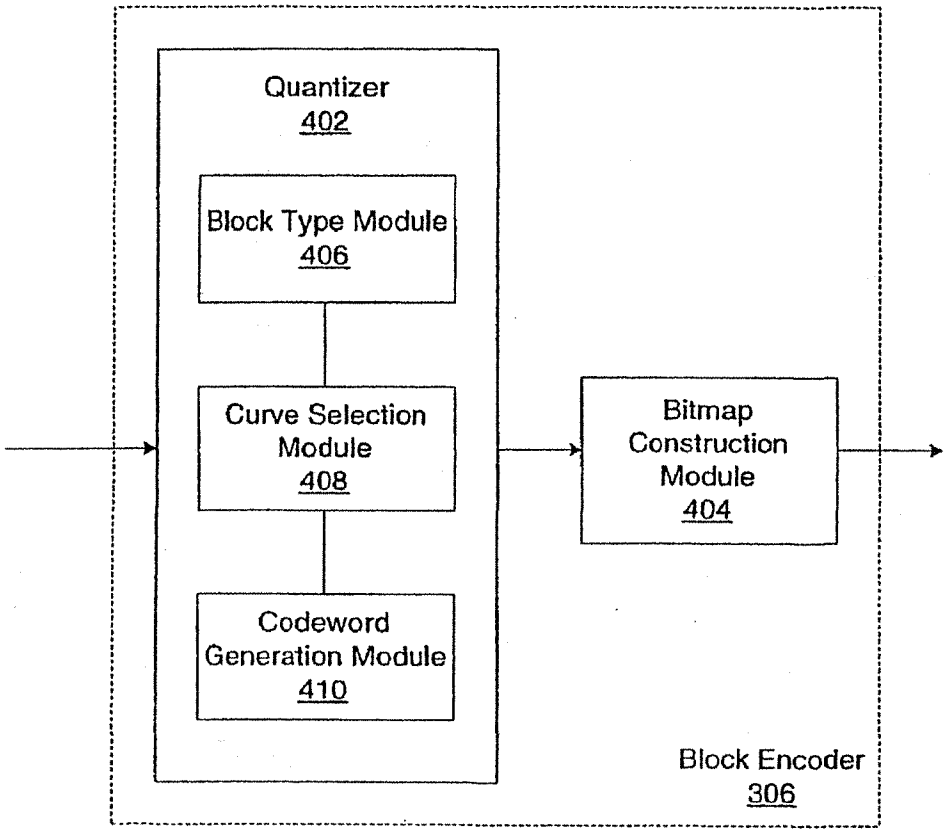


FIG. 4

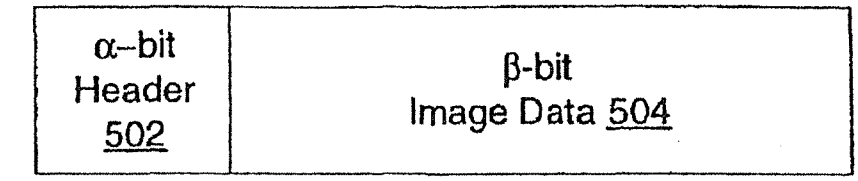


FIG. 5A

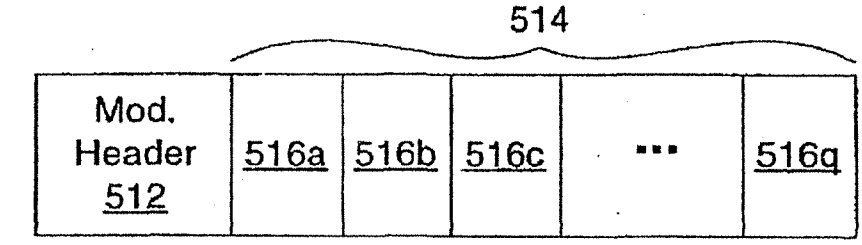


FIG. 5B

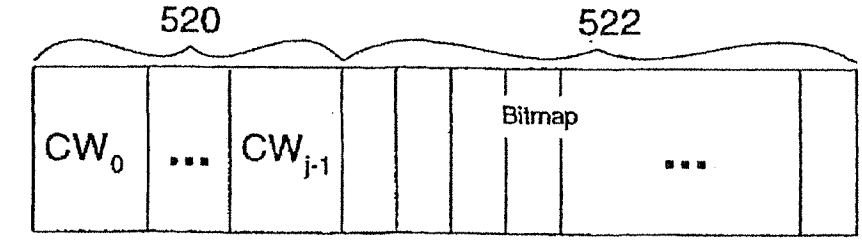


FIG. 5C

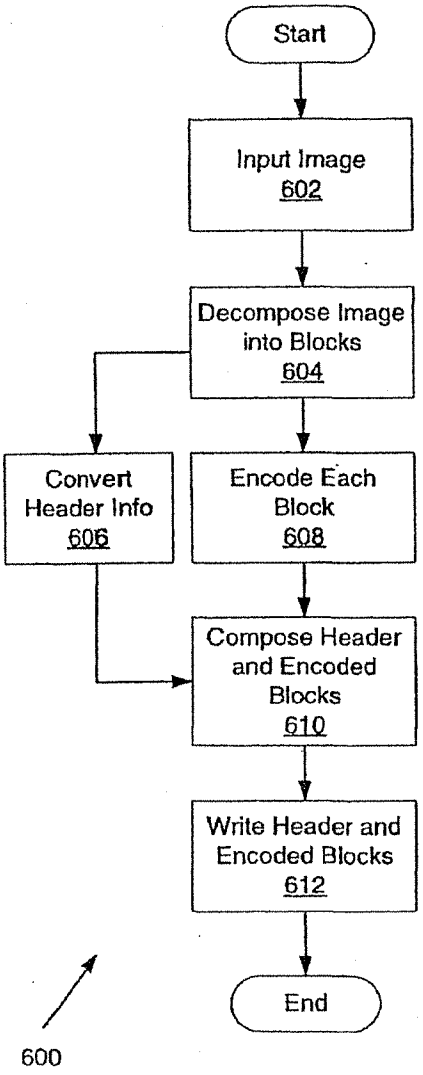


FIG. 6A

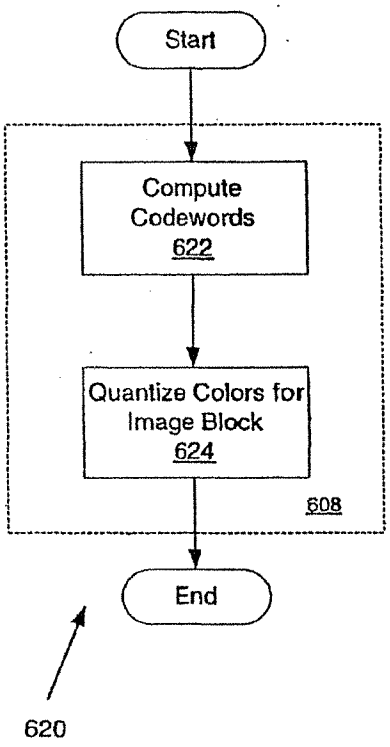


FIG. 6B

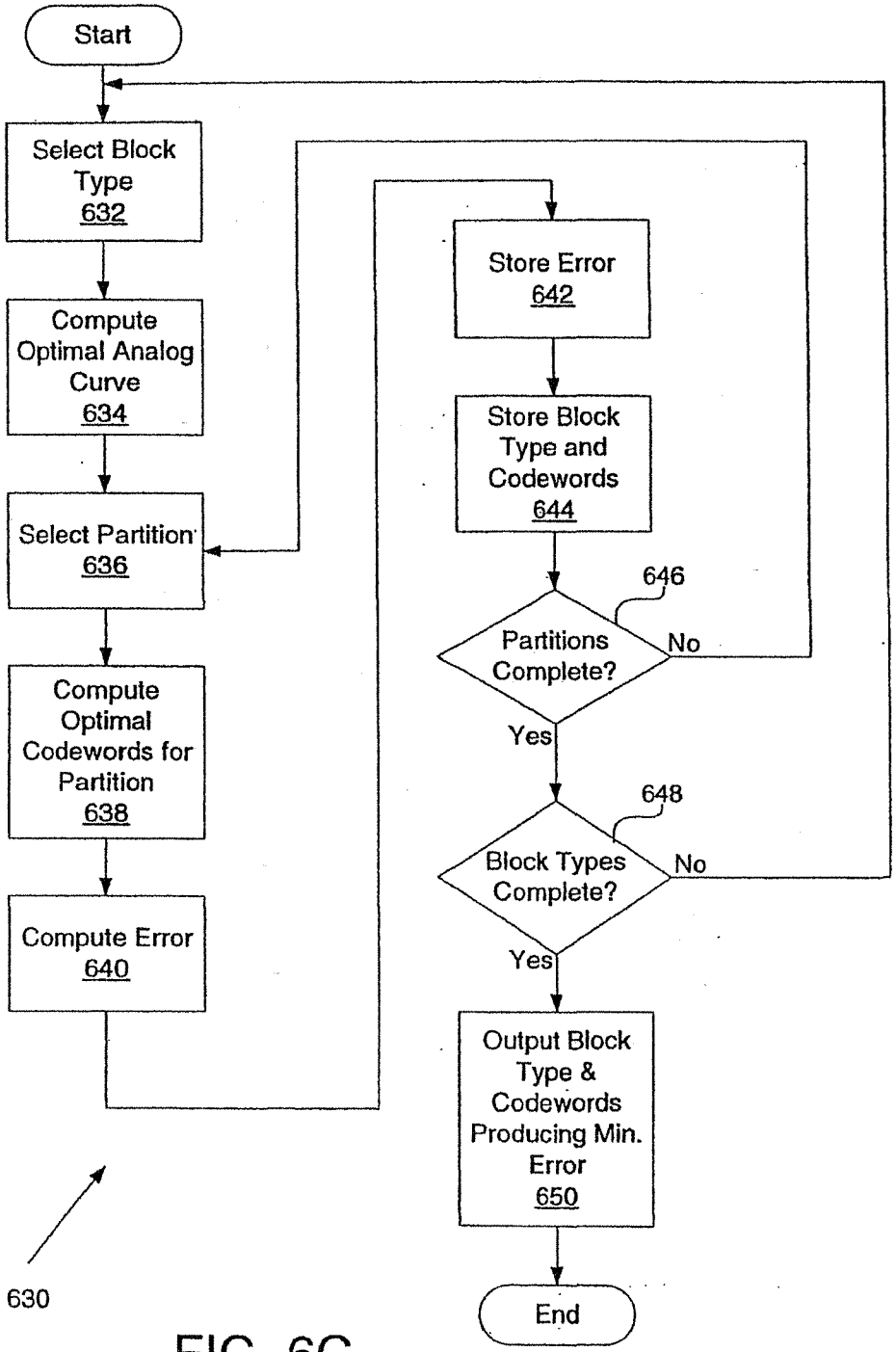


FIG. 6C

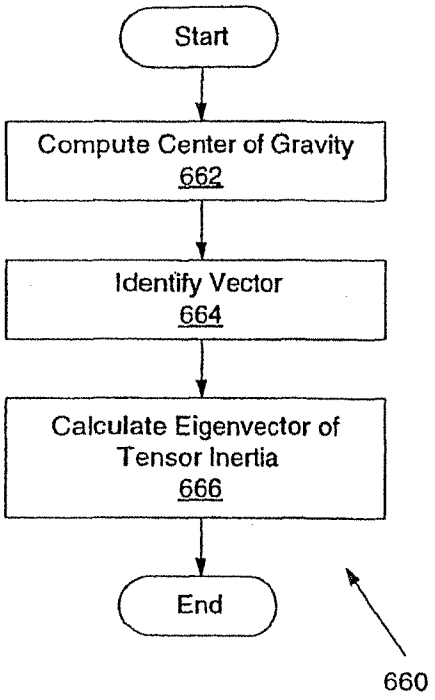


FIG. 6D

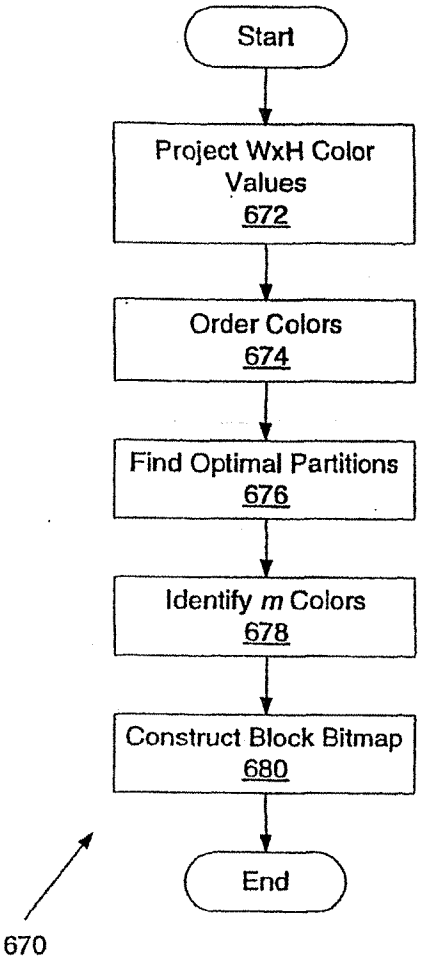


FIG. 6E

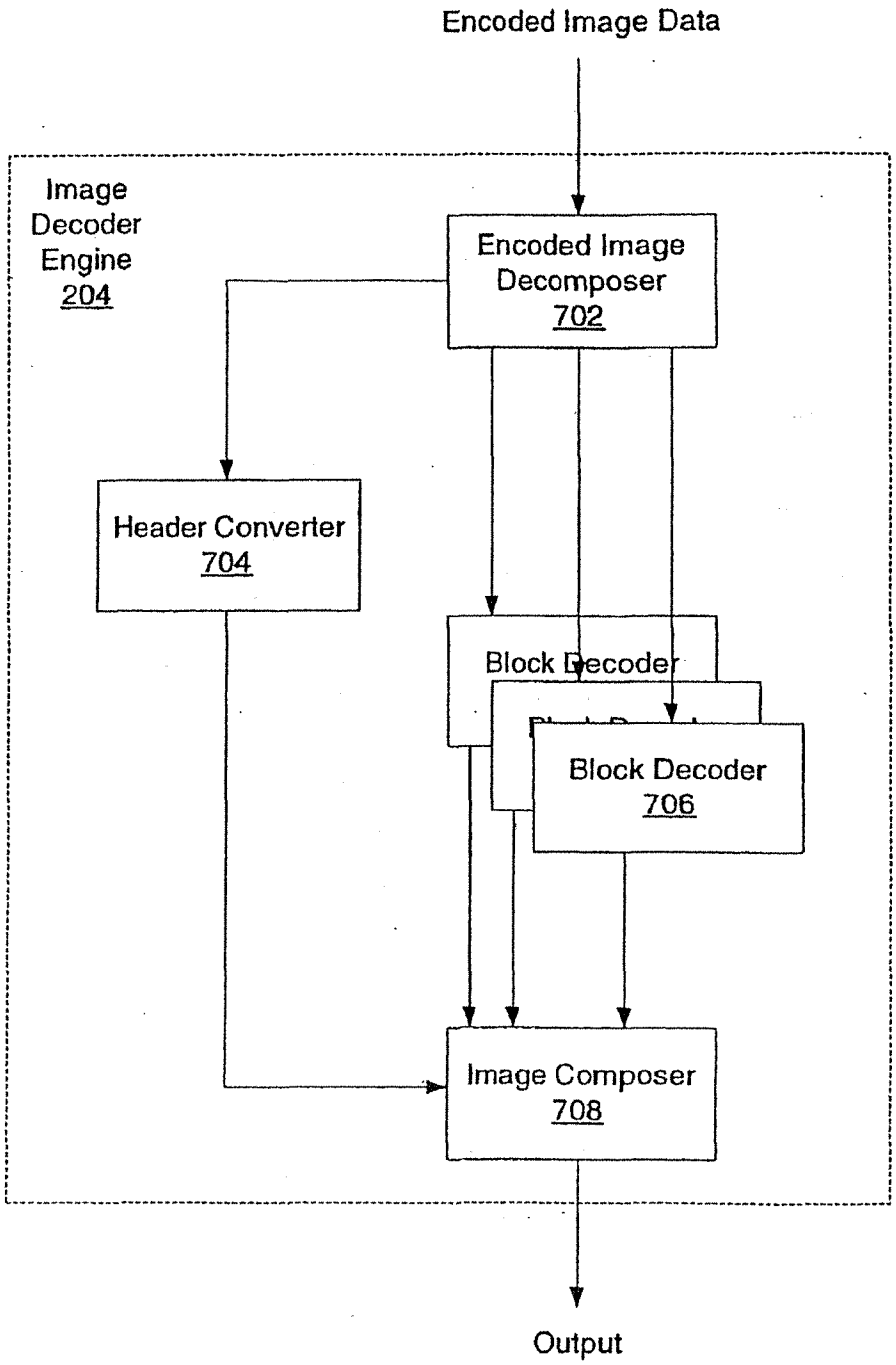


FIG. 7A

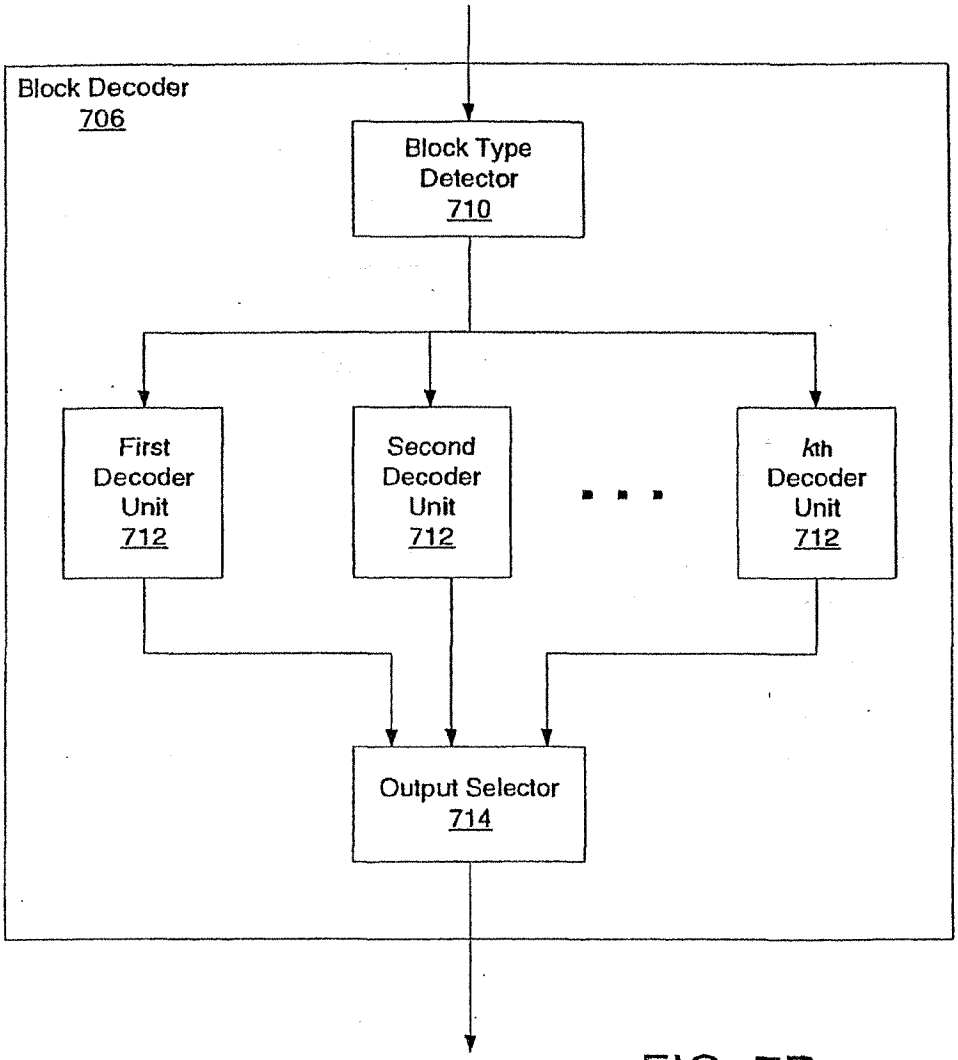


FIG. 7B

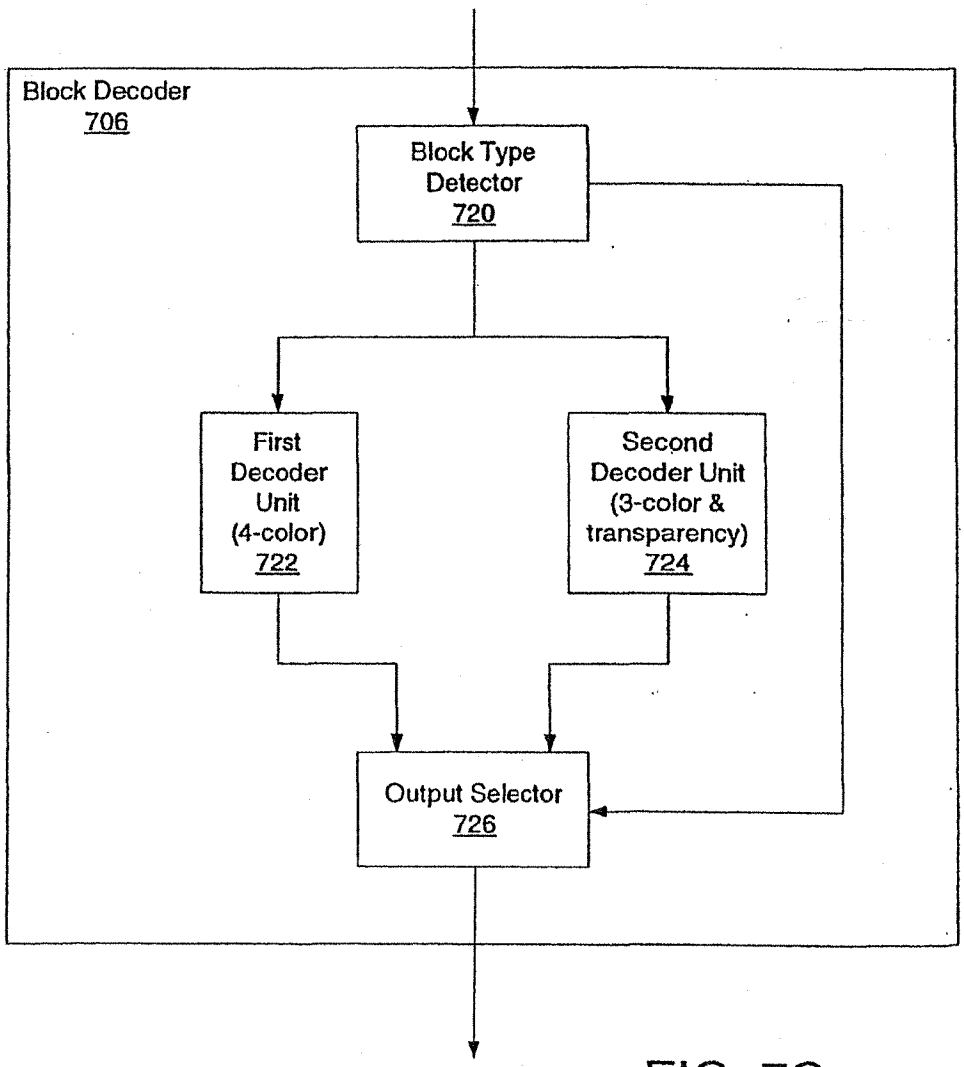


FIG. 7C

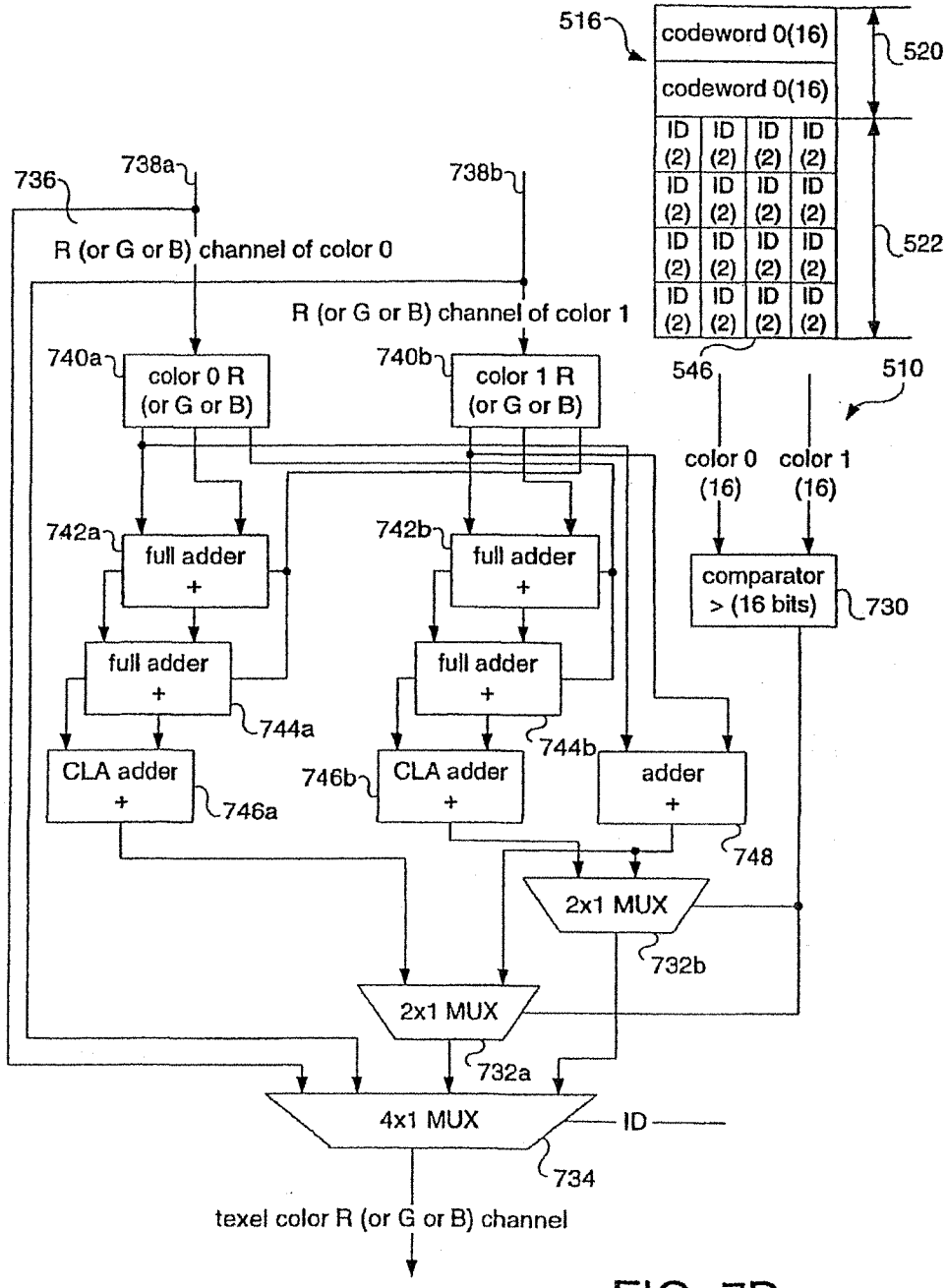


FIG. 7D

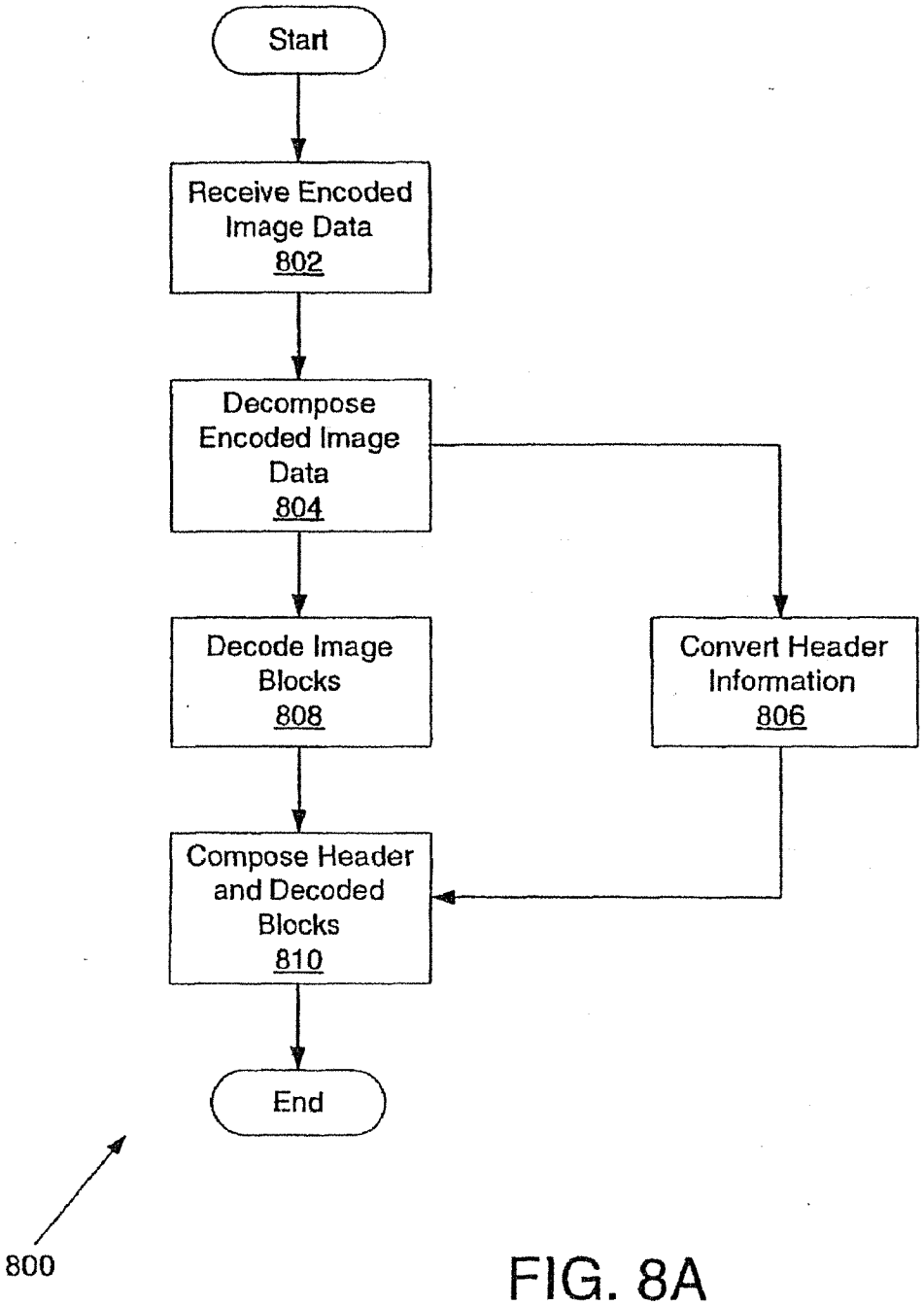


FIG. 8A

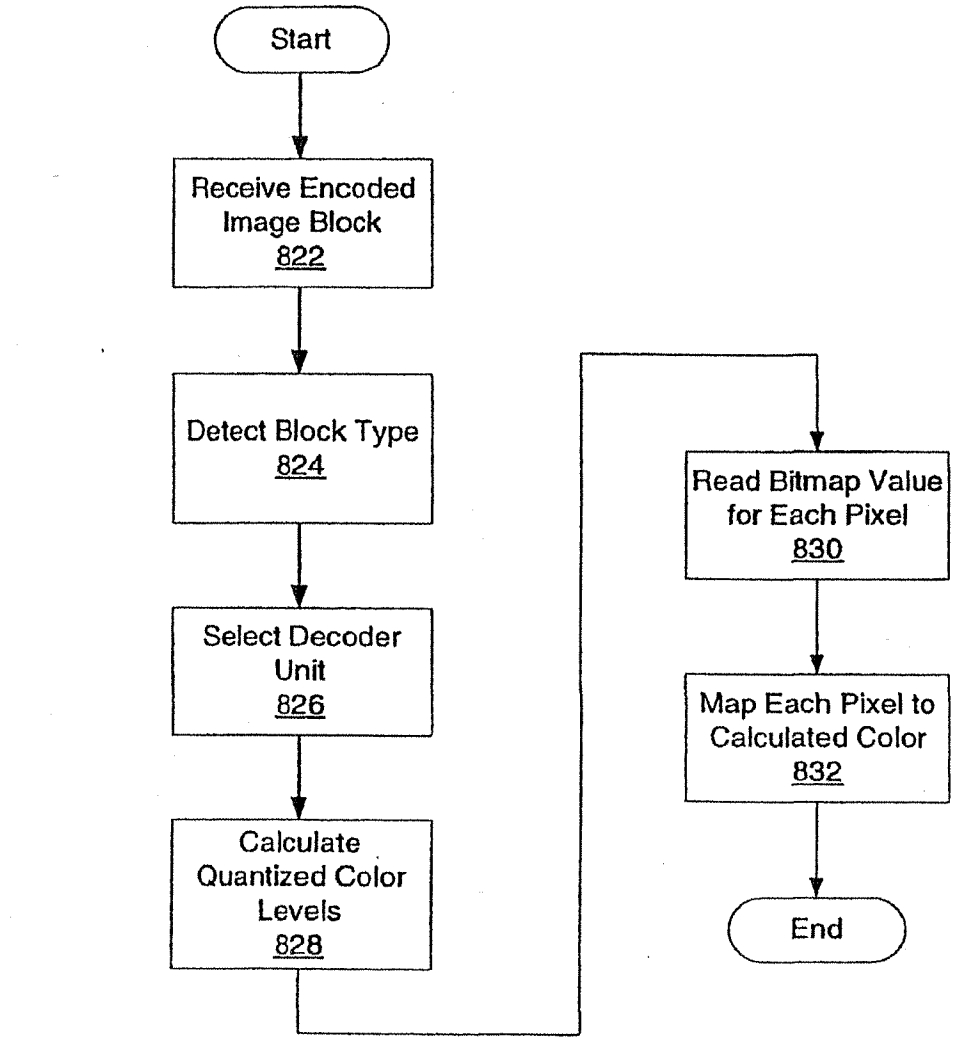


FIG. 8B

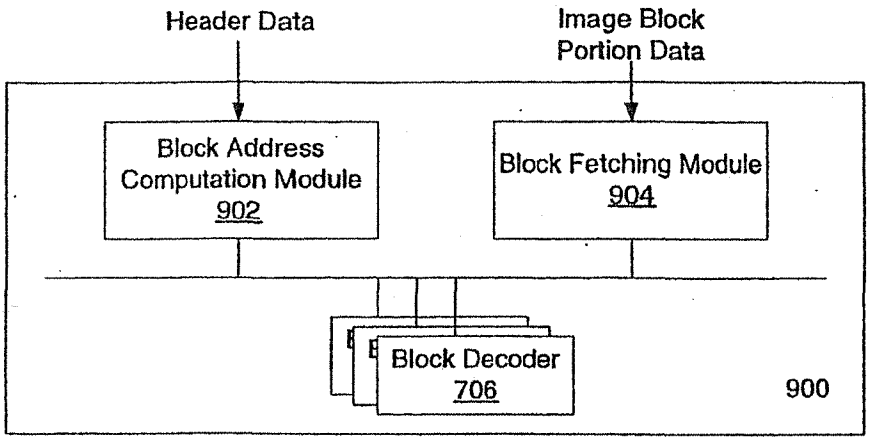


FIG. 9A

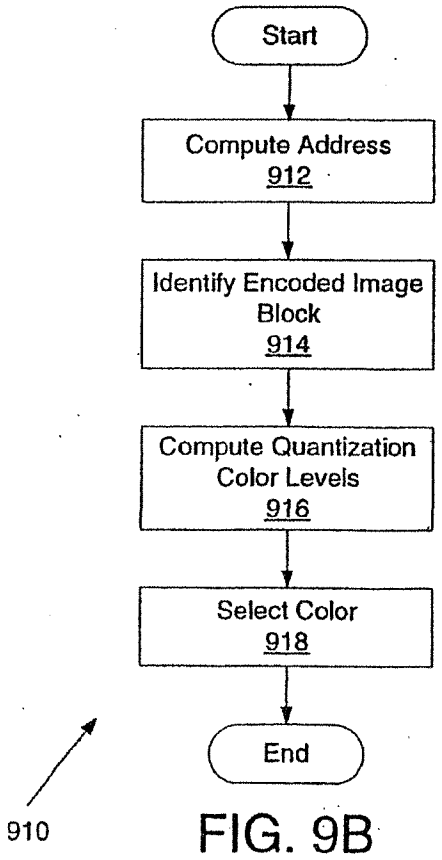


FIG. 9B

IMAGE PROCESSING SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of and claims the priority benefit of U.S. patent application Ser. No. 10/052,613 entitled "Fixed-Rate Block-Based Image Compression with Inferred Pixel Values" filed Jan. 17, 2002 and now U.S. Pat. No. 6,775,417, which is a continuation-in-part of U.S. patent application Ser. No. 09/351,930 entitled "Fixed-Rate Block-Based Image Compression with Inferred Pixel Values" filed Jul. 12, 1999 and now U.S. Pat. No. 6,658,146 which is a continuation of U.S. patent application Ser. No. 08/942,860 entitled "System and Method for Fixed-Rate Block-Based Image Compression with Inferred Pixel Values" filed Oct. 2, 1997 and now U.S. Pat. No. 5,956,431. The disclosure of the above-referenced applications and patents are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to image processing, and more particularly to three-dimensional rendering using fixed-rate image compression.

2. Description of Related Art

Conventionally, generating images, such as realistic and animated graphics on a computing device, required tremendous memory bandwidth and processing power on a graphics system. Requirements for memory and processing power are particularly true when dealing with three-dimensional images. In order to reduce bandwidth and processing power requirements, various compression methods and systems have been developed including Entropy or lossless encoders, Discrete Cosine Transform (DCT) or JPEG type compressors, block truncation coding, and color cell compression. However, these methods and systems have numerous disadvantages.

Entropy or lossless encoders include Lempel-Ziv encoders, which rely on predictability. For data compression using entropy encoders, a few bits are used to encode most commonly occurring symbols. In stationary systems where probabilities are fixed, entropy coding provides a lower bound for compression than can be achieved with a given alphabet of symbols. However, coding does not allow random access to any given symbol. Part of the compressed data preceding a symbol of interest must be first fetched and decompressed to decode the symbol, requiring considerable processing time and resources, as well as decreasing memory throughput. Another problem with existing entropy methods and systems is that no guaranteed compression factor is provided. Thus, this type of encoding scheme is impractical where memory size is fixed.

Discrete Cosine Transform (DCT) or JPEG-type compressors allow users to select a level of image quality. With DCT, uncorrelated coefficients are produced so that each coefficient can be treated independently without loss of compression efficiency. The DCT coefficients can be quantized using visually-weighted quantization values which selectively discard least important information.

DCT, however, suffers from a number of shortcomings. One problem with DCT and JPEG-type compressors is a requirement of large blocks of pixels, typically, 8×8 or 16×16 pixels, as a minimally accessible unit in order to obtain a reasonable compression factor and quality. Access to a very small area, or even a single pixel involves fetching

a large quantity of compressed data; thus requiring increased processor power and memory bandwidth. A second problem is that the compression factor is variable, therefore requiring a complicated memory management system that, in turn, requires greater processor resources. A third problem with DCT and JPEG-type compression is that using a large compression factor significantly degrades image quality. For example, an image may be considerably distorted with a form of ringing around edges in the image as well as noticeable color shifts in areas of the image. Neither artifact can be removed with subsequent low-pass filtering.

A further disadvantage with DCT and JPEG-type compression is the complexity and significant hardware cost for a compressor and decompressor (CODEC). Furthermore, high latency of a decompressor results in a large additional hardware cost for buffering throughout the system to compensate for the latency. Finally, DCT and JPEG-type compressors may not be able to compress a color-keyed image.

Block truncation coding (BTC) and color cell compression (CCC) use a local one-bit quantizer on 4×4 pixel blocks. Compressed data for such a block consists of only two colors and 16-bits that indicate which of the two colors is assigned to each of 16 pixels. Decoding a BTC/CCC image consists of using a multiplexer with a look-up table so that once a 16-texel (or texture element, which is the smallest addressable unit of a texture map) block (32-bits) is retrieved from memory, the individual pixels are decoded by looking up the two possible colors for that block and selecting the color according to an associated bit from 16 decision bits.

Because the BTC/CCC methods quantize each block to just two color levels, significant image degradation may occur. Further, a two-bit variation of CCC stores the two colors as 8-bit indices into a 256-entry color lookup table. Thus, such pixel blocks cannot be decoded without fetching additional information, which may consume additional memory bandwidth.

The BTC/CCC methods and systems can use a 3-bit per pixel scheme, which stores the two colors as 16-bit values (not indices into a table) resulting in pixel blocks of six bytes. Fetching such units, however, decreases system performance because of additional overhead due to memory misalignment. Another problem associated with BTC/CCC methods is a high degradation of image quality when used to compress images that use color keying to indicate transparent pixels.

Therefore, there is a need for a system and method that maximizes accuracy of compressed images while minimizing storage, memory bandwidth requirements, and decoding hardware complexities. There is a further need for compressing image data blocks into convenient sizes to maintain alignment for random access to any one or more pixels.

SUMMARY OF THE INVENTION

The present invention provides for fixed-rate block based image compression with inferred pixel values. An image processing system includes an image encoder engine and an image decoder engine. The image encoder engine includes an image decomposer, at least one block encoder, and an encoded image composer. The block decomposer decomposes an original image into a header and a plurality of blocks, which are composed of a plurality of image elements or pixels. The block encoder subsequently processes each block. The block encoder includes a selection module, a codeword generation module, and a construction module.

Specifically, the selection module computes a set of parameters from image data values of each set of image elements. The codeword generation module then generates codewords, which are reference image data values such as colors or density values. Subsequently, the construction module uses the codewords to derive a set of quantized image data values. The construction module then maps each of the image element's original image data values with an index to one of the derived image data values. Finally, the codewords and indices are output as encoded image blocks.

Conversely, the image decoder engine includes an encoded image decomposer, at least one block decoder, and an image composer. The image decomposer takes the encoded image and decomposes the encoded image into a header and plurality of encoded image blocks. The block decoder uses the codewords in the encoded image blocks to generate a set of derived image data values. Subsequently, the block decoder maps the index values for each image element to one of the derived image data values. The image composer then reorders the decompressed image blocks in an output data file, which is forwarded to a display device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a data processing system, according to an embodiment of the present invention;

FIG. **2** is a block diagram of an image processing system;

FIG. **3A** is a block diagram of one embodiment of an image encoder system;

FIG. **3B** is a block diagram of an alternative embodiment of an image encoder system;

FIG. **3C** is a graphical representation of an image block;

FIG. **3D** is a graphical representation of a three-dimensional image block;

FIG. **4** is a block diagram of an image block encoder of FIG. **2A**, **3A**, or **3B**;

FIG. **5A** is a data sequence diagram of an original image;

FIG. **5B** is a data sequence diagram of encoded image data of an original image output from the image encoder system;

FIG. **5C** is a data sequence diagram of an encoded image block from the image block encoder of FIG. **4**;

FIG. **6A–6E** are flowcharts illustrating encoding processes, according to the present invention;

FIG. **7A** is a block diagram of an image decoder system;

FIG. **7B** is a block diagram of one embodiment of a block decoder of FIG. **7A**;

FIG. **7C** is a block diagram of an alternative embodiment of a block decoder of FIG. **7A**;

FIG. **7D** is a logic diagram illustrating an exemplary decoder unit, according to the present invention;

FIG. **8A** is a flowchart illustrating a decoding process of the image decoder of FIG. **2**;

FIG. **8B** is a flowchart illustrating operations of the block encoder of FIG. **7A**;

FIG. **9A** is a block diagram of a subsystem for random access to a pixel or an image block; and

FIG. **9B** is a flowchart illustrating random access to a pixel or an image block.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **1** is a block diagram of an exemplary data processing system **100** for implementing the present invention. The data processing system **100** comprises a CPU **102**, a memory **104**, a storage device **106**, input devices **108**, output devices **110**, and a graphics engine **112** all of which are coupled to a system bus **114**. The memory **104** and storage device **106** store data within the data processing system **100**. The input device **108** inputs data into the data processing system **100**, while the output device **110** receives data from the data processing system **100**. Although the data bus **114** is shown as a single line, alternatively, the data bus **114** may be a combination of a processor bus, a PCI bus, a graphic bus, or an ISA bus.

FIG. **2** is a block diagram of an exemplary image processing system **200**. In one embodiment, the image processing system **200** is contained within the graphics engine **112** (FIG. **1**). The image processing system **200** includes an image encoder engine **202** and an image decoder engine **204**. The image processing system **200** may also include, or be coupled to, an image source unit **206**, which provides images to the image encoder engine **202**. Further, the image processing system **200** may include or be coupled to an output unit **208** to which processed images are forwarded for storage or further processing. Additionally, the image processing system **200** may be coupled to the memory **104** (FIG. **1**) and the storage device **106** (FIG. **1**). In an alternative embodiment, the image encoder engine **202** and the image decoder engine **204** are contained within different computing devices, and the encoded images pass between the two engines **202** and **204**.

Within the image encoder engine **202**, images are broken down into individual blocks and processed before being forwarded, for example, to the storage device **106** as compressed or encoded image data. When the encoded image data are ready for further processing, the encoded image data are forwarded to the image decoder engine **204**. The image decoder engine **204** receives the encoded image data and decodes the data to generate an output that is a representation of the original image that was received from the image source unit **206**.

FIGS. **3A** and **3B** are block diagrams illustrating two exemplary embodiments of the image encoder engine **202** of FIG. **2**. The image encoder engine **202** comprises an image decomposer **302**, a header converter **304**, one or more block encoders **306** in FIG. **3A** (**306***a*–**306***n*, where n is the nth encoder in FIG. **3B**), and an encoded image composer **308**. The image decomposer **302** is coupled to receive an original image **310** from a source, such as the image source unit **206** (FIG. **2**), and forwards information from a header of the original image **310** to the header converter **304**. Subsequently, the header converter **304** modifies the original header to generate a modified header, as will be described further in connection with FIG. **5B**. The image decomposer **302** also breaks, or decomposes, the original image **310** into R numbers of image blocks, where R is any integer value. The number of image blocks the original image **310** is broken into may depend on the number of image pixels. In an exemplary embodiment, the image **310** having A image pixels by B image pixels will, typically, be (A/4)×(B/4) blocks. For example, an image that is 256 pixels by 256 pixels will be broken down into 64×64 blocks. In the present embodiment, the image is decomposed such that each image block is 4 pixels by 4 pixels (16 pixels). Those skilled in the art will recognize that the number of pixels or the image block size may be varied.

Briefly turning to FIG. **3C**, an example of a single image block **320** is illustrated. The image block **320** is composed of image elements (pixels) **322**. The image block **320** may be defined as an image region, W pixels in width by H pixels in height. In the embodiment of FIG. **3C**, the image block **320** is W=4 pixels by H=4 pixels (4×4).

In an alternative embodiment, the original image **310** (FIG. 3A or 3B) may be a three-dimensional volume data set as shown in FIG. 3D. FIG. 3D illustrates an exemplary three-dimensional image block **330** made up of sixteen image elements (volume pixels or voxels) **332**. Image block **330** is defined as an image region W voxels in width, H voxels in height, and D voxels in depth.

The three-dimensional volume data set may be divided into image blocks of any size or shape. For example, the image may be divided along a z-axis into a plurality of xxyxz sized images, where z=1. Each of these xxyx1 images may be treated similarly with two-dimensional images, where each xxyx1 image is divided into two-dimensional image blocks, as described above with respect to FIG. 3C. However, decomposing the three-dimensional image into two-dimensional "slices" for compression does not fully utilize the graphical similarities that may exist in the z (depth) direction in a three-dimensional image. To utilize such similarities, the volume data may be decomposed into a plurality of three-dimensional image blocks. It will be understood that in alternative embodiments, other combinations of WxHxD are possible, and may be more desirable, depending on the data being compressed.

This type of three-dimensional image data is used, for example, in medical imaging applications such as ultrasound or magnetic resonance imaging ("MRI"). In such an application, a body part is scanned to produce a three-dimensional matrix of image elements (i.e., image block comprised of voxels **320**). The image is x voxels wide by y voxels high by z voxels deep. In this example, each voxel provides density data regarding characteristics of body tissue. In ultrasound applications, each voxel may be provided with a brightness level indicating the strength of echoes received during scanning.

In the embodiment of FIG. 3D, the original image **310** is a three-dimensional data volume where the image data are density values. In alternative embodiments, other scalar data types may be represented in the original image **310**, such as transparency or elevation data. In further embodiments, vector data, such as the data used for "bump maps", may be represented.

Referring back to FIGS. 3A and 3B, each block encoder **306** receives an image block **320** from the image decomposer **302**, and encodes or compresses each image block **320**. Subsequently, each encoded image block is forwarded to the encoded image composer **308**, which orders the encoded image blocks in a data file. Next, the data file from the encoded image composer **308** is concatenated with the modified header from the header converter **304** to generate an encoded image data file that is forwarded to an output **312**. Thus, the modified header and the encoded image blocks together form the encoded image data that represent the original image **310**. Alternatively, having more than one block encoder **306***a*–**306***n*, as shown in FIG. 3B, allows for encoding multiple image blocks simultaneously, one image block per block encoder **306***a*–**306***n*, within the image encoder engine **202**. Advantageously, simultaneous encoding increases image processing efficiency and performance.

The image data associated with the original image **310** may be in any one of a variety of formats including red-green-blue ("RGB"), YUV 420 (YUV are color models representing luminosity and color difference signals), YUV 422, or a propriety color space. In some cases, conversion to a different color space before encoding the original image **310** may be useful. In one embodiment, each image block **320** is a 4×4 set of pixels where each pixel **322** is 24-bits in size. For each pixel **322**, there are 8-bits for a Red ("R")-channel, 8-bits for a Green ("G")-channel, and 8-bits for a Blue ("B")-channel in an RGB implementation color space. Alternatively, each encoded image block is also a 4×4 set of pixels with each pixel being only 2-bits in size and having an aggregate size of 4-bits as will be described further below.

FIG. **4** is a block diagram illustrating an exemplary block encoder **306** of FIGS. 3A and 3B. The block encoder **306** includes a quantizer **402** and a bitmap construction module **404**. Further, the quantizer **402** includes a block type module **406**, a curve selection module **408**, and a codeword generation module **410**.

Each image block **320** (FIG. 3C) of the decomposed original image **310** (FIGS. 3A and 3B) is received and initially processed by the quantizer **402** before being forwarded to the bitmap construction module **404**. The bitmap construction module **404** outputs encoded image blocks for the encoded image composer **308** (FIGS. 3A and 3B) to order. The bitmap construction module **404** and the modules of the quantizer **402** are described in more detail below.

Briefly, FIG. 5A is a diagram of a data sequencer or string **500** representing the original image **310** (FIGS. 3A and 3B) that is received by the block decomposer **302** (FIGS. 3A and 3B). The data string **500** includes an α-bit header **502** and a β-bit image data **504**. The header **502** may include information such as pixel width, pixel height, format of the original image **310** (e.g., number of bits to the pixel in RGB or YUV format), as well as other information. The image data **504** are data representing the original image **310**, itself.

FIG. 5B is a diagram of a data sequence or string **510** representing encoded image data that are generated by the image encoder engine **202** (FIG. **2**). The encoded image data string **510** includes a modified header portion **512** and an encoded image block portion **514**. The modified header portion **512** is generated by the header converter **304** (FIGS. 3A and 3B) from the original α-bit header **502** (FIG. 5A) and includes information about file type, number of bits per pixel of the original image **310** (FIGS. 3A and 3B), addressing in the original image **310**, other miscellaneous encoding parameters, as well as the width and height information indicating size of the original image **310**. The encoded image block portion **514** includes encoded image blocks **516***a*–*q* from the block encoders **306** (FIGS. 3A and 3B) where q is the number of blocks resulting from the decomposed original image **310**.

FIG. 5C is a diagram of a data sequence or string **518** representing an encoded image block. The data string **518** may be similar to any one of the encoded image blocks **516***a*–*q* (FIG. 5B) shown in the encoded image data string **510** of FIG. 5B.

The encoded image block data string **518** includes a codeword section **520** and a bitmap section **522**. The codeword section **520** includes j codewords, where j is an integer value, that are used to compute colors of other image data indexed by the bitmap section **522**. A codeword is an n-bit data string that identifies a pixel property, such as color component, density, transparency, or other image data values. In one embodiment, there are two 16-bit codewords CW_0 and CW_1 (j=2). The bitmap section **522** is a Q-bit data portion and is described in more detail in connection with FIG. 6B.

In an alternative embodiment, each encoded image block is 64-bits, which includes two 16-bit codewords and a 32-bit (4×4×2 bit) bitmap **522**. Encoding the image block **320** (FIG. 3C) as described above provides greater system flexibility and increased data processing efficiency. In a further exemplary embodiment, each 32-bit bitmap section **522** may be a three-dimensional 32-bit bitmap.

FIGS. 6A–6E describe operations of the image encoder engine **202** (FIG. **2**). In flowchart **600**, a general operation of the image encoder engine **202** is shown. In block **602**, a data string **500** (FIG. 5A) of the original image **310** (FIGS. 3A and 3B), which includes the α-bit header **502** (FIG. 5A) and the β-bit image data **504** (FIG. 5A), is input into the image decomposer **302** (FIGS. 3A and 3B). The image decomposer **302** decomposes the image **310** into the α-bit header and a plurality of blocks in block **604**. The α-bit header **502** is then forwarded to the header converter **304** (FIGS. 3A and 3B). Subsequently, the header converter **304** generates a modified header **512** (FIG. 5B) from the α-bit header **502** in block **606**. The modified header **512** is then forwarded to the encoded image composer **308** (FIGS. 3A and 3B).

Simultaneous with the header conversion process, each image block **320** is encoded in block **608** by one or more of the block encoders **306***a*–**306***n* (FIGS. 3A and 3B) to generate the encoded image blocks **516** (FIG. 5B). Each image block **320** may be processed sequentially in one block encoder **306**, or multiple image blocks **320** may be processed in parallel in multiple block encoders **306***a*–**306***n*.

The encoded image blocks **516** are output from the block encoders **306**, and are placed into a predefined order by the encoded image composer **308**. In one embodiment, the encoded image blocks **516** are arranged in a file from left to right and top to bottom and in the same order in which the encoded image blocks **516** were broken down by the image decomposer **302** (FIGS. 3A and 3B). The image encoder engine **202** subsequently composes the modified header information **512** from the header converter **304** and the encoded image blocks **516***a*–**516***q* in block **610**. Specifically, the modified header **512** and the ordered encoded image blocks **516** are concatenated to generate the encoded image data file **510** (FIG. 5B), which may be written as encoded output **312** (FIGS. 3A and 3B) to the memory **104**, storage device **106**, or any output device **110** (FIG. **1**) in block **612**.

FIG. 6B is a flowchart **620** showing the encoding process of block **608** (FIG. 6A) in more detail. In block **622**, codewords **520** (FIG. 5C) are computed by the codeword generation module **410** (FIG. **4**). The process for computing these codewords **520** is described in more detail in connection with FIG. 6C.

Once the codewords **520** have been computed, pixel values or properties, such as colors, for the image block **320** (FIG. 3C) are computed or quantized in block **624**. Specifically, the codewords **520** provide points in a pixel space from which m quantized pixel values may be inferred. The m quantized pixel values are a limited subset of pixels in a pixel space that are used to represent the current image block. The process for quantizing pixel values, and more specifically colors, will be described infra in connection with FIGS. 8A and 8B. Further, the embodiments will now be described with respect to colors of a pixel value although one skilled in the art will recognize that, in general, any pixel value may be used with respect to the present invention. Therefore, the image data, which is quantized may be any form of scalar or vector data, such as density values, transparency values, and "bump map" vectors.

In an exemplary embodiment, each pixel is encoded with two bits of data which can index one or m quantized colors, where m=4 in this embodiment. Further, four quantized colors are derived from the two codewords **520** where two colors are the codewords **520**, themselves, and the other two colors are inferred from the codewords **520**, as will be described below. It is also possible to use the codewords **520** so that there is one index to indicate a transparent color and three indices to indicate colors, of which one color is inferred.

In another embodiment, the bitmap **522** (FIG. 5C) is a 32-bit data string. The bitmap **522** and codewords **520** are output in block **624** as a 64-bit data string representing an encoded image block **518**. Specifically, the encoded image block **514** (FIG. 5B) includes two 16-bit codewords **520** (n=16) and a 32-bit bitmap **522**. Every codeword **520** that is a 16-bit data string includes a 5-bit red-channel, 6-bit green-channel, and 5-bit blue-channel.

Each of the encoded image blocks **516** is placed together and concatenated with modified header information **512** derived from the original α-bit header **502** of the original image **310** (FIGS. 3A and 3B). A resulting output is the encoded image data **510** representing the original image **310**.

FIG. 6C is a flowchart **630** illustrating a process for computing codewords for the image blocks **320** (FIG. 3C), and relates to color quantizing using quantizer **402** (FIG. **4**). The process for computing codewords can be applied to all scalar and vector image data types. In select block type **632**, the quantizer **402** uses the block type module **406** (FIG. **4**) to select a first block type for the image block **320** that is being processed. For example, a selected block type may be a four-color or a three-color plus transparency block type, where the colors within the particular block type have equidistant spacing in a color space. Those of ordinary skill in the art will readily recognize that selecting a block type for each image is not intended to be limiting in any way. Instead, the present invention processes image blocks that are of a single block type, which eliminates the need to distinguish between different block types, such as the three- and four-color block types discussed above. Consequently, the block type module **406** and select block type **632** are optional.

Once the block type is selected, the quantizer **402** computes an optimal analog curve for the block type in block **634**. Computation of the optimal analog curve will be further described in connection with FIG. 6D. The analog curve is used to simplify quantizing of the colors in the image block. Subsequently in block **636**, the quantizer **402** selects a partition of points along the analog curve, which is used to simplify quantizing of the colors in the image block. A partition may be defined as a grouping of indices {1 . . . (W×H)} into m nonintersecting sets. In one embodiment, the indices (1 . . . 16) are divided into three or four groups or clusters (i.e., m=3 or 4) depending on the block type.

Once a partition is selected, optimal codewords for the particular partition are computed in block **638**. In addition to computing the codewords, an error value (square error as described infra) for the codeword is also computed in block **640**. Both computations will be described in more detail in connection with FIG. 6E. If the computed error value is the first error value, the error value is stored in block **642**. Alternatively, the computed error value is stored if it is less than the previously stored error value. For each stored error value, corresponding block type and codewords are also stored in block **644**. The process of flowchart **630** seeks to find the block type and codewords that minimize the error function.

Next in block **646**, the code generation module **410** (FIG. **4**) determines if all possible partitions are completed. If there are more partitions, the code generation module **410** selects the next partition, computes the codewords and associated error values, and stores the error values, associated block

types, and codewords if the error value is less than the previously stored error value.

After all the possible partitions are completed, the codeword generation module **410** determines, in block **648**, whether all block types have been selected. If there are more block types, the codeword generation module **410** selects the next block type and computes the codeword and various values as previously described. After the last block type has been processed, the codeword generation module **410** outputs a result of the block type and codewords **520** (FIG. 5C) having the minimum error in block **650**.

In an alternative embodiment, the optimal analog curve may be computed before selecting the block type. That is, the optimal analog curve is computed before the selection of the block type and partition, computation of the codewords and error values, and storage of the error value, block type, and codeword. Computing the optimal analog curve first is useful if all block types use the same analog curve and color space because the analog curve does not need to be recomputed for each block type.

FIG. **6D** is a flowchart **660** describing a process of identifying the optimal analog curve. The curve selection module **408** (FIG. 4) first computes a center of gravity for pixel colors of an image block **320** (FIG. 3C) in block **662**. The center of gravity computation includes averaging the pixel colors. Once the center of gravity is computed, a vector in color space is identified in block **664** to minimize the first moment of the pixel colors of the image block **320**. Specifically for identifying a vector, a straight line is fit to a set of data points, which are the original pixel colors of the image block **320**. The straight line is chosen passing through the center of gravity of the set of data points such that it minimizes a "moment of inertia" (i.e., square error). For example, to compute a direction of a line minimizing the moment of inertia for three pixel properties, tensor inertia, T, is calculated from individual colors as follows:

$$T=\sum_{i=1}^{W\times H}\begin{bmatrix} C_{1i}^2+C_{2i}^2 & -C_{0i}C_{1i} & -C_{0i}C_{2i} \\ -C_{0i}C_{1i} & C_{0i}^2C_{2i}^2 & -C_{1i}C_{2i} \\ -C_{0i}C_{2i} & -C_{2i}C_{1i} & C_{0i}^2+C_{1i}^2 \end{bmatrix}$$

where C_0, C_1, and C_2 represent pixel properties (e.g., color components in RGB or YUV) relative to a center of gravity. In one embodiment of an RGB color space, C_{0i} is a value of red, C_{1i} is a value of green, and C_{2i} is a value of blue for each pixel, i, of the image block. Further, i takes on integer values from 1 to W×H, so that if W=4 and H=4, i ranges from 1 to 16.

An eigenvector of tensor inertia, T, with the smallest eigenvalue is calculated in block **666** using conventional methods. An eigenvector direction along with the calculated gravity center, defines an axis that minimizes the moment of inertia. This axis is used as the optimal analog curve, which, in one embodiment, is a straight line. Those of ordinary skill in the art will readily recognize that the optimal analog curve is not limited to a straight line, but may include a set of parameters, such as pixel values or colors, that minimizes the moment of inertia or mean-square-error when fit to the center of gravity of the pixel colors in the image block. The set of parameters may define any geometric element, such as a curve, plate, trapezoid, or the like.

FIG. **6E** is a flowchart **670** describing the process undertaken by the codeword generation module **410** (FIG. 4) for selecting the partitions, computing the codewords and associated error for the partitions, and storing the error value, block type, and codeword if the error value is less than a previously stored error value. In block **672**, the codeword generation module **410** projects the W×H color values onto the previously constructed optimal analog curve. The value of W×H is the size in number of pixels of an image block **320** (FIG. 3C). In one embodiment where W and H are both four pixels, W×H is 16 pixels.

Subsequently in block **674**, the colors are ordered sequentially along the analog curve based on a position of the color on a one-dimensional analog curve. After the colors are ordered, the codeword generation module **410** searches, in block **676**, for optimal partitions. Thus, the codeword generation module **410** takes the W×H colors (one color associated with each pixel) that are ordered along the analog curve and partitions and groups the colors into a finite number of clusters with a predefined relative spacing. In one embodiment where W=4 and H=4 (i.e., W×H is 16), the 16 colors are placed in three and four clusters (i.e., m=3 or 4).

In conducting the search for the optimal partition, a color selection module within the codeword generation module **410** finds the best m clusters from the W×H points projected onto the optimal curve, so that the error associated with the selection is minimized. The best m clusters are determined by minimizing the mean-square-error with the constraint that the points associated with each cluster are spaced to conform to the predefined spacing.

In one embodiment for a block type of four equidistant colors, the error may be defined as a square error along the analog curve, such as

$$E^2=\sum_{cluster0}(x_i-p_0)^2+\sum_{cluster1}\left[x_i-\left(\frac{2}{3}p_0+\frac{1}{3}p_1\right)\right]^2+\sum_{cluster2}\left[x_i-\left(\frac{1}{3}p_0+\frac{2}{3}p_1\right)\right]^2+\sum_{cluster3}(x_i-p_1)^2$$

where E is the error for the particular grouping or clustering, p_0 and p_1 are the coded colors, and x_i are the projected points on the optimal analog curve.

In instances where the block type indicates three equidistant colors, the error may be defined as a squared error along the analog curve, such as

$$E^2=\sum_{cluster0}(x_i-p_0)^2+\sum_{cluster1}\left[x_i-\left(\frac{1}{2}p_0+\frac{1}{2}p_1\right)\right]^2+\sum_{cluster2}(x_i-p_1)^2$$

After the resulting optimal codewords **520** are identified, the codewords **520** are forwarded to the bitmap construction module **404** (FIG. 4). The bitmap construction module **404** uses the codewords **520** to identify the m colors that may be specified or inferred from those codewords **520** in block **678**. In one embodiment, the bitmap construction module **404** uses the codewords **520** (e.g., CW_0 and CW_1) to identify the three or four colors that may be specified or inferred from those codewords **520**.

Next in block **680**, the bitmap construction module **404** constructs a block bitmap **522** (FIG. 5C) using the codewords **520** associated with the image block **320** (FIG. 3C).

Colors in the image block **320** are mapped to the closest color associated with one of the quantized colors specified by, or inferred from, the codewords **520**. The result is a color index, referenced as ID, per pixel in the block identifying the associated quantized color.

Information indicating the block type is implied by the codewords **520** and the bitmap **522**. In one embodiment, the order of the codewords **520** indicates the block type. If a numerical value of CW_0 is greater than a numerical value of CW_1, the image block is a four-color block. Otherwise, the block is a three-color plus transparency block.

In one embodiment discussed above, there are two-color image block types. One color image block type has four equidistant colors, while the other color image block type has three equidistant colors with the fourth color index used to specify that a pixel is transparent. For both color image block types, the color index is two bits. In an embodiment with density values in place of color values, each density image block type has four equidistant density values.

The output of the bitmap construction module **404** is an encoded image block **514** (FIG. 5B) having the m codewords **520** plus the bitmap **522**. Each encoded image block **516** is received by the encoded image composer **308** (FIGS. 3A and 3B) that, in turn, orders the encoded image blocks **516** in a file. In one embodiment, the encoded image blocks **516** are arranged from left to right and from top to bottom and in the same order as the blocks were broken down by the image decomposer **302**. The ordered file having the encoded image blocks **516** is concatenated with the modified header information **512** that is derived from the α-bit header **502** of the original image **310** (FIGS. 3A and 3B) to generate the encoded image data **510** that is the output of the image encoder engine **202** (FIG. 2). The output may then be forwarded to the memory **104**, the storage device **106**, or the output device **110** (FIG. 1).

The exemplary embodiment of the image encoder engine **202** advantageously reduces the effective data size of an image from 24-bits per pixel to 4-bits per pixel. Further, the exemplary embodiment beneficially addresses transparency issues by allowing codewords to be used with a transparency identifier.

FIG. 7A is a block diagram of an exemplary image decoder engine **204** (FIG. 2). The image decoder engine **204** includes an encoded image decomposer **702**, a header converter **704**, one or more block decoders **706** (**706***a*–**706***p*, where p represents the last block decoder), and an image composer **708**. The encoded image decomposer **702** is coupled to receive the encoded image data **514** (FIG. 5B) output from the image encoder engine **202** (FIG. 2). The encoded image decomposer **702** receives the encoded image *data string* **510** and *decomposes*, or *breaks*, the encoded image data string **510** into the header **512** (FIG. 5B) and the encoded image blocks **514** (FIG. 5B). Next, the encoded image decomposer **702** reads the modified header **512**, and forwards the modified header **512** to the header converter **704**. The encoded image decomposer **702** also decomposes the encoded image data string **510** into the individual encoded image blocks **516** (FIG. 5B) that are forwarded to the one or more block decoders **706**.

The header converter **704** converts the modified header **512** into an output header. Simultaneously, the encoded image blocks **516** are decompressed or decoded by the one or more block decoders **706**. Each encoded image block **516** may be processed sequentially in one block decoder **706**, or multiple encoded image blocks **514** may be processed in parallel with one block decoder **706** for each encoded image block **516**. Thus, multiple block decoders **706** allow for parallel processing that increases the processing performance and efficiency of the image decoder engine **204** (FIG. 2).

The image composer **708** receives each decoded image blocks from the one or more block decoders **706** and orders the decoded image block in a file. Further, the image composer **708** receives the converted header from the header converter **704**. The converted header and the decoded image blocks are placed together to generate output data representing the original image **310**.

FIG. 7B is a block diagram of an exemplary embodiment of a block decoder **706**. Each block decoder **706** includes a block type detector **710**, one or more decoder units **712**, and an output selector **714**. The block type detector **710** is coupled to the encoded image decomposer **702** (FIG. 7A), the output selector **714**, and each of the one or more decoder units **712**.

The block type detector **710** receives the encoded image blocks **514** and determines the block type for each encoded image block **516** (FIG. 5B). The block type is detected based on the codewords **520** (FIG. 5C). After the block type is determined, the encoded image blocks **514** are passed to each of the decoder units **712**, which decompress or decode each encoded image block **516** to generate colors for each particular encoded image block **516**. The decoder units **712** may be c-channels wide (e.g., one channel for each color component or pixel property being encoded), where c is any integer value. Using the selector signal, the block type detector **710** enables the output selector **714** to output the color of each encoded image block **516** from one of the decoder units **712** that corresponds with the block type detected by the block type detector **710**. Specifically, the block type detector **710** passes a selector signal to the output selector **714** that is used to select an output corresponding to the block type detected. Alternatively, using the selector signal, the appropriate decoder unit **712** could be selected so that the encoded block is only processed through the selected decoder unit.

FIG. 7C is a block diagram of an alternative embodiment of a block decoder **706**. In this embodiment, the block decoder **706** includes a block type detector **720**, a first decoder unit **722**, a second decoder unit **724**, and an output selector **726**. The block type detector **720** is coupled to receive each encoded image block **516** (FIG. 5B), and determine by comparing the codewords **520** (FIG. 5C) of the encoded image block, the block type for each encoded image block **516**. For example, the block type may be four quantized colors or three quanitized colors and a transparency. Once the block type is selected and a selector signal is forwarded to the output selector **726**, the encoded image blocks **516** are decoded by the first and second decoder units **722** and **724**, respectively, to produce the pixel colors of each image block. The output selector **726** is enabled by the block type detector **720** to output the colors from the first and second decoder units **722** and **724** that correspond to the block type selected.

FIG. 7D is a logic diagram illustrating an exemplary embodiment of a decoder unit similar to the decoder units **722** and **724** of FIG. 7C. For simplicity, the functionality of each of the first and second decoder units **722** and **724** is merged into the single logic diagram of FIG. 7D. Those skilled in the art will recognize that although the diagram is described with respect to a red-channel of the decoder units, the remaining channels (i.e., the green-channel and the blue-channel) are similarly coupled and functionally equivalent.

The logic diagram illustrating the first and second decoder units **722** and **724** is shown including portions of the block type detector **710**, **720** (FIGS. 7B and 7C, respectively) such as a comparator unit **730**. The comparator unit **730** is coupled to and works with a first 2×1 multiplexer **732***a* and a second 2×1 multiplexer **732***b*. Both 2×1 multiplexers **732***a* and **732***b* are coupled to a 4×1 multiplexer **734** that serves to select an appropriate color to output. The 4×1 multiplexer **734** is coupled to receive a transparency indicator signal that indicates whether or not a transparency (e.g., no color) is being sent. The 4×1 multiplexer **734** selects a color for output based on the value of the color index, referenced as the ID signal, that references the associated quantized color for an individual pixel of the encoded image block **514** (FIG. 5B).

A red-channel **736** of the first decoder unit **722** includes a first and a second red-channel line **738***a* and **738***b* and a first and a second red-color block **740***a* and **740***b*. Along the path of each red-color block **740***a* and **740***b* is a first full adder **742***a* and **742***b*, a second full adder **744***a* and **744***b*, and carry-look ahead (CLA) adders **746***a* and **746***b*. The second decoder unit **724** contains similar components as the first decoder unit **722**.

The CLA adder **746***a* of the first red-color block **740***a* path of the first decoder unit **722** is coupled to the first 2×1 multiplexer **732***a*, while the CLA adder **746***b* of the second red-color block **740***b* path of the first decoder unit **722** is coupled to the second 2×1 multiplexer **732***b*. Further, adder **748** of the second decoder unit **724** is coupled to both the first and the second 2×1 multiplexers **732***a* and **732***b*.

FIG. **8**A is a flowchart **800** illustrating an operation of the decoder engine **204** (FIG. 2) in accordance with an exemplary embodiment of the present invention. For purposes of illustration, the process for the decoder engine **204** will be described with a single block decoder **706** (FIG. 7A) having two decoder units **722** and **724** as described earlier in connection with FIG. 7C. Those skilled in the art will recognize that the process is functionally equivalent for decoder systems having more than one block decoder **706** and more than two decoder units **712**, as discussed in connection with FIG. 7B.

In block **802**, the encoded image decomposer **702** (FIG. 7A) receives the encoded or compressed image data **510** (FIG. 5B) from the image encoder engine **202** (FIG. 2), through the memory **104** (FIG. 1) or the storage device **106** (FIG. 1). Next, the encoded image decomposer **702** decomposes the encoded image data **510** by forwarding the modified header **512** (FIG. 5B) to the header converter **704** (FIG. 7A) in block **804**.

Subsequently in block **806**, the header converter **704** converts the header information to generate an output header that is forwarded to the image composer **708** (FIG. 7A). Simultaneously, the one or more block decoders **706** (FIG. 7A) decode pixel colors for each encoded image block **516** (FIG. 5B) in block **808**. Each encoded image block **516** may be decoded sequentially in one block decoder **706** or multiple encoded image blocks **514** (FIG. 5B) may be decoded in parallel in multiple block decoders **706** in block **808**. The process for decoding each encoded image block **516** is further described in connection with FIG. 8B. Each decoded image block is then composed into a data file with the converted header information by the image composer **708** in block **810**. The image composer **708** then generates the data file as an output that represents the original image **310** (FIGS. 3A and 3B).

FIG. **8**B is a flowchart **820** illustrating an operation of the block decoder **706** (FIG. 7A) in accordance with an exemplary embodiment of the present invention. Initially, each encoded image block **516** (FIG. 5B) is received by the block decoder **706** in block **822**. Specifically, for one embodiment, the first and the second codewords **520** (e.g., CW_0 and CW_1 of FIG. 5C) are received by the block type detector **710**, **720** (FIGS. 7B and 7C, respectively) of the block decoder **706**. As discussed above, comparing the numerical values of CW_0 and CW_1 reveals the block type. The first five bits of each codeword **520** that represent the red-channel color are received by the red-channel of each of the first and second decoder units **722** and **724** (FIG. 7C). Furthermore, the second 6-bits of each codeword **520** that represent the green-channel color are received by the green-channel of each of the first and the second decoder units **722** and **724**, while the last 5-bits of each codeword **520** that represent the blue-channel color are received by the blue-channel of each of the first and second decoder units **722** and **724**.

Next in block **824**, the block type detector **710** detects the block type for an encoded image block **514**. Specifically, the comparator **730** (FIG. 7D) compares the first and the second codewords **520** (e.g., CW_0 and CW_1) and generates a flag signal to enable the first 2×1 multiplexer **732***a* or the second 2×1 multiplexer **732***b*. In block **826**, either the first decoder unit **722** or the second decoder unit **724** is selected.

Subsequently quantized color levels for the decoder units **722** and **724** are calculated in block **828**. The calculation of the quantized color levels will now be discussed in more detail. Initially, the first decoder unit **722** calculates the four colors associated with the two codewords **520** (e.g., CW_0 and CW_1) using the following exemplary relationship:

$$CW_0 = \text{first codeword} = \text{first color},$$

$$CW_1 = \text{second codeword} = \text{second color},$$

$$CW_2 = \text{third color} = \frac{2}{3}CW_0 + \frac{1}{3}CW_1; \text{ and}$$

$$CW_3 = \text{fourth color} = \frac{1}{3}CW_0 + \frac{2}{3}CW_1.$$

In one embodiment, the first decoder unit **722** may estimate the above equations for CW_2 and CW_3 as follows:

$$CW_2 = \frac{5}{8}CW_0 + \frac{3}{8}CW_1; \text{ and}$$

$$CW_3 = \frac{3}{8}CW_0 + \frac{5}{8}CW_1.$$

The red-color blocks **740***a* and **740***b* (FIG. 7D) serve as one-bit shift registers to obtain

$$\frac{1}{2}CW_0 \text{ or } \frac{1}{2}CW_1.$$

Further, each full adder **742***a*, **742***b*, **744***a*, and **744***b* (FIG. 7D) also serves to shift the signal left by 1-bit. Thus, the signal from the first full adders **742***a* and **742***b* is

$$\frac{1}{4}CW_0 \text{ or } \frac{1}{4}CW_1.$$

respectively, because of a 2-bit overall shift, while the signal from the second full adders 744*a* and 744*b* is

$$\frac{1}{8}CW_0 \text{ or } \frac{1}{8}CW_1,$$

respectively due to a 3-bit overall shift. These values allow for the above approximations for the color signals.

The second decoder unit 724 (FIG. 7C) calculates three colors associated with the codewords 520 (e.g., CW_0 and CW_1), and includes a fourth signal that indicates a transparency is being passed. The second decoder unit 724 calculates colors using the following exemplary relationship:

CW_0 = first codeword = first color;

CW_1 = second codeword = second color;

CW_3 = third color = $\frac{1}{2}CW_0 + \frac{1}{2}CW_1$; and

T = Transparency.

In one embodiment, the second decoder unit 724 has no approximation because the signals received from the red-color blocks 740*a* and 740*b* are shifted left by 1-bit so that the color is already calculated to

$$\frac{1}{2}CW_0 \text{ and } \frac{1}{2}CW_1,$$

respectively.

After the quantized color levels for the decoder units 722 and 724 selected in block 826 have been calculated in block 828, each bitmap value for each pixel is read from the encoded image data block 510 (FIG. 5A) in block 830. As each index is read, it is mapped in block 832 to one of the four calculated colors if the first decoder unit 722 is selected. Alternatively, one of the three colors and transparency is mapped in block 832 if the second decoder unit 724 is selected. The mapped colors are selected by the 4×1 multiplexer 734 based on the value of the ID signal from the bitmap 522 (FIG. 5C) of the encoded image block 514. As stated previously, a similar process occurs for selection of colors in the green-channel and the blue-channel.

As the color data are output from the red-channel, green-channel and blue-channel, the output are received by the image composer 708 (FIG. 7A). Subsequently, the image composer 708 arranges the output from the block encoders 706 in the same order as the original image 310 was decomposed. The resulting image is the original image 310, which is then forwarded to an output unit 208 (FIG. 2; e.g., a computer screen), which displays the image.

This exemplary embodiment beneficially allows for random access to any desired image block 320 (FIG. 3C) within an image, and any pixel 322 (FIG. 3C) within an image block 320. FIG. 9A is a block diagram of a subsystem 900 that provides random access to a pixel 322 or an image block 320 in accordance with one embodiment of the present invention.

The random access subsystem 900 includes a block address computation module 902, a block fetching module 904, and one or more block decoders 706 coupled to the block address computation module 902 and the block fetching module 904. The block address computation module 902 receives the header information 512 (FIG. 5B) of the encoded image data string 510 (FIG. 5B), while the block-fetching module 904 receives the encoded image block portion 514 (FIG. 5B) of the encoded image data string 510.

FIG. 9B is a flowchart 910 of a process for random access to a pixel 322 (FIG. 3C) or an image block 320 (FIG. 3C) using the random access subsystem 900 of FIG. 9A. When particular pixels 322 have been identified for decoding, the image decoder engine 204 (FIG. 2) receives the encoded image data string 510 (FIG. 5B). The modified header 512 (FIG. 5B) of the encoded image data string 510 is forwarded to the block address computation module 902 (FIG. 9A), and the encoded image block portion 514 (FIG. 5B) of the encoded image data string 510 is forwarded to the block-fetching module 904 (FIG. 9A).

In block 912, the block address computation module 902 reads the modified header 512 to compute an address of the encoded image block portion 514 having the desired pixels 322. The address computed is dependent upon the pixel coordinates within an image. Using the computed address, the block-fetching module 904 identifies each encoded image block 516 (FIG. 5B) of the encoded image block portion 514 that contains the desired pixels 322 in block 914. Once each encoded image block 516 having the desired pixels 322 has been identified, only the identified encoded image block 516 is forwarded to the block decoders 706 (FIG. 9A) for processing.

FIG. 9B is similar to the process described above in FIG. 8B, wherein the block decoders 706 compute quantized color levels for each identified encoded image blocks 516 having the desired pixels in block 916. After the quantized color levels have been computed, the color of the desired pixel is selected in block 918 and output from the image decoder engine 204.

Random access to pixels 322 of an image block 320 (FIG. 3C) advantageously allows for selective decoding of only needed portions or sections of an image. Random access also allows the image to be decoded in any order the data is required. For example, in three-dimensional texture mapping only portions of the texture may be required and these portions will generally be required in some non-sequential order. Thus, this embodiment of the present invention increases processing efficiency and performance when processing only a portion or section of an image. Further, the present invention beneficially encodes or compresses the size of an original image 310 (FIGS. 3A and 3B) from 24-bits per pixel to an aggregate 4-bits per pixel, and then decodes or decompresses the encoded image data string 510 (FIG. 5B) to get a representation of the original image 310. Additionally, the exemplary embodiment uses two base points or codewords from which additional colors are derived so that extra bits are not necessary to identify a pixel 322 color.

Moreover, the exemplary embodiment advantageously accomplishes the data compression on an individual block basis with the same number of bits per block so that the compression rate can remain fixed. Further, because the blocks are of fixed size with a fixed number of pixels 322, random access to any particular pixel 322 in the block is allowed. Additionally, an efficient use of system resources is provided because entire blocks of data are not retrieved and decoded to display data corresponding to only a few pixels 322.

Finally, the use of fixed-rate 64-bit data blocks provides the advantage of having simplified header information that allows for faster processing of individual data blocks. A 64-bit data block allows for faster processing as the need to wait until a full data string is assembled is eliminated. Further, an imaging system in accordance with the present invention may also reduce the microchip space necessary for a decoder system because the decoder system only needs to decode each pixel **322** to a set of colors determined by, for example, the two codewords **520** (FIG. 5C).

The present invention has been described above with reference to specific embodiments. It will be apparent to those skilled in the art that various modifications may be made and other embodiments can be used without departing from the broader scope of the invention. These and other variations of the specific embodiments are intended to be covered by the present invention.

What is claimed is:

1. An image decoder engine for decoding an encoded image data file, comprising:

an encoded image decomposer for decomposing the encoded image data file into a modified header and at least one compressed image block, each image block having at least one associated codeword and a plurality of image elements associated with an index value; and

at least one block decoder coupled to the encoded image decomposer for decompressing the at least one compressed image block into at least one decompressed image block by generating a set of quantized image data values and mapping the index value to a quantized image data value from the set of quantized image data values, the at least one block decoder further comprising,

at least one decoder configured for decompressing each of the at least one compressed image block to generate colors for each of the at least one compressed image block.

2. The image decoder engine of claim **1** further comprising an image composer configured for ordering the at least one decompressed image blocks in an output data file.

3. The image decoder engine of claim **1** wherein the set of quantized image data values comprise the at least one associated codeword and at least one image data value derived from the at least one associated codeword.

4. The image decoder engine of claim **1** further comprising a header converter coupled to the encoded image decomposer and configured for converting the modified header into an output header.

5. The image decoder engine of claim **4** wherein the image composer orders the at least one decompressed image block and the output header into a data file.

6. The image decoder engine of claim **1** wherein the at least one block decoder further comprises a block type detector configured for determining a block type for each of the at least one compressed image block based on the at least one associated codeword.

7. The image decoder engine of claim **1** wherein the decoder is configured to decompress each of the at least one compressed image block based on a block type.

8. The image decoder engine of claim **1** wherein the at least one block decoder further comprises an output selector for outputting the at least one decompressed image block.

* * * * *

Exhibit 12

SECURITIES AND EXCHANGE COMMISSION

WASHINGTON, D.C. 20549

FORM 8-K/A

(AMENDMENT NO. 1)

CURRENT REPORT

PURSUANT TO SECTION 13 OR 15(D) OF THE SECURITIES EXCHANGE ACT OF 1934

DATE OF REPORT: JANUARY 3, 2001
(Date of earliest event reported)

SONICBLUE INCORPORATED

(Exact name of registrant as specified in its charter)

DELAWARE	0-21126	77-0204341
(State or other jurisdiction of incorporation)	(Commission File Number)	(IRS Employer Identification No.)

2841 MISSION COLLEGE BOULEVARD, SANTA CLARA, CALIFORNIA 95054
(Address of principal executive offices) (Zip Code)

Registrant's telephone number, including area code: (408) 588-8000

Item 7. Financial Statements and Exhibits.

Item 7 of the Registrant's Current Report on Form 8-K, filed with the
Securities and Exchange Commission on January 18, 20001, is hereby amended and restated in its entirety as follows:

(a) Financial Statements of Business Acquired.

Not applicable.

(b) Unaudited Pro Forma Financial Information.

The unaudited pro forma condensed consolidated financial statements include: (1) unaudited pro forma condensed consolidated statement of operations for the year ended December 31, 1999; (2) unaudited pro forma condensed consolidated statement of operations for the nine-month period ended September 30, 2000; (3) unaudited pro forma condensed consolidated balance sheet as of September 30, 2000; and (4) the accompanying notes to unaudited pro forma condensed consolidated financial statements.

The unaudited pro forma condensed consolidated balance sheet as of September 30, 2000 reflects the financial position of SONICblue Incorporated ("SONICblue") after giving effect to the disposition of assets and liabilities and receipt of proceeds as if the disposition of the graphics chip business occurred on September 30, 2000.

The unaudited pro forma condensed consolidated statement of operations for the nine-month period ended September 30, 2000 assumes the disposition of the graphics chip business occurred on January 1, 2000. The unaudited pro forma condensed consolidated statement of operations for the year ended December 31, 1999 is presented as if the disposition of the graphics chip business and the acquisition of Diamond Multimedia Systems, Inc. (which was acquired on September 24, 1999) occurred on January 1, 1999. The pro forma adjustments are preliminary and based on management's estimates. Based on the timing of the closing of the transaction, the finalization of the separation plans and other factors, final adjustments may differ materially from those presented in these pro forma financial statements.

The unaudited pro forma condensed consolidated financial statements are not necessarily indicative of what the actual financial results would have been had the transactions described above taken place on January 1, 2000, January 1, 1999 or September 30, 2000. In addition, they do not purport to indicate the future results of operations or financial position of VIA Technologies, Inc. or SONICblue.

These unaudited pro forma condensed consolidated financial statements should be read in conjunction with the historical annual and interim financial statements of SONICblue that have been filed with the Securities and Exchange Commission.

SONICBLUE INCORPORATED
UNAUDITED PRO FORMA CONDENSED CONSOLIDATED BALANCE SHEET
SEPTEMBER 30, 2000
(IN THOUSANDS)

	HISTORICAL	ADJUSTMENT		PRO FORMA
ASSETS				
Current assets:				
Cash and cash equivalents	$ 27,303	(1,018)	1	26,285
Investment -UMC	340,126	-		340,126
Short-term investments	62,807	-		62,807
Accounts receivable, net	81,194	(36,502)	1	44,692
Inventory	87,062	(56,662)	1	30,400
Prepaid expenses and other assets	14,159	(2,161)	1	11,998
Total current assets	612,651	(96,343)		516,308
Property, plant and equipment, net	27,988	(9,765)	1	18,223
Investment - UMC	406,363	-		406,363
Other investments	32,483	-		32,483
Goodwill and intangible assets	171,195	-		171,195
Other assets	13,130	-		13,130
Total Assets	$1,263,810	(106,108)		1,157,702
LIABILITIES AND STOCKHOLDERS' EQUITY				
Current liabilities:				
Accounts payable	$ 86,155	(30,784)	1	$ 55,371
Notes payable	54,381	--		54,381
Accrued liabilities	59,669	(6,867)	1	52,802
Deferred taxes	39,014	--		39,014
Deferred revenue	7,882	(314)	1	7,568
Total current liabilities	247,101	(37,965)		209,136
Deferred taxes	106,796	--		106,796
Other liabilities	5,151	(653)	1	4,498
Convertible subordinated debentures	103,500	--		103,500
Total liabilities	462,548	(38,618)		423,930
Stockholders' equity:				
Common stock	591,120	(46,861)	4,5	544,259
Accumulated other comprehensive losses	(126,052)	--		(126,052)
Accumulated earnings	336,194	(20,629)	1,4,5	315,565
Total stockholders' equity	801,262	(67,490)		733,772
TOTAL LIABILITIES AND STOCKHOLDERS' EQUITY	$1,263,810	(106,108)		1,157,702

See Accompanying Notes to Unaudited Pro Forma Condensed Consolidated Financial Statements.

SONICBLUE INCORPORATED
UNAUDITED PRO FORMA CONDENSED CONSOLIDATED
STATEMENT OF OPERATIONS
NINE MONTHS ENDED SEPTEMBER 30, 2000
(IN THOUSANDS, EXCEPT PER SHARE AMOUNTS)

	HISTORICAL	ADJUSTMENTS	PRO FORMA
Net sales	$ 437,499	(192,913) 2	244,586
Cost of sales	439,323	(173,491) 2	265,832
Gross margin (loss)	(1,824)	(19,422)	(21,246)
Operating expenses:			
Research and development	63,708	(17,680) 2	46,028
Selling, marketing and admin	88,102	(8,124) 2	79,978
Restructuring expenses	8,981	--	8,981
Amortization of goodwill	33,354	--	33,354
Total operating expenses	194,145	(25,804)	168,341
Income (loss) from operations	(195,969)	6,382	(189,587)
Gain on sale of joint venture	14,738	--	14,738
Gain on UMC investment	873,749	--	873,749
Gain on other investment	5,917	--	5,917
Other income (expense)	(2,539)	538 2	(2,001)
Income before income taxes	695,896	6,920	702,816
Provision for income taxes	306,183	--	306,183
Income before minority interest	389,713	6,920	396,633
Minority interest in Rioport	(9,374)	--	(9,374)
Net income	380,339	6,920	387,259
Net income per share:			
Basic	$4.25		$5.07
Diluted	$3.79		$4.39
Number of shares used in computing net income per share:			
Basic	89,416		76,416
Diluted	101,179		88,179

See Accompanying Notes to Unaudited Pro Forma Condensed Consolidated Financial Statements.

SONICBLUE INCORPORATED
UNAUDITED PRO FORMA CONDENSED CONSOLIDATED
STATEMENT OF OPERATIONS
YEAR ENDED DECEMBER 31, 1999
(IN THOUSANDS, EXCEPT PER SHARE AMOUNTS)

	HISTORICAL	ADJUSTMENTS		PRO FORMA
Net sales	$ 352,583	136,071	3	488,654
Cost of sales	307,161	184,990	3	492,151
Gross margin (loss)	45,422	(48,919)		(3,497)
Operating expenses:				
Research and development	73,896	(43,645)	3	30,251
Selling, marketing and admin	52,832	49,960	3	102,792
Other operating expenses	6,700	--		6,700
Amortization of goodwill	12,156	--		12,156
Total operating expenses	145,584	6,315		151,899
Loss from operations	(100,162)	(55,234)		(155,396)
Gain on sale of joint venture	22,433	--		22,433
Other expense	(913)	(4,707)	3	(5,620)
Loss before income taxes	(78,642)	(59,941)		(138,583)
Provision (benefit) for income taxes	(47,916)	--		(47,916)
Loss before joint venture and minority interest	(30,726)	(59,941)		(90,667)
Equity in income from joint venture	4,588	--		4,588
Minority interest in Rioport	(4,642)	--		(4,642)
Net loss	(30,780)	(59,941)		(90,721)
Net loss per share:				
Basic	$(0.52)			$(1.96)
Diluted	$(0.52)			$(1.96)
Number of shares used in computing net loss per share:				
Basic	59,244			46,244
Diluted	59,244			46,244

See Accompanying Notes to Unaudited Pro Forma Condensed Consolidated Financial Statements.

NOTES TO UNAUDITED PRO FORMA
CONDENSED CONSOLIDATED FINANCIAL STATEMENTS

BASIS OF PRESENTATION

On January 3, 2001, SONICblue Incorporated (formerly S3 Incorporated) ("SONICblue"), completed the transactions contemplated by the Amended and Restated Investment Agreement, dated as of August 28, 2000 between SONICblue and VIA Technologies, Inc. ("VIA"), and a joint venture. At the closing, SONICblue completed the transfer of its graphics chips assets and liabilities to S3 Graphics Co., Ltd., a joint venture ("JV") between a wholly owned subsidiary of SONICblue and VIA. Under the terms of the agreement, SONICblue received 13 million shares of its common stock as initial payment from VIA and 100 million shares of Class A Common Stock of the JV. The agreement provides that, upon occurrence of certain events, SONICblue shall pay damages subject to a maximum damages cap.

Also, SONICblue will receive earn-out payments if the new venture meets certain aggressive profitability goals. The effect of the earn-out payments has not been presented in the unaudited pro forma financial statements.

The agreement provides that the Class A shareholders, Class B shareholders and Class C shareholders shall have 50%, 48% and 2%, respectively, of the voting power of JV irrespective of the actual number of outstanding shares of such class with respect to the election of directors and own 0.1%, 99.4% and 0.5%, respectively, of the economic interest of JV.

At closing, SONICblue granted a wholly owned subsidiary of VIA a warrant (the "Warrant") to purchase up to 2 million shares of SONICblue common stock at an exercise price of $10.00 per share, for an aggregate exercise price of $20 million. The Warrant expires on January 3, 2005, unless terminated earlier pursuant to its terms. The fair value of the Warrant is recorded in the pro forma balance sheet.

The unaudited pro forma condensed consolidated statement of operations for the year ended December 31, 1999 also includes pro forma results of the acquisition of Diamond Multimedia Systems, Inc. ("Diamond"). Diamond was acquired by SONICblue on September 24, 1999. The unaudited pro forma condensed consolidated statement of operations for the year ended December 31, 1999 has been prepared as if the acquisition of Diamond had occurred on January 1, 1999.

NOTES TO UNAUDITED PRO FORMA CONDENSED CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

WEIGHTED AVERAGE SHARES OUTSTANDING

For the nine months ended September 30, 2000, the pro forma number of shares used in computing net income was calculated as follows:

DESCRIPTION	YEAR ENDED DECEMBER 31, 1999 (BASIC AND DILUTED)	NINE MONTHS ENDED SEPT. 30, 2000	
		BASIC	DILUTED
Weighted average shares outstanding	59,244	89,416	101,179
Decrease in common shares attributable to the cancellation of SONICblue common stock	13,000	13,000	13,000
Total pro forma shares assumed outstanding	46,244	76,416	88,179

ADJUSTMENTS

The unaudited pro forma condensed statements give effect to the following pro forma adjustments:

(1) To reflect the elimination of assets transferred to and liabilities assumed by the JV in exchange for the consideration referenced in (4) below.

(2) To eliminate the operating results of the disposed graphics chip business for the nine months ended September 30, 2000.

(3) To eliminate the operating results of the disposed graphics chip business for the year ended December 31, 1999 and to reflect the operations of Diamond Multimedia Systems, Inc. as if the acquisition occurred as at January 1, 1999.

(4) To reflect the receipt and cancellation of 13 million shares of SONICblue common stock at a value of $57,241 (valued as of January 3, 2001) and the resulting loss of approximately $20,629.

(5) To record the fair value of the issuance of the Warrant of $10,380.

(c) Exhibits.

2.1*	Investment Agreement, dated as of August 28, 2000, among the Registrant, VIA Technologies, Inc. and JV.
2.2*	Letter dated January 3, 2001 from the Registrant to S3 Graphics Co., Ltd. in reference to Section 2.2(f) of the Investment Agreement.
4.1*	Common Stock Purchase Warrant of the Registrant, dated January 3, 2001, issued in the name of VIABASE, Inc. (BVI).
99.1	Joint Venture Agreement, dated as of January 3, 2001, between the Registrant, Sonica3, Inc. and VIA Technologies, Inc. (as amended).
99.2*	Amended and Restated Investor Rights Agreement, dated as of January 3, 2001, between the Registrant and VIABASE, Inc.
99.3*	Class A Shares Option Agreement, dated as of January 3, 2001, between Sonica3, Inc. and VIA Technologies, Inc.

* Filed previously.

SIGNATURE

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned hereunto duly authorized.

Dated: February 27, 2001.

SONICBLUE INCORPORATED

By /s/ William F. McFarland
William F. McFarland
Controller and Interim Chief Financial Officer

INDEX TO EXHIBITS

Exhibit Number	Description
2.1*	Investment Agreement, dated as of August 28, 2000, among the Registrant, VIA Technologies, Inc. and JV. The exhibits to the Investment Agreement, as listed in the table of contents thereto, have been omitted. The Registrant will furnish copies of the omitted exhibits to the Commission upon request.
2.2*	Letter dated January 3, 2001 from the Registrant to S3 Graphics Co., Ltd. in reference to Section 2.2(f) of the Investment Agreement.
4.1*	Common Stock Purchase Warrant of the Registrant, dated January 3, 2001, issued in the name of VIABASE, Inc. (BVI).
99.1	Joint Venture Agreement, dated as of January 3, 2001, between the Registrant, Sonica3, Inc. and VIA Technologies, Inc. (as amended). The exhibits to the Joint Venture Agreement, as listed in the table of contents thereto, have been omitted. The Registrant will furnish copies of the omitted exhibits to the Commission upon request.
99.2*	Amended and Restated Investor Rights Agreement, dated as of January 3, 2001, between the Registrant and VIABASE, Inc.
99.3*	Class A Shares Option Agreement, dated as of January 3, 2001, between Sonica3, Inc. and VIA Technologies, Inc.

* Filed previously.

EXHIBIT 99.1

JOINT VENTURE AGREEMENT

BETWEEN

SONICBLUE INCORPORATED,

SONICA3, INC.

AND

VIA TECHNOLOGIES, INC.

DATED AS OF JANUARY 3, 2001

TABLE OF CONTENTS

TABLE OF CONTENTS
(continued)

JOINT VENTURE AGREEMENT

This Joint Venture Agreement (this "Agreement"), dated as of January 3, 2001 between SONICblue Incorporated, a corporation organized under the laws of the State of Delaware and Sonica3, Inc., a Delaware corporation (collectively "SONICblue" unless otherwise indicated herein), and VIA Technologies, Inc., a corporation organized under the laws of Taiwan ("VIA").

INTRODUCTION

A. SONICblue is engaged in the manufacture and sale of graphic accelerators and has a wide and rich experience in this field of industry.

B. VIA is engaged in the manufacture and sale of core logic chipsets and has a wide and rich experience in this field of industry.

C. SONICblue and VIA desire to form a corporation under the laws of the Cayman Islands ("JV") for the purpose of manufacturing and distributing graphics products and conducting related research and development activities. SONICblue Incorporated has designated Sonica3, Inc. to hold the Class A Common Shares of JV pursuant to Section 2.2(f) of the Investment Agreement (as defined below).

IN CONCLUSION, in consideration of the foregoing premises and the covenants contained herein, the parties agree as follows:

1. DEFINITIONS. Unless otherwise defined herein, capitalized terms used in this Agreement shall have the meanings ascribed to them in the Investment Agreement (as defined below). In addition, for the purpose of this Agreement, the following terms shall have the meanings hereinafter set forth:

1.1. "Articles of Association" shall mean the Articles of Association of JV attached hereto as Exhibit A, as amended from time to time.

1.2. "Board of Directors" shall mean the board of directors of JV as from time to time constituted pursuant to the terms of this Agreement.

1.3. "Business Day" shall mean any day except a Saturday, Sunday or other day on which commercial banks in New York are authorized or required by law or executive order to close.

1.4. "Class A Common Shares," "Class B Common Shares" and "Class C Common Shares" are defined in the Memorandum of Association.

1.5. "Confidential Information" shall mean any trade secrets, know-how, data, formulas, processes, source code, netlists, Intellectual Property or other nonpublic information, tangible or intangible, of one party that becomes known by the other party.

Any information exchanged by the parties and entitled to protection under this Agreement shall be identified as such by appropriate marking as "Confidential" on any documents exchanged, or, if the disclosure has been made orally or if it is not feasible to mark the disclosed information, then the disclosing party shall identify the information as "Confidential" at the time of disclosure and, within two (2) weeks of the disclosure, shall confirm in writing the confidential nature of such disclosure.

1.6. "Independent Accounting Firm" shall mean a certified public accounting firm qualified under the laws of the United States that, under the rules of the American Institute of Certified Public Accountants and the SEC, is independent from the Person retaining such firm.

1.7. "Investment Agreement" shall mean the Amended and Restated Investment Agreement, between SONICblue and VIA, dated as of August 28, 2000.

1.8. "Memorandum of Association" shall mean the Memorandum of Association of JV attached hereto as Exhibit B, as amended from time to time.

1.9. "Transfer", when used as a verb, shall mean to sell, pledge, assign, encumber, dispose of or otherwise transfer (including by merger, testamentary disposition, interspousal disposition pursuant to a domestic relations proceeding or otherwise or otherwise by operation of law), or, when used as a noun, means a sale, pledge, assignment, encumbrance, disposition, or other transfer (including a merger, testamentary disposition, interspousal disposition pursuant to a domestic relations proceeding or otherwise or other transfer by operation of law).

2. INCORPORATION.

2.1. Formation of JV. On the day prior to the Closing Date and after receipt of all Government Approvals, the Parties shall form JV by filing the Memorandum of Association and Articles of Association in the forms attached hereto as Exhibits A and B. On the Closing Date, the parties shall cause JV to execute this Agreement, the Investment Agreement, and the other JV Transaction Agreements to which it is a party and, thereupon, it shall become a party to this Agreement and the Investment Agreement, and the other JV Transaction Agreements to which it is a party.

2.2. The Name of JV. The name of JV shall be set forth in the Memorandum of Association as S3 Graphics Co., Ltd.

2.3. Principal Offices. The principal office and place of business of JV shall be located at 2841 Mission College Boulevard, Santa Clara, California, or at such other place as the Board of Directors may from time to time designate. The registered office of the company shall be at the offices of Charles Adams, Ritchie & Duckworth, P.O. Box 709 GT, Zephyr House, Mary Street, Grand Cayman, Cayman Islands, B.W.I.

2.4. Capital Contributions; Liabilities.

2.4.1 The authorized capital stock of JV shall consist of the number and classes of shares set forth in the Memorandum of Association and each class of shares shall have such rights, preferences and privileges, and the qualifications, limitations or restrictions thereof, as are described in the Memorandum of Association. The parties hereby agree to form JV through the filing of the Memorandum of Association and Articles of Association, which provide that the Class A shareholders the Class B shareholders and Class C shareholders shall have fifty percent (50%), forty-eight percent (48%) and two percent (2%), respectively, of the voting power of JV irrespective of the actual number of outstanding shares of such class with respect to the election of directors and own one tenth of one percent (.1%), ninety-nine and four tenths percent (99.4%), and one-half of one percent (.5%), respectively, of the economic interest of JV. SONICblue or its designee shall own all outstanding shares of Class A stock and JV shall not, except for Class B shares and Class C shares, authorize any other class of shares with rights to vote for the election of directors.

2.4.2 SONICblue shall contribute the Graphics Chip Business Assets to such entity or entities as JV designates and execute and deliver all of the JV Transaction Agreements to which it is a party, and JV shall issue to SONICblue Incorporated or its designee 100,000,000 shares of its Class A Common Shares.

2.4.3 VIA or its designee shall contribute to JV the cash and/or securities set forth in Section 2.2(c) of the Investment Agreement and execute and deliver all of the JV Transaction Agreements to which it is a party, and JV shall issue to VIA or its designee 30,000,000 shares of its Class B Common Shares. VIA shall retain all of its shares of Class B Common Shares in one entity.

2.4.4 Wallvision Electronic Inc. shall contribute to JV $ 337,525 and JV shall issue to Wallvision Electronic Inc. 200,000 shares of Class C Common Shares.

2.4.5 VIA shall make such additional contributions of cash and/or securities to JV as JV and VIA shall from time to time determine are necessary or advisable. Subject to the terms of the Investment Agreement, JV shall assume the Assumed Liabilities. No other liabilities or obligations of SONICblue of any nature, whether known or unknown, whether fixed or contingent, accrued or unaccrued, shall be assumed by JV, and such liabilities and obligations shall remain the responsibility of SONICblue.

2.5. Reimbursement of Incorporation Expenses. JV shall reimburse the party hereto acting as the incorporator for reasonable expenses incurred directly by it in connection with the incorporation of JV to the extent permitted under the laws of the Cayman Islands.

2.6. Profit-Based Earn Out. JV shall pay SONICblue $100 million in each of fiscal years 2001 and 2002 if JV earns annual net operating income (before income taxes, extraordinary transactions and non-recurring items) in excess of $500 million in each of such fiscal years determined in accordance with GAAP. Such payment shall be in cash and shall be paid within 10 business days following the release of JV's audited financial statements for such applicable fiscal years.

3. MANAGEMENT OF JV.

3.1. Meetings and Resolutions of Stockholders. Meetings of shareholders may be called from time to time in accordance with the Articles of Association, and convened in accordance with the provisions thereof.

3.2. Election of Directors. JV shall be administered by a Board of Directors composed of six (6) directors. The Board of Directors shall be divided into three classes of two each. One class of directors shall be subject to reelection at each annual meeting of the stockholders. The initial members of the Board of Directors and their respective reelection year shall be as follows:

Class I (Term Expires in 2001)	Class II (Term Expires in 2002)	Class III (Term Expires in 2003)
Cher Wang	Jonathan Chang	
Tzu-Mu Lin	Timothy Chen	Kenneth Potashner
		Wen-Chi Chen

3.3. Officers.

3.3.1 The Board of Directors shall appoint the officers of JV and vest them with such titles and powers, as required by Applicable Law.

3.3.2 Each of the parties hereto shall cause the directors it has nominated to exercise their voting rights as members of the Board of Directors to elect the following persons as the initial officers of JV:

Chief Executive Officer: Wen-Chi Chen Chief Financial Officer: Gerry Liu

3.4. Statement of Policy.

3.4.1 The parties hereto intend that the business and affairs of JV be carried on and conducted in a sound, prudent and constructive manner for the purpose of building a successful and financially strong corporation.

3.4.2 The day-to-day operations of JV shall be managed by the officers appointed under Section 3.3.2 above and supervised by the Board of Directors. Such operations shall be conducted in accordance with the policies established by the Board of Directors and pursuant to such resolutions as the Board of Directors may from time to time adopt.

3.5. Accounting and Reporting Obligations.

3.5.1 JV's fiscal year shall be the 12 month period ending on December 31.

3.5.2 The Board of Directors shall designate an Independent Accounting Firm.

3.5.3 The annual accounting report of JV shall be audited at the expense of JV by its Independent Accounting Firm in accordance with generally accepted auditing standards.

4. RIGHTS AND OBLIGATIONS OF THE PARTIES.

4.1. Reports and Statements. JV shall provide the following reports and statements to the parties within the time periods set forth below:

(a) Within 45 days after the close of each fiscal quarter, a report on booking and billing quarterly results, balance sheet, statement of operations and cash flow statement.

(b) Within 3 months after the end of each fiscal year, a report on booking and billing annual results, balance sheet, statement of operations, cash flow statement and statement of shareholders equity.

4.2. Transfer of Shares. No shares of Class A Common Shares shall be Transferred for consideration or otherwise other than to a party hereto or a subsidiary or designee of a party to this Agreement unless the other shareholder(s) consent(s) in writing to such Transfer. If SONICblue or Sonica3 proposes to Transfer any shares of Class A Common Shares, then VIA and JV shall have a right of first refusal (the "Right of First Refusal") to purchase some or all of such shares of Class A Common Shares proposed to be Transferred. SONICblue or Sonica3 shall give a written notice (the "Transfer Notice") to VIA and JV describing fully the proposed Transfer including the number of shares proposed to be Transferred, the proposed Transfer price and the name and address of the proposed transferee. The Transfer Notice shall be signed both by SONICblue or Sonica3 and by the proposed transferee and must constitute a binding commitment of both such parties for the Transfer of such Class A Common Shares. VIA or JV shall exercise this Right of First Refusal by delivery of a notice of exercise to SONICblue or Sonica3 within 30 days after the receipt of the

Transfer Notice by SONICblue or Sonica3. Such notice shall indicate the number of shares of Class A Common Shares VIA and JV wish to purchase under this Right of First Refusal. SONICblue or Sonica3 shall then sell to VIA and JV on a date set by VIA or JV which is not more than 30 days after the date of its response notice the number of shares set forth in the response notice at a price per share equal to the proposed per share Transfer price and on the payment terms set forth in the Transfer Notice. If VIA and JV elect to purchase none or less than all of the shares of Class A Common Shares to be Transferred by SONICblue or Sonica3, SONICblue or Sonica3 may Transfer all of such shares, or the balance of such shares, as the case may be, to the proposed transferee on the terms set forth in the Transfer Notice. If the proposed Transfer price or the terms of payment set forth in the Transfer Notice changes, or if the sale of the Class A Common Shares is not consummated with the proposed transferee within 30 days of JV's or VIA's response notice, SONICblue or Sonica3 shall be required to reinstitute the above procedures if it intends to Transfer its Class A Common Shares on such different terms or after the aforesaid 30-day period.

4.3. Confidentiality.

4.3.1 Except as expressly authorized by the disclosing party, each party agrees not to disclose or permit the disclosure or use by others of any Confidential Information of the disclosing party, and agrees that it will use such Confidential Information only for the purpose of its Graphics Chip Business. The restrictions on use and disclosure of Confidential Information shall not apply to the extent such Confidential Information (i) becomes a matter of public knowledge through no action or inaction of the party receiving the Confidential Information, (ii) was in the receiving party's possession before receipt from the party providing such Confidential Information, (iii) is rightfully received by the receiving party from a third party without any duty of confidentiality, (iv) is disclosed to a third party by the party providing the Confidential Information without a duty of confidentiality on the third party, (v) is disclosed with the prior written approval of the party providing such Confidential Information, or (vi) is independently developed by the receiving party without any use of the other party's Confidential Information. Disclosure of the other party's Confidential Information by the receiving party shall not constitute a material breach of this Agreement, if the disclosing party can prove that the disclosure occurred despite the receiving party's exercise of the same degree of care used by the receiving party to safeguard its own similar type of Confidential Information, but in no event less than a reasonable degree of care, and that the receiving party has used best efforts to minimize any adverse effects resulting from such disclosure and to prevent any further use or unauthorized disclosure.

4.3.2 In furtherance, and not in limitation of the foregoing
Section 4.3.1, each party agrees to do the following with respect to any such Confidential Information: (i) exercise the same degree of care to safeguard the confidentiality of, and prevent the unauthorized use of, such information as that party exercises to safeguard the confidentiality of its own similar type of Confidential Information; (ii) restrict disclosure

of such information to those of its employees and agents who have a "need to know" and, with prior written approval of the disclosing party, those of its third party contractors who have a "need to know," and (iii) instruct, require and obtain the written agreement of such employees, agents and subcontractors to maintain the confidentiality of such information and not to use such Confidential Information except as expressly permitted. Each party further agrees not to remove or destroy any proprietary or confidential legends or markings placed upon any documentation or other materials.

4.3.3 The terms and conditions of this Agreement are Confidential Information, provided, however, that either party may disclose this Agreement:
(a) to its legal and financial advisers on a need-to-know basis; (b) to third-party financing sources on a need-to-know basis and subject to a non-disclosure agreement; and (c) to the extent necessary to comply with Applicable Law, including, but not limited to SEC regulations, provided that the party proposing to make such disclosure shall, if possible, provide prior notice to the other party and an opportunity to reasonably contest the need for such disclosure. In addition, either party may disclose the general terms and conditions of this Agreement (but not the Agreement itself) to customers of JV's products under a non-disclosure agreement.

4.3.4 The obligations under this Section 4.3 shall not prevent the parties from disclosing the Confidential Information or terms of this Agreement to any Governmental Authority as required by law (provided that the party intending to make such disclosure in such circumstances has given the other party prompt notice prior to making such disclosure so that the other party may seek a protective order or other appropriate remedy prior to such disclosure and cooperates fully with such other party in seeking such order or remedy).

4.3.5 Each party shall be free to use for any purpose (including, but not limited to, use in the development, manufacture, marketing and maintenance of its own products and services) the Residuals (as defined below) resulting from access to or work with Confidential Information, provided that the party maintains the confidentiality of the Confidential Information as provided herein, and nothing herein shall be deemed to grant a license under any patents that may cover such Residuals. The term "Residuals" shall mean information in non-tangible form that may be inadvertently retained by persons who have had rightful access to the Confidential Information, including the ideas, concepts, know-how or techniques contained therein. Notwithstanding the provisions of this Section 4.3.5, neither party may avoid its obligations toward a particular item of Confidential Information merely by having a person commit such item to memory so as to reduce it to a non-tangible form.

The obligations under this Section 4.3 shall apply with respect to any Confidential Information for a period of five (5) years from the date of disclosure of such Confidential Information to the other party, unless with respect to any particular Confidential

Information the providing party in good faith notifies the receiving party that a longer period shall apply, in which case the obligations under this Section 4.3 with respect to such Confidential Information shall apply for such longer period.

5. TERM AND TERMINATION.

5.1. Closing Date. This Agreement shall come into force on the Closing Date and shall remain in effect until terminated in accordance with the terms of this Section 5.

5.2. Term. The term of this Agreement shall be perpetual unless otherwise provided for in this Agreement.

5.3. Termination Events. This Agreement shall terminate:

5.3.1 If the Investment Agreement terminates, whether before or after the Closing; or

5.3.2 If SONICblue or its successor-in-interest by operation of law sells, assigns, transfers, pledges or otherwise disposes of the Class A Common Stock pursuant to the terms of this Agreement or the Class A Shares Option Agreement.

5.4. Nonsolicitation. So long as a party or its Affiliate(s) holds shares in JV, except as otherwise agreed by the parties, such party and its Affiliate(s) shall be prohibited from soliciting for employment or recommending for employment any person employed by the other party, an Affiliate of the other party or by JV. The foregoing restrictions shall not apply to or be breached by (i) advertising of open positions, participating in job fairs and comparable activities, or other forms of soliciting candidates for employment which are general in nature and not directed specifically at any such employees, (ii) responding to unsolicited inquiries about employment opportunities or possibilities from job placement agencies or other agents acting for unidentified principals, or (iii) responding to unsolicited inquiries about employment opportunities from any individual.

6. MISCELLANEOUS.

6.1. Force Majeure. No party shall be liable for failure to perform (other than payment of amounts due), in whole or in material part, its obligations under this Agreement, if such failure is caused by acts of God, earthquakes, fires, natural disasters, explosions, declared public states of emergency due to acts of public enemy, riots, civil commotion and insurrection, or any other similar catastrophic casualty, occurrence, condition, event or circumstance not reasonably within the excused Party's control and which could not have been anticipated and avoided by reasonable measures; provided, however, that Force Majeure shall not include any action or failure to act by the

Government of Taiwan or any agency, committee or subdivision thereof, including, without limitation, any act, order or injunction against (or failure to approve, where such approval is legally required to accomplish) the transfer of funds or property pursuant to, or the consummation of any other action contemplated by, this Agreement

6.2. Assignment. Except as provided herein or in the Investment Agreement, neither this Agreement nor any of the rights and obligations created hereunder may be assigned, transferred, pledged, or otherwise encumbered or disposed of, in whole or in part, whether voluntary or by operation of law, or otherwise, by either party without the prior written consent of the other party, and any attempt to do so, contrary to the terms of this Agreement, shall be null and void.

6.3. Survival. Without limiting any provision in any of the JV Transaction Agreements, the obligations of the parties pursuant to Sections 2.5 (Reimbursement of Incorporation Expenses), 2.6 (Profit-Based Earn Out), 4.3 (Confidentiality), 5.4 (Nonsolicitation), 6.3 (Survival), 6.4 (Notices), and 6.6 through 6.17 shall survive the termination of this Agreement.

6.4. Notices. All notices, requests, consents, demands, instructions, approvals and other communications hereunder shall be in writing and shall be validly given, made or served, if delivered personally or sent by mail, recognized courier service, telex or telefax (confirmed by mail or recognized courier service in the case of telefaxes), and shall be deemed effective when actually received, as follows:

If to SONICblue Incorporated or to Sonica3, Inc., to:

SONICblue Incorporated/ or to Sonica3, Inc., as applicable 2841 Mission College Blvd.
Santa Clara, California 95054
Attention: President
Fax: (408) 588-8050

With copies to:

Pillsbury Winthrop LLP
2550 Hanover Street
Palo Alto, California 94304
Attention: Jorge A. del Calvo, Esq. Fax: (650) 233-4545

If to VIA, to:

VIA Technologies, Inc.
8F, No. 553 Chung-Cheng Road

Hsing-Tien,Taipei
Taiwan
Attention: President
Telecopier: 886-2-2218-7970

With a copies to:

Heller Ehrman White & McAuliffe LLP 525 University Avenue
Palo Alto, California 94301-1900 Attention: Sarah A. O'Dowd, Esq. Fax: (415) 324-0638

If to JV, to:

S3 Graphics Co., Ltd.
c/o VIA Technologies, Inc.
2841 Mission College Blvd.
Santa Clara, California 95054
Attention: President
Fax: (408) 588-8050

With copies to S3 and VIA as above provided or to such other address or addresses as any party may from time to time designate in writing delivered in a like manner to the other parties hereto.

6.5. Export Control. Without in any way limiting the provisions of this Agreement, each of the parties agrees that no products procured from or technical information disclosed by the other party or JV under this Agreement are intended to or shall be exported or re-exported, directly or indirectly, to any destination restricted or prohibited by Applicable Law without necessary authorization by the Governmental Authorities.

6.6. Entire Agreement. This Agreement, the Investment Agreement and the JV Transaction Agreements and the exhibits and schedules hereto and thereto, embody the entire agreement and understanding between the parties with respect to the subject matter hereof, superseding, as of the Closing Date, all previous and contemporaneous communications, representations, agreements and understandings, whether written or oral, in existence on the date this Agreement is executed. Neither party has relied upon any representation or warranty of the other party except as expressly set forth herein.

6.7. Modification. This Agreement and the surviving provisions thereof may not be modified or amended, in whole or part, except by a writing executed by duly authorized representatives of both parties.

6.8. Severability. If any term or provision of this Agreement shall, for any reason, be held to be invalid, illegal or unenforceable, such provision shall be deemed severed from this Agreement. The remaining provisions of this Agreement shall remain in full force and effect, and shall be construed and interpreted in a manner that corresponds as closely as possible with the intentions of the parties as expressed in this Agreement.

6.9. No Waiver. Except to the extent that a party hereto may have otherwise agreed in writing, no waiver by that party of any condition of this Agreement or breach by the other party of any of its obligations or representations hereunder shall be deemed to be a waiver of any other condition or subsequent or prior breach of the same or any other obligation or representation by the other party, nor shall any forbearance by the first party to seek a remedy for any noncompliance or breach by the other party be deemed to be a waiver by the first party of its rights and remedies with respect to such noncompliance or breach.

6.10. Governing Law and Dispute Resolution. This Agreement shall be governed by and construed in accordance with the laws of the State of Delaware without regard to conflicts of law. For purposes of any action or proceeding involving this Agreement, JV hereby expressly submits to the jurisdiction of all federal and state courts located in the State of California and consents to be served with any process or paper by registered mail or by personal service within or without the State of California.

6.11. Language. This Agreement, and the exhibits and schedules hereto, including the Memorandum of Association and Articles of Association, are in the English language, which language shall be controlling in all respects.

6.12. No Agency. This Agreement shall not constitute an appointment of either party as the legal representative or agent of the other party, nor shall either party have any right or authority to assume, create or incur in any manner any obligation or other liability of any kind, express or implied, against, in the name or on behalf of, the other party. Nothing herein or in the transactions contemplated by this Agreement shall be construed as, or deemed to be, the formation of a partnership by or among the parties. No party has the authority to make, on behalf of the JV or the other party, an election for the JV to be taxable as other than a corporation for United States federal income tax purposes.

6.13. No Third Party Beneficiaries. No provisions of this Agreement are intended to, or shall be construed to, confer upon or give to any person other than the

parties hereto and thereto, any rights, remedies or other benefits under or by reason of such agreements.

6.14. Headings. The section and other headings contained in this Agreement are for convenience of reference only and shall not be deemed to be a part of this Agreement or to affect the meaning or interpretation of this Agreement.

6.15. Construction and Reference. Words used in this Agreement, regardless of the number or gender specifically used, shall be deemed and construed to include any other number, singular or plural, and any other gender masculine, feminine or neutral, as the context shall require. Unless otherwise specified, all references in this Agreement to Sections are deemed references to be corresponding Sections in this Agreement, and all references in this Agreement to Exhibits are references to the corresponding Exhibits attached to this Agreement.

6.16. Governmental Approvals. Each of the parties shall use its reasonable best efforts to obtain all Governmental Approvals and shall cooperate with the other parties in good faith.

6.17. Counterparts. This Agreement may be executed in counterparts, each of which shall be deemed an original, and all of which shall be deemed to constitute one and the same instrument.

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be executed by their duly authorized representatives on the date set forth above.

SONICblue Incorporated	VIA Technologies, Inc.
_____	_____
Signature	Signature
By: /s/ Ken Potashner	By: /s/ Jonathan Chang
_____	_____
Ken Potashner Chief Executive Officer	Wen-Chi Chen* President and Chief Executive Officer *By power of attorney
Date:	Date:
_____	_____
Acknowledged and adopted by:	
S3 Graphics Co., Ltd.	Sonica3, Inc.
/s/ Shao-Hung Gerald Liu	/s/ Ken Potashner
_____	_____
Signature	Signature
By:	By:
_____	_____
Shao-Hung Gerald Liu Chief Financial Officer	Ken Potashner Chief Executive Officer
Date:	Date:
_____	_____

Exhibit 13

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EXHIBIT 2.1

AMENDED AND RESTATED INVESTMENT AGREEMENT

AMONG

S3 INCORPORATED

VIA TECHNOLOGIES, INC.

AND

JV

DATED AS OF AUGUST 28, 2000

TABLE OF CONTENTS

<TABLE>
<CAPTION>

<TABLE>
<S> <C>

<TABLE>
<S> <C>

</TABLE>

<TABLE>
<CAPTION>
EXHIBITS

<S>	<C>
Exhibit 1	Class A Shares Option Agreement
Exhibit 4	Joint Venture Agreement
Exhibit 5	Non-Competition Agreement
Exhibit 8	Intellectual Property Cross License Agreement
Exhibit 9	S3 Warrant and Amended and Restated Investor Rights Agreement
Exhibit 10	Guaranty
Exhibit 11	Trademark License Agreement
Exhibit 12	Employees and Consultants bound by the Proprietary Rights and Information Agreement
Exhibit 13	Form of S3 Counsel's Opinion
Exhibit 14	Escrow Agreement
Exhibit 15	Management Agreement
Exhibit 16	Release

</TABLE>

<TABLE>
<CAPTION>
SCHEDULES

<S>	<C>
Schedule A	Assumed Liabilities
Schedule B	Additional Disclosure Schedule
Schedule 3.3	S3 Stock Options
Schedule 3.4	Consents (S3)
Schedule 3.5(c)	February 27, 2000 Balance Sheet
Schedule 3.6	Taxes
Schedule 3.7	Litigation
Schedule 3.8	Compliance with Laws
Schedule 3.9	Business Operations not through S3, the S3 Subsidiaries or any other division or Affiliate
Schedule 3.10	Contributed Assets
Schedule 3.11(a)	Graphics Chip Business Contracts
Schedule 3.11(a)(i)	Employment Contracts

</TABLE>

<TABLE>
<S> <C>

</TABLE>

AMENDED AND RESTATED INVESTMENT AGREEMENT

This Amended and Restated Investment Agreement, dated as of August 28, 2000, by and among S3 Incorporated, a corporation organized under the laws of the State of Delaware ("S3") and VIA Technologies, Inc., a corporation organized under the laws of Taiwan ("VIA").

W I T N E S S E T H:

WHEREAS, S3 and VIA desire to form a corporate joint venture ("JV") for the purpose of manufacturing and distributing graphics products and conducting related research and development activities; and

WHEREAS, the Parties desire to provide for the transfer from S3 to JV of certain assets comprising certain of the assets used by S3 in its graphics chip products business, in exchange for JV stock and the transfer by VIA or its designee of cash and/or S3 stock to JV in exchange for JV stock; and

WHEREAS, on April 10, 2000, S3 and VIA entered into an Investment Agreement (the "Investment Agreement") which memorialized their agreements and obligations with regard to the above-described transactions; and

WHEREAS, circumstances have changed since the Parties executed the Investment Agreement and the Parties now wish to amend and restate their agreements and obligations on the terms set forth herein;

NOW, THEREFORE, in consideration of the premises and the representations, warranties, covenants and agreements herein contained, the Parties hereto hereby agree that the Investment Agreement shall be amended and restated as follows:

ARTICLE 1.

DEFINITIONS

For purposes of this Agreement, the following terms shall have the meanings set forth below:

"Additional Capital Assets" has the meaning set forth in Section 5.22.

"Affiliate" means, with respect to any Person, any other Person directly or indirectly controlling, controlled by or under common control with such other Person; provided, however, that for purposes of this Agreement JV shall not be deemed to be an Affiliate of or controlled by any of the Parties, and provided, further, that neither S3 nor VIA should be deemed to be an Affiliate of the other.

"Agreement" means this Amended and Restated Investment Agreement, as it may be amended from time to time pursuant to Section 10.1 hereof, and the Exhibits and Schedules listed in the table of contents hereto.

"Additional Disclosure Schedules" means the schedules attached hereto which contains material amendments or modification to the Schedules and Exhibits to the Investment Agreement, in the form delivered by S3 to VIA pursuant to Section 6.1(h) of the Investment Agreement.

"Applicable Law" means all applicable provisions of all (i) constitutions, treaties, statutes, laws (including the common law), rules, regulations, ordinances, codes or orders of any Governmental Authority, (ii) Governmental Approvals and (iii) orders, decisions, injunctions, judgments, awards and decrees of or agreements with any Governmental Authority.

"Assumed Liabilities" means the liabilities for inventory purchases and other items agreed to by the Parties only, and described in Schedule A hereto.

"Class A Shares Option Agreement" means the Class A Shares Option Agreement between JV and S3 to be executed and delivered on the Closing Date, in the form attached hereto as Exhibit 1.

"Closing" has the meaning set forth in Section 2.1.

"Closing Balance Sheet" means the balance sheet of the Graphics Chip Business as of the Closing Date which shall be prepared in the same manner, and include the same classes of assets and liabilities as the February 27, 2000 Balance Sheet.

"Closing Date" has the meaning set forth in Section 2.1.

"Code" means the Internal Revenue Code of 1986, as amended.

"Consent" means any consent, approval, authorization, waiver, permit, grant, franchise, concession, agreement, license, exemption or order of, registration, certificate, declaration or filing with, or report or notice to, any Person, including but not limited to any Governmental Authority.

"Contracts" has the meaning set forth in Section 3.11(b).

"Contributed Assets" means the assets described in Schedule 3.10 along with such other assets as the Parties may mutually agree, together with the proceeds of all insurance on such assets plus an amount equal to any applicable deductible or retention amount in the event of a casualty.

"Contributed Intellectual Property" has the meaning set forth in Section 3.14(a).

"Control" (including, with correlative meanings, the terms "controlled by" and "under common control with"), when used with respect to any Person, means the possession, directly or indirectly, of the power to direct or cause the direction of the management and policies of such Person, whether through ownership of voting securities, by contract or otherwise.

"Encumbrance" means any mortgage, deed of trust, lien, pledge, easement, hypothecation, assignment, security interest or any other encumbrance or restriction of any type whatsoever.

"Environmental Law" means any federal, state, local or foreign law, statute, ordinance, rule, regulation, code, license, permit, authorization, approval, consent, legal doctrine, order, judgment, decree, injunction, requirement or agreement with any governmental entity relating to (x) the protection, preservation or restoration of the environment (including, without limitation, air, water vapor, surface water, groundwater, drinking water supply, surface land, subsurface land, plant and animal life or any other natural resource) or to human health or safety or (y) the exposure to, or the use, storage, recycling, treatment, generation, transportation, processing, handling, labeling, production, release or disposal of Hazardous Substances, in each case as amended and as in effect on the Closing Date.

"ERISA" means the Employee Retirement Income Security Act of 1974, as amended.

"Escrow Agreement" means the escrow agreement attached hereto as Exhibit 14.

"Escrow Assets" has the meaning set forth in Section 7.3.

"Exchange Act" means the Securities Exchange Act of 1934, as amended.

"Excluded Licenses" has been the meaning set forth in Section 3.11(b).

"February 27, 2000 Balance Sheet" means the balance sheet representing only the accounts that pertain to Graphics Chip Business prepared by S3, a copy of which is attached hereto as Schedule 3.5(c).

"Force Majeure" means: acts of God; earthquakes; fires; natural disasters; explosions; declared public states of emergency due to acts of public enemy, riots, civil commotion and insurrection; or any other similar catastrophic casualty, occurrence, condition, event or circumstance not reasonably within the excused Party's control and which could not have been anticipated and avoided by reasonable measures.

"GAAP" means generally accepted accounting principles as in effect in the United States applicable to the financial statements of a corporation with one or more classes of its securities registered under the Exchange Act.

"Governmental Approval" means any Consent of, with or to any Governmental Authority.

"Governmental Authority" means any nation or government, state or other political subdivision thereof, any entity exercising executive, legislative, judicial, regulatory or administrative functions of government, including, without limitation, any government authority, agency, department, board, commission or instrumentality of the United States or Taiwan, any State of the United States or any political subdivision thereof or of Taiwan and any tribunal or arbitrator(s) of competent jurisdiction, and any self-regulatory organization to which any such functions of government have been delegated in respect of such functions.

"Graphics Chip Business" shall mean S3's current business which involves the development, design, and manufacture of discrete graphics chips or discrete graphics chips integrated with core logic. Notwithstanding anything to the contrary herein, the Graphics Chip Business shall not include S3's board or add-in card business even though the products of such business contain graphics chips or provide graphics functionality to their users or S3's professional graphics business (e.g., the FireGL graphics board product line) which S3 conducts through its professional graphics divisions.

"Graphics Chip Business Assets" means the Contributed Assets, the Contributed Intellectual Property and any transferred Contracts.

"Guaranty" means that undertaking by VIA to be dated as of the Closing Date in the form attached hereto as Exhibit 10.

"Hazardous Substance" means any substance presently or hereafter listed, defined, designated or classified as hazardous, toxic, radioactive or dangerous, or otherwise regulated, under any Environmental Law. Hazardous Substance includes any substance to which exposure is regulated by any Government Authority or any Environmental Law including, without limitation, any toxic waste, pollutant, contaminant, hazardous substance, toxic substance, hazardous waste, special waste, industrial substance or petroleum or any derivative or by-product thereof, radon, radioactive material, asbestos or asbestos containing material, urea formaldehyde foam insulation, lead or polychlorinated biphenyls.

"HSR Act" means the Hart-Scott-Rodino Antitrust Improvements Act of 1976, as amended.

"Information" means all information (whether written or oral) furnished (whether before or after the date hereof) by any of the Parties or any of its Representatives to any other Party hereto or its Representatives and all analyses, compilations, forecasts, studies or other documents prepared by a Party or its Representatives in connection with its review of the transactions contemplated hereby which contain or reflect any such information, excluding information which (i) is or becomes publicly available other than as a result of disclosure by the receiving Party or its Representatives or (ii) is or becomes available to the receiving Party on a non-confidential basis from a source (other than a Party or its Representatives) which, to the best of the receiving Party's knowledge after due inquiry, is not prohibited from disclosing such information to the receiving Party by a legal, contractual or fiduciary obligation.

"Intel License" means the Intellectual Cross License Agreement, dated December 16, 1998, between Intel Corporation and S3.

"Intellectual Property" means any and all United States and foreign: (i) patents (including design patents, industrial designs and utility models) and patent applications (including docketed patent disclosures awaiting filing, reissues, divisions, continuations-in-part and extensions), patent disclosures awaiting filing determination, inventions and improvements thereto; (ii) trademarks, service marks, trade names, trade dress, logos, business and product names, slogans, and registrations and applications for registration thereof, together with the goodwill associated therewith and symbolized thereby; (iii) copyrights (including software) and

registrations thereof; (iv) inventions, processes, designs, formulae, trade secrets, know-how, industrial models, confidential and technical information, manufacturing, engineering and technical drawings, product specifications and confidential business information; (v) mask work and other semiconductor chip

rights and registrations thereof; (vi) intellectual property rights similar to any of the foregoing; and (vii) copies and tangible embodiments thereof (in whatever form or medium, including electronic media).

"Intellectual Property Assets" has the meaning set forth in Section 3.14(a).

"Intellectual Property Cross License Agreement" means the Cross License Agreement, to be dated as of the Closing Date, between S3 and JV in the form attached hereto as Exhibit 8.

"Intellectual Property Licenses" has the meaning set forth in Section 3.14(c).

"IRS" means the United States Internal Revenue Service.

"Joint Venture Agreement" means the Joint Venture Agreement, to be dated as of the Closing Date, between S3 and VIA in the form attached hereto as Exhibit 4.

"JV Transaction Agreements" means the Joint Venture Agreement, the Guaranty, the Non-Competition Agreement, the Intellectual Property Cross License Agreement, the Trademark License Agreement, the Class A Shares Option Agreement, the Release, the S3 Warrant and the Escrow Agreement.

"Leased Real Properties" means the premises located at 2841 Mission College Boulevard, Santa Clara, CA 95054, and any other premises which the parties mutually agree shall be subleased at the Closing.

"Leases" means the leases for the Leased Real Properties, pursuant to which S3 is the lessee.

"Management Agreement" means the Management Agreement of even date herewith between S3 and VIA in the form attached hereto as Exhibit 15.

"Material Adverse Effect" means a material adverse change in the value, condition or utility of the Graphics Chip Business Assets taken as a whole; provided, however, that the following shall not be taken into account in determining whether there has been or could or would be a "Material Adverse Effect:" (i) any change which occurs as a result of the announcement of this Agreement or the pendency of the transactions contemplated hereby, involving the loss of employees and customers, delay or cancellation of orders or the lack of or delay in availability of materials from suppliers, (ii) any change which occurs as a result of any action or failure to act by VIA pursuant to the Management Agreement (iii) any litigation brought or threatened against S3, VIA or JV, which does not result in the entry of injunctive relief, (iv) any action or order by the Government of Taiwan or any state or political subdivision thereof made or issued in connection with this Agreement or the transactions contemplated hereby (v) any change relating to the economy of the United States in general or the economies in which the Graphics Chip Business operates or the personal computer industry in general and not specifically related to the Graphics Chip Business, and (vi) any change that occurs as a result

of failure to sublease to JV the premises located at 2841 Mission College Boulevard, Santa Clara, California 95054. Without limiting the generality of the foregoing definition, termination of the Intel License prior to the Closing Date shall constitute a Material Adverse Effect.

"Monthly Financial Statements" has the meaning set forth in Section 5.15.

"Non-Competition Agreement" means the Non-Competition Agreement between S3 and JV, to be executed and delivered on the Closing Date, in the form

attached hereto as Exhibit 5.

"Parties" means S3 and VIA and JV (when it becomes a party hereto), and their respective successors and permitted assigns.

"Permitted Encumbrance" means (i) any Encumbrance for Taxes (other than income taxes) either not yet due and payable or being contested in good faith by appropriate proceedings and for which adequate reserves have been provided; (ii) mechanic's, materialmen's, workmen's, warehousemen's and other similar Encumbrances incurred in the ordinary course of business with respect to obligations which are not past due or which are being contested in good faith by appropriate proceedings and for which adequate reserves have been provided; (iii) a lien securing any Assumed Liability; and (iv) such liens, minor imperfections of title, easements on real property or leasehold estates as do not materially impair the value of the Graphics Chip Business Assets, the Excluded Licenses, or the operation of the Graphics Chip Business.

"Person" means an individual, corporation, partnership, limited liability company, trust, unincorporated organization or other entity or a government or any agency or political subdivision thereof.

"Release" means the Release in the form attached hereto as Exhibit 16.

"Representatives" means all of the directors, officers, employees, Affiliates and other representatives (including, without limitation, financial advisors, attorneys and accountants) or agents of a Person.

"S3 Subsidiaries" means S3 International Ltd., S3 Ventures, Ltd. and S3 -- VIA, Inc.

"S3 Warrant" shall mean that certain warrant to purchase 2,000,000 shares of S3 Common Stock at $10.00 per share, in the form attached hereto as Exhibit 9.

"Scheduled Closing Date" has the meaning set forth in Section 2.1.

"SEC" means the U.S. Securities and Exchange Commission.

"Securities Act" means the Securities Act of 1933.

"Subleases" means those subleases between S3, as sublessor, and JV, as sublessee, to be executed and delivered on the Closing Date with respect to the Leased Real Properties.

"Subsidiaries" means each corporation or other Person in which a Person owns or controls, directly or indirectly, capital stock or other equity interests representing at least 50% of the outstanding voting stock or other equity interests.

"Tax" or "Taxes" means (i) any and all federal, state, local and foreign taxes, assessments and other governmental charges, duties, impositions and liabilities relating to taxes, including taxes based upon or measured by gross receipts, income, profits, sales, use and occupation, and value added, ad valorem, transfer, franchise, withholding, payroll, recapture, employment, excise, stamp and property taxes and customs duties, (ii) all interest, penalties and additions imposed with respect to such amounts, and (iii) any obligations to any Tax authority or other Governmental Authority under Treasury Regulations 1.1502-6 (or any comparable provision of the laws of any state, local or foreign jurisdiction), or under any agreements or arrangements with any other Person, with respect to amounts described in clauses (i) and (ii), including any liability for Taxes of a predecessor entity.

"Tax Return" means any and all federal, state and local and foreign

returns, estimates, information statements and reports relating to Taxes.

"Third Party Claim" means any claim made by any third party which is to be the basis for a claim for indemnification hereunder.

"Trademark License Agreement" means the Trademark License Agreement between S3 and JV to be executed and delivered on the Closing Date, with respect to the S3 trademark, in the form attached hereto as Exhibit 11.

"Transfer," when used as a verb, means to sell, pledge, assign, encumber, dispose of or otherwise transfer, or, when used as a noun, means a sale, pledge, assignment, encumbrance, disposition, or other transfer.

"Transferred Employees" has the meaning set forth in Section 3.15.

ARTICLE 2.

ACTIONS TO BE TAKEN AT THE CLOSING

2.1 The Closing. The closing of the transactions provided for in this Article 2 (herein called the "Closing") shall take place at the offices of Heller Ehrman White & McAuliffe LLP, 525 University Avenue, Palo Alto, CA, at 2:00 p.m., local time, on January 3, 2001; provided, that (a) if the Closing has not occurred by January 3, 2001 and the delay is due to events (other than Force Majeure) not within the control of S3 or VIA, then the Closing shall take place on January 10, 2001, (b) if the Closing has not occurred by January 3, 2001 and the delay is due exclusively to an event constituting Force Majeure and arising from any act or failure to act by the government of Taiwan or any agency, committee or subdivision thereof, including, without limitation, any act, order or injunction against (or failure to approve, where such approval is legally required to accomplish) the transfer of funds or property pursuant to, or the consummation of any other action contemplated by, this Agreement, then the Closing shall take place as soon as practicable after the cessation of such event, but in no event later than January 17, 2001, or (c) if the Closing has not occurred by January 3, 2001 and the delay is due

exclusively to an event constituting Force Majeure of a type other than the type described in clause (b) above, then the Closing shall take place as soon as practicable after the cessation of such event, but in no event later than January 31, 2001. The date on which the Closing is to occur under this Section 2.1 is referred to in this Agreement as the "Scheduled Closing Date." The date on which the Closing actually occurs is referred to in this Agreement as the "Closing Date."

2.2 Actions at Closing. At the Closing, subject to the terms and conditions of this Agreement, the applicable Parties hereby agree to take the following actions in the following order, all of which shall be deemed to occur simultaneously:

(a) Concurrent with the Closing, the parties shall form JV and cause it to become a party to this Agreement.

(b) S3 and the S3 Subsidiaries shall transfer to JV all of their right, title and interest in and to the Contributed Assets, the Contributed Intellectual Property and the Contracts (to the extent such are assignable or consent to such assignment has been obtained).

(c) VIA, or its designee, shall deliver to JV $208,000,000 payable in cash or shares of S3 common stock or any linear combination thereof. For purposes of this Section 2.2(c), each share of S3 common stock shall be valued at $16.00.

(d) JV shall deliver to S3 $208,000,000 payable in the same form

contributed by VIA pursuant to Section 2.2(c).

(e) JV shall assume the Assumed Liabilities.

(f) JV shall deliver certificates representing 100,000,000 shares of JV Class A common stock to S3 or its designee.

(g) JV shall deliver certificates representing 30,000,000 shares of JV Class B common stock to VIA or its designee.

(h) JV shall deliver certificates representing 200,000 shares of JV Class C common stock to a person or entity to be identified by VIA.

(i) S3, VIA and JV shall each execute and deliver the JV Transaction Agreements to which each of them is a party.

(j) S3 shall deliver the Release.

2.3 Instruments of Conveyance and Transfer, etc. At the Closing, the applicable Parties will deliver the following documents:

(a) S3 will deliver to JV such bills of sale, endorsements, certificates and instruments of assignment, conveyance and transfer reasonably satisfactory in form and substance to JV as shall be necessary to vest in JV or any Subsidiary designated by JV good and marketable title to

the Contributed Assets, in each case, free and clear of any Encumbrances, except Permitted Encumbrances.

(b) If VIA, or its designee, delivers S3 shares pursuant to Section 2.2(c), VIA or its designee will deliver appropriate stock certificates representing such S3 shares registered in the name of JV or S3 stock certificates endorsed in blank or with standard blank stock powers affixed thereto free and clear of any Encumbrances, except Permitted Encumbrances.

(c) JV will deliver to S3 such instruments of assumption as shall be reasonably satisfactory in form and substance to the Parties as shall be necessary for JV to assume the Assumed Liabilities.

2.4 Further Assurances. If at any time at or after the Closing any Party shall consider or be advised that any further instruments of conveyance and transfer, assignments, assumptions or assurances in law or any other things are necessary, desirable or proper to vest, perfect or confirm in JV, of record or otherwise, the title to any assets, properties or rights acquired or to be acquired by reason of, or as a result of, the transfers to be effected at the Closing, or to vest, perfect or confirm in S3, of record or otherwise, the security interests and liens to be effected at Closing, or to perfect or confirm the assumption by JV of the liabilities or obligations to be assumed by it at the Closing, each of the Parties agrees to execute and deliver all such deeds, instruments, assignments, assumptions and assurances in law and to do all things necessary, desirable or proper to vest, perfect or confirm title to the applicable assets, properties or rights or to confirm the assumption of the applicable liabilities and otherwise to carry out the purposes of this Agreement.

2.5 Post-Closing Audit. Within two weeks after the Closing Date, S3 shall prepare and deliver the Closing Balance Sheet of the Graphics Chip Business. The Closing Balance Sheet shall be prepared in accordance with GAAP applied on a consistent basis and shall exclude any re-evaluation or re-adjustment as a result of the transactions contemplated by this Agreement. Promptly thereafter, JV shall cause the Closing Balance Sheet to be audited by a "Big Five" accounting firm other than Deloitte & Touche, LLP or Ernst & Young (the "Outside Auditor"). Within 60 days thereafter, the Outside Auditor shall

deliver an audited balance sheet, together with the notes thereto and the report of the Outside Auditor thereon, to VIA and S3. In the event that the net value of the accounts receivable, inventories and prepaid items relating to inventories contributed by S3 to JV, and the Assumed Liabilities (other than those additional liabilities assumed by VIA pursuant to Section 5.22), reflected in the audited balance sheet prepared in accordance with GAAP applied on a consistent basis varies by more than $500,000 from the net value of such assets and liabilities reflected on the Closing Balance Sheet prepared by S3, the entire excess, if any shall be paid to S3 by VIA and the entire deficiency, if any, shall be paid to JV by S3 within 48 hours of the determination of such excess or deficiency by the Outside Auditor.

ARTICLE 3.

REPRESENTATIONS AND WARRANTIES OF S3

S3 represents and warrants to VIA as follows:

3.1 Authorization, etc. S3 has the corporate power and authority to execute and deliver this Agreement and the JV Transaction Agreements to which it will be a party, to perform fully its obligations hereunder and thereunder, and to consummate the transactions contemplated hereby and thereby. The execution and delivery by S3 of this Agreement and the JV Transaction Agreements to which it will be a party, and the consummation of the transactions contemplated hereby and thereby, have been, and on the Closing Date the execution and delivery by S3 of this Agreement and the JV Transaction Agreements to which it will be a party and the consummation of the transactions contemplated hereby and thereby will have been, duly authorized by all requisite corporate action of S3. S3 has duly executed and delivered this Agreement, and on the Closing Date S3 will have duly executed and delivered the JV Transaction Agreements to which it will be a party. This Agreement is, and on the Closing Date each JV Transaction Agreement to which S3 is a party will be, legal, valid and binding obligations of S3, enforceable against it in accordance with its respective terms except as may be limited by bankruptcy, insolvency, reorganization and similar Applicable Laws affecting creditors generally and by the availability of equitable remedies. Neither the execution and delivery of this Agreement or the JV Transaction Agreements, nor the consummation of the transactions contemplated hereby or thereby, is required to be approved by the stockholders of S3. The factual assumptions recited by S3's counsel in the opinion attached hereto as Exhibit 13 are true and correct in all material respects.

3.2 Corporate Status.

(a) S3 and the S3 Subsidiaries are corporations duly organized, validly existing and in good standing under the laws of the jurisdiction of their incorporation with full corporate power and authority to carry on the Graphics Chip Business and to own or lease and to operate the properties necessary to the operation of the Graphics Chip Business as and in the places where such business is conducted and such properties are owned, leased or operated.

(b) S3 and the S3 Subsidiaries are duly qualified or licensed to do business in each of the jurisdictions in which the operation of the Graphics Chip Business or the character of the properties owned, leased or operated by it in connection with the Graphics Chip Business makes such qualification or licensing necessary, and where the failure to do so would not have a Material Adverse Effect.

(c) S3 has delivered to VIA complete and correct copies of the certificate of incorporation and by-laws or other organizational documents of S3 and each of its Subsidiaries, in each case as amended and in effect on the date hereof. Neither S3 nor the S3 Subsidiaries are in violation of any of the provisions of its certificate of incorporation or by-laws or other organizational documents.

(d) To S3's knowledge, S3 is not in violation of any order of any Governmental Authority or any Applicable Law to which S3 or the S3 Subsidiaries or any of their properties or assets utilized primarily in the Graphics Chip Business are subject. To S3's knowledge, S3 has obtained all licenses, permits and other authorizations and has taken all action required by Applicable Law in connection with the Graphics Chip Business as now conducted.

3.3 Employee Options. Stock options granted by S3 pursuant to S3's 1989 Stock Option Plan (the "S3 Option Plan") are referred to in this Agreement as "S3 Stock Options." Schedule 3.3, as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.3"), sets forth the following information with respect to each S3 Stock Option outstanding as of the date of this Agreement: (i) the name of the optionee; (ii) the particular plan pursuant to which such S3 Stock Option was granted; (iii) the number of shares of common stock subject to such S3 Stock Option; (iv) the exercise price of such S3 Stock Option; (v) the vesting schedule of such S3 Stock Option and whether such vesting accelerates on a change of control of S3, as defined in S3 Option Plan; (vi) the date on which such S3 Stock Option was granted; and (vii) the date on which such S3 Stock Option expires. S3 has made available to VIA accurate and complete copies of the S3 Option Plan and the forms of all agreements evidencing S3 Stock Options. All shares of common stock subject to issuance as aforesaid, upon issuance on the terms and conditions specified in the instrument pursuant to which they are issuable, would be duly authorized, validly issued, fully paid and nonassessable. Except as designated in Schedule 3.3, there are no commitments or agreements of any character to which S3 is bound obligating S3 to accelerate the vesting of any S3 Stock Option as a result of the transactions contemplated by this Agreement.

3.4 No Conflicts, etc. The execution, delivery and performance by S3 of this Agreement and each JV Transaction Agreement to which it is a party, and the consummation of the transactions contemplated hereby and thereby, do not, except as would not materially impair the ability of S3 to perform obligations hereunder and under the JV Transaction Agreements, conflict with or result in a violation of or a default under (with or without the giving of notice or the lapse of time or both), create in any other Person a right or claim of termination, amendment, modification (including without limitation the commencement of any royalty or other payment obligation on behalf of S3), acceleration or cancellation of, or result in the creation of any Encumbrance (or any obligation to create any Encumbrance) upon any of the Graphics Chip Business Assets under, (i) any Applicable Law applicable to S3 or the Graphics Chip Business Assets, (ii) the certificate of incorporation or by-laws or other organizational documents of S3 and the S3 Subsidiaries, or (iii) except as set forth in Schedule 3.4, any contract, agreement, intellectual property license or instrument to which S3 or the S3 Subsidiaries may be bound or affected and which is included or used in the Graphics Chip Business or the Graphics Chip Business Assets to be transferred to JV. Except as specified in Schedule 3.4, to S3's knowledge, no Governmental Approval or other Consent of any party is required to be obtained or made by S3 in connection with the execution and delivery of this Agreement or the JV Transaction Agreements or the consummation of the transactions contemplated hereby or thereby.

3.5 S3 Financial Statements.

(a) Each of the consolidated financial statements (including, in each case, any related notes thereto) for the last three fiscal years delivered to VIA (the "S3 Financials"), (i) was

prepared in accordance with GAAP applied on a consistent basis throughout the periods involved (except as may be indicated in the notes thereto) and (ii) fairly presented the consolidated financial condition of S3 and its Subsidiaries as at the respective dates thereof and the consolidated results of S3's operations and cash flows for the periods indicated.

(b) The historical audited financial statements of the Graphics Chip Business, when prepared and delivered to JV pursuant to Section 5.14, shall be true and correct as of the date thereof, be prepared in accordance with GAAP applied on a consistent basis and fairly present the financial condition of the Graphics Chip Business as at December 31, 1999, 1998 and 1997 and the results of its operations and its cash flow for the years then ended.

(c) The February 27, 2000 Balance Sheet when prepared and delivered to VIA is true and correct in all material respects as of the date thereof, was prepared in accordance with GAAP applied on a consistent basis and fairly presents the financial condition of the Graphics Chip Business as of the date thereof.

(d) The Closing Balance Sheet, when prepared and delivered to VIA, shall be true and correct in all material respects, be prepared in accordance with GAAP applied on a consistent basis and fairly presents the Graphics Chip Business Assets and the Additional Capital Assets as of the date thereof.

3.6 Taxes.

(a) S3 and the S3 Subsidiaries have timely filed all material Tax Returns required to be filed by them, which Tax Returns are true, correct and complete in all significant respects, and have paid (or S3 has paid on behalf of the S3 Subsidiaries) all Taxes required to be paid as shown on such Tax Returns.

(b) Except for Taxes described on Schedule 3.6, S3 has paid all Taxes assessed or asserted to be due by any Governmental Authority.

(c) There is no Encumbrance for Taxes upon any Graphics Chip Business Asset, other than liens for Taxes not yet due and payable.

(d) S3 has provided to VIA correct and complete copies of all notices and communications from any Governmental Authorities related to Taxes of or on the Graphics Chip Business, the Graphics Chip Business Assets, the Contributed Intellectual Property, and the Contracts.

(e) Except as provided to VIA in writing, there are no Tax-allocation, Tax-sharing or indemnification agreements related to or binding on the Graphics Chip Business or the Graphics Chip Business Assets.

(f) Except as provided to VIA in writing, there is no contract, agreement, plan or arrangement covering any employee of the Graphics Chip Business that could give rise to the payment of any amount that would not be deductible under Section 280G, 404, or 162(m) of the Code.

3.7 Litigation. Except as set forth in Schedule 3.7, as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.7"), to S3's knowledge, there is no action, claim, demand, suit, proceeding, arbitration, grievance, citation, summons, subpoena, inquiry or investigation of any nature, civil, criminal, regulatory or otherwise, in law or in equity, pending against or relating to the Graphics Chip Business Assets, the Excluded Licenses, or the Graphics Chip Business, or against or relating to the transactions contemplated by this Agreement or the JV Transaction Agreements. Neither VIA nor JV shall assume S3's obligations under any ongoing litigation, whether or not related to the Graphics Chip Business. Except as set forth in such Schedule 3.7, to the knowledge of S3, no liability under any citations, fines or penalties has been asserted against S3 or the S3 Subsidiaries since January 1, 1995 under any

Environmental Law with respect to the Leased Real Properties. Neither S3 nor the S3 Subsidiaries nor any of the Graphics Chip Business Assets are subject, or in default under any order, writ, judgment, injunction or decree of any court, tribunal, arbitration panel or any government department, commission, board, agency or instrumentality, domestic or foreign with respect to the Graphics Chip Business.

3.8 Compliance with Laws; Governmental Approvals and Consents. Except as disclosed in Schedule 3.8, to the knowledge of S3, the Graphics Chip Business Assets are being used and operated in compliance with Applicable Law applicable to the Graphics Chip Business.

3.9 Operation of the Graphics Chip Business. Except as disclosed in Schedule 3.9, S3 has conducted the Graphics Chip Business only through S3 and the S3 Subsidiaries and not through any other divisions or any other Affiliate of S3.

3.10 Graphics Chip Business Assets. Schedule 3.10, sets forth a true and complete list of all of the assets held by or used in the Graphics Chip Business designated by S3 and VIA to be contributed on the Closing Date to JV (the "Contributed Assets"). On the Closing Date, S3 and the S3 Subsidiaries will have good title to or a valid leasehold interest in or license to all of the assets comprising the Graphics Chip Business Assets, including, without limitation, the Contributed Assets, the Leased Real Property, and the Contributed Intellectual Property, in each case free and clear of any and all Encumbrances other than Permitted Encumbrances. Except for the Graphics Chip Business Assets, the Intellectual Property Assets and the Intellectual Property Licenses, there are no material assets or properties used in the operation of the Graphics Chip Business as currently conducted. Except as set forth herein and as disclosed to VIA during due diligence, S3 has no knowledge of any facts, events or circumstances relating to or affecting the Graphics Chip Business, the Graphics Chip Business Assets, or the Excluded Licenses which has since February 27, 2000 or could, individually or in the aggregate, result in a Material Adverse Effect. Except as disclosed to VIA during due diligence, the tangible personal property assets used in the Graphics Chip Business are in good repair and operating condition (subject to normal wear and tear).

3.11 Contracts.

(a) Schedule 3.11(a) as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.11(a)") and Schedules 3.14(c)(i), as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.14(c)(i)"), and Schedule 3.14(c)(ii) contain a complete and correct list of all agreements and contracts (whether written or oral) of the types described below relating to the

Graphics Chip Business, to which S3 or the S3 Subsidiaries are a party and are bound or materially affected or to which S3 or the S3 Subsidiaries are a party or by which they are bound in connection with the Graphics Chip Business:

(i) employment contracts concerning Transferred Employees, whether written or oral, consulting agency, collective bargaining or other similar contracts and agreements under which current or future obligations exist relating to or for the benefit of Transferred Employees;

(ii) asset purchase agreements and other acquisition or divestiture agreements (other than agreements for sales of inventory in the ordinary course of business) and any agreements relating to the sale, lease or disposal of any capital assets in the amount of $100,000 or more;

(iii) brokerage or finder's agreements;

(iv) orders and other contracts for the purchase or sale of materials, supplies, products or services under which current or future obligations exist, including (i) the names and addresses of all suppliers from which S3 ordered raw materials, supplies, merchandise and other goods and services with an aggregate purchase price for each such supplier of $100,000 or more during the twelve-month period ended December 31, 1999 and the amount for which each supplier invoiced S3 during such period and (ii) the names and addresses of all customers of S3 that ordered goods and services of $100,000 or more during the twelve-month period ended December 31, 1999 and the amount for which each such customer was invoiced during such period;

(v) lease agreements providing for the leasing of personal property primarily used in, or held for use primarily in connection with, the Graphics Chip Business; and

(vi) any other contracts, agreements or commitments that are material to the Graphics Chip Business.

(b) Schedule 3.11(b)(i) as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.11(b)(i)") sets forth a list of the contracts and agreements which have been designated by S3 for assignment to JV on the Closing Date (the "Contracts"). A number of these Contracts require third party consents for assignment. Within 30 days after the Closing Date, JV shall designate which of the Contracts it wishes to have assigned to JV; provided, however, that JV shall accept assignment of the Contracts specified in Schedule 3.11(b)(i) with an asterisk (*). Schedule 3.11(b)(ii) (hereafter "Schedule 3.11(b)(ii)"), sets forth a list of certain of the contracts, licenses and agreements which have not been designated for assignment to JV on the Closing Date (the "Excluded Licenses") and which are related to the Graphics Chip Business. While S3 shall undertake good faith efforts to request and obtain any consents necessary to such assignments, there can be no assurance that such consents can be obtained or that it will be able to assign any or all of the Contracts that require such consent. S3 shall undertake commercially reasonable efforts to maintain the Excluded Licenses in full force and effect; provided, however,

that subject to Section 5.6, nothing herein shall limit or affect S3's right to enter into a merger or other similar transaction or to modify or amend said Excluded Licenses in a manner that S3 believes is in the best interests of its stockholders.

(c) S3 has made available to VIA complete and correct copies of all written Contracts, together with all amendments thereto, and accurate descriptions of all material terms of all oral Contracts, set forth or required to be set forth in Schedules 3.11(a) and 3.11(b)(i).

(d) Except where the failure would result in a Material Adverse Effect, all Contracts are in full force and effect and enforceable against S3 and the S3 Subsidiaries, and against each other party thereto. No party has declared an event of default under any Contract, and no such event or condition exists that, after notice or lapse of time or both, would constitute a violation, breach or event of default thereunder on the part of S3 or to the knowledge of S3, any other party thereto except as set forth in Schedule 3.11(d). To S3's knowledge, there is no fact, event or circumstance that will materially impair the ability of S3 to perform its obligations under this Agreement and the JV Transaction Agreements.

(e) Except as set forth in Schedule 3.11(e), S3 does not have outstanding any power of attorney that relates to the operation of the Graphics Chip Business or the Graphics Chip Business Assets.

3.12 Territorial Restrictions. Except as set forth in Schedule 3.12, neither S3 nor the S3 Subsidiaries is a party to any agreement placing a

territorial restriction on the use of the Graphics Chip Business Assets.

3.13 Inventories.

(a) All of the inventories of raw materials, supplies, work in process, finished products, spare parts, replacement and component parts included in the Contributed Assets are of good, usable and merchantable quality in all material respects and except as set forth in Schedule 3.13, as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.13"), do not include obsolete or discontinued items.

(b) All such inventories are of such quality as to meet the quality control standards of S3 and any applicable governmental quality control standards.

(c) All such inventories that are finished goods are saleable as current inventories at the current prices thereof in the ordinary course of business.

(d) All such inventories are recorded on the books of S3 at the lower of cost or market value determined in accordance with GAAP.

(e) Schedule 3.13 lists the locations of all such inventories.

3.14 Intellectual Property.

(a) Title. Schedule 3.14(a)(i) sets forth a list of all the Intellectual Property that is related to, used in or held for use in connection with, or is material to the operation of, the

Graphics Chip Business (the "Intellectual Property Assets"). Schedule 3.14(a)(ii), sets forth the Intellectual Property Assets which are owned by S3 and which S3 will Transfer to JV on the Closing Date (the "Contributed Intellectual Property"). Except as disclosed on Schedules 3.14(a)(i), (ii) to S3's knowledge, the Intellectual Property Assets are free and clear of all Encumbrances except Permitted Encumbrances.

(b) No Infringement. To the knowledge of S3, neither the conduct nor products of the Graphics Chip Business nor the Graphics Chip Business Assets infringe or otherwise conflict with any rights of any Person, none of the Graphics Chip Business Assets is being infringed by any Person, and there is no patent or patent application or trademark or trademark application that interferes with the Graphics Chip Business Assets or has a Material Adverse Effect.

(c) Licensing Arrangements. Schedule 3.14(c)(i) designates all agreements or contracts pursuant to which any other Person has licensed or sublicensed to S3 or the S3 Subsidiaries any Intellectual Property Assets, or otherwise knowingly permitted S3's or the S3 Subsidiaries' use of such Intellectual Property Assets (through non-assertion, settlement or similar agreements relating to the Graphics Chips Business) (the "Intellectual Property Licenses"). Schedule 3.14(c)(ii) designates all agreements or arrangements pursuant to which S3 or the S3 Subsidiaries have licensed or sublicensed to any other Person any Intellectual Property Assets relating to the Graphics Chips Business, or otherwise knowingly permitted such Person's use of such Intellectual Property Assets relating to the Graphics Chips Business (through non-assertion, settlement or similar agreements). Except as set forth in such Schedules 3.14(c)(i), as amended by the Additional Disclosure Schedules (hereafter "Schedule 3.14(c)(i)"), and 3.14(c)(ii), to the knowledge of S3, the Intellectual Property Licenses relating to the Graphics Chips Business (x) are in full force and effect in accordance with their terms and no default exists thereunder by S3 or its Subsidiaries or to the knowledge of S3, by any other party thereto, and (y) are free and clear of all Encumbrances. S3 or the S3 Subsidiaries have made available to VIA true and complete copies of all

Intellectual Property Licenses relating to the Graphics Chips Business (including amendments, supplements, renewals, waivers and other modifications), which are set forth on such Schedules 3.14(c)(i) and 3.14(c)(ii).

(d) No Intellectual Property Litigation. To the knowledge of S3, there are no claims that any default exists under any agreement or arrangement pertaining to the Contributed Intellectual Property, or the Excluded Licenses except as set forth on Schedule 3.7, as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.7"). Except as set forth on such Schedule 3.7, none of the Contributed Intellectual Property, or the Excluded Licenses is subject to any outstanding order, ruling, decree, judgment or stipulation by or with any court, arbitrator, or administrative agency.

(e) Due Registration, etc. To S3's knowledge, S3 has taken all such necessary or desirable actions to ensure that the patents and trademarks owned by S3 and included in the Contributed Intellectual Property or to be subject to the Intellectual Property Cross License Agreement have been duly registered under any Applicable Laws in the appropriate filing offices, and, to S3's knowledge, such registrations were issued on the basis of applications that were true and correct as of their dates, and are in full force and effect.

(f) Protection of Intellectual Property. Exhibit 12, as amended by the Additional Disclosure Schedule (hereafter "Exhibit 12"), sets forth a true and complete list of all employees and consultants of S3's Graphics Chip Business who are bound by a form of proprietary rights and information agreement with S3 (the "Proprietary Rights and Information Agreement"). It has been S3's policy and practice to obtain a Proprietary Rights and Information Agreement from each employee and consultant of the Graphics Chip Business during the thirty-six (36) months prior to this Agreement. S3 has delivered to VIA complete and correct copies of such Proprietary Rights and Information Agreements. To the knowledge of S3, none of such confidential proprietary rights have been used, distributed or otherwise commercially exploited under circumstances which have caused the loss of any patent, trademark, copyright or trade secret used in the Graphics Chip Business.

3.15 Employees, Labor Matters, etc. Schedule 3.15, as amended by the Additional Disclosure Schedule (hereafter "Schedule 3.15"), which shall be CONFIDENTIAL and sealed, sets forth the following information with respect to each person designated by S3 and VIA as an employee to be transferred to JV on or immediately after the Closing Date (the "Transferred Employees"): (i) the name of the employee; (ii) the position of the employee; (iii) the compensation rate of the employee; and (iv) any obligation of S3 or the S3 Subsidiaries to pay or compensate any of said employees for bonuses, retention or sick or other paid time off. Except as set forth in Schedule 3.15, S3 is not a party to or bound by any collective bargaining agreement and there are no labor unions or other organizations representing, purporting to represent or attempting to represent any Transferred Employee. Since January 1, 1995, there has not occurred or been threatened any material strike, slowdown, picketing, work stoppage, concerted refusal to work overtime or other similar labor activity with respect to any employees employed by S3 in connection with the Graphics Chip Business. To S3's knowledge, there are no material labor disputes currently subject to any grievance procedure, arbitration or litigation and there is no representation petition pending or threatened with respect to any Transferred Employee other than those listed on such Schedule 3.15. To its knowledge, S3 has not received any written notice of, or is otherwise aware of, any federal, foreign, state or local administrative proceeding (excluding workers compensation proceedings) with respect to any Transferred Employee.

3.16 Rebates. Except as listed on Schedule 3.16, S3 has not entered into, or offered to enter into, any agreement, contract, commitment or other arrangement (whether written or oral) pursuant to which S3 is obligated, with respect to the Graphics Chip Business Assets, to make any rebates, discounts, promotional allowances or similar payments or arrangements, including without

limitation returns of S3 Graphics Chip Business products or merchandise, with the ten largest customers of S3 (based on 1999 purchases) ("Rebate Obligations"). Neither S3 nor JV shall, without their respective consent, assume any liability for any other rebates. All Rebate Obligations are reflected in the S3's historical financial statements and in the February 27, 2000 Balance Sheet, and will be reflected in the Closing Balance Sheet.

3.17 Brokers, Finders, etc. All negotiations relating to this Agreement and the JV Transaction Agreements, and the transactions contemplated hereby and thereby, have been carried on without the participation of any Person acting on behalf of S3 or Affiliates of S3 in such manner as to give rise to any valid claim against VIA for any brokerage or finder's commission, fee or similar compensation, or for any bonus payable by VIA to any officer,

director, employee, agent or sales representative of or consultant to S3 upon consummation of the transactions contemplated hereby or thereby.

3.18 Real Property.

(a) Leases. S3 has made available to VIA correct and complete copies of the Leases. The Leases are legal, valid, binding, enforceable, and in full force and effect, except as may be limited by bankruptcy, insolvency, reorganization and similar Applicable Laws affecting creditors generally and by the availability of equitable remedies. To the knowledge of S3, no party is in default, violation or breach in any material respect under the Leases, and no event has occurred and is continuing that constitutes or, with notice or the lapse of time or both, would constitute a default, violation or breach in any respect under the Leases. Each Lease grants the tenant under the Lease the exclusive right to use and occupy the premises demised thereunder. Either S3 or the S3 Subsidiaries enjoy peaceful and undisturbed possession under the Leases for the Leased Real Properties.

(b) No Proceedings. To S3's knowledge, there are no eminent domain or other similar proceedings pending or affecting any portion of any of the Leased Real Properties. There is no writ, injunction, decree, order or judgment outstanding, nor any action, claim, suit or proceeding, pending or, to the knowledge of S3, threatened, relating to the ownership, lease, use, occupancy or operation by any Person of any of the Leased Real Properties.

3.19 Environmental Matters.

(a) Except as set forth on Schedule 3.19(a), with respect to the Graphics Chip Business Assets and the Leased Real Property, S3 is and on the Closing Date will be in compliance in all material respects with all applicable Environmental Laws, except for violations that would not individually or in the aggregate have a Material Adverse Effect. To the knowledge of S3, there is no pending civil or criminal litigation, notice of violation or non-compliance of administrative proceedings relating to Environmental Laws involving S3 or the S3 Subsidiaries other than litigation, notices of violation, or administrative proceedings which would not reasonably be expected, if adversely decided, to have individually or in the aggregate a Material Adverse Effect.

(b) Except as set forth on Schedule 3.19(b), neither S3 nor the S3 Subsidiaries have received any notice, nor does S3 have knowledge of (i) any violation of or non-compliance with any Environmental Law or any other law, statute, rule, or regulation regarding Hazardous Substances on, at, under or associated with the Leased Real Property or (ii) the actual institution or pendency of any suit, action, claim, proceeding or investigation by any Governmental Authority relating to or associated with any Leased Real Property or (iii) any actual or threatened request or demand by any Governmental Authority or third party for or relating to the investigation or removal of Hazardous Substances from any Leased Real Property or any part thereof other than violations, suits, actions, claims, proceedings, investigations or requests

which could not, individually or in the aggregate, reasonably be expected to have a Material Adverse Effect.

(c) To the knowledge of S3, there is no condition existing on or associated with the Graphics Chip Business Assets or any Leased Real Property which could reasonably be expected to give rise to the assertion of a claim, relating to or associated with any release of Hazardous Substances or other materials on, at, under or from the Graphics Chip Business Assets or any Leased Real Property by any private individuals or Governmental Authority for cleanup of such Hazardous Substances or materials or for damages associated therewith including for alleged exposure thereto, including, but not limited to, claims involving allegations of personal injury and/or property damage.

3.20 Accounts Receivable. Schedule 3.20, sets forth a true and complete list of all accounts receivable of the Graphics Chip Business as of the date hereof, along with an "aging" of all such accounts. At the Closing Date, all of the accounts receivable included in the Graphics Chip Business Assets will be (i) valid and binding obligations of the party owing thereunder, (ii) current in accordance with their payment terms and not older than 60 days from the date of original invoice, and (iii) to S3's knowledge, not subject to setoff or equitable defenses against S3 or other assignors. Except as set forth in Schedule 3.20, S3 has no knowledge that any of the accounts receivable are uncollectible.

3.21 Purchase for Investment. S3 or its designee is acquiring the shares of JV Class A common stock solely for investment, with no present intention to resell such shares. S3 hereby acknowledges that the shares of JV Class A common stock have not been registered pursuant to Applicable Law and may not be transferred in the absence of such registration or an exemption therefrom, and that the stock certificates representing the shares issued to S3 will bear a restrictive legend to the foregoing effect.

3.22 Disclosure. To the knowledge of S3, no representation or warranty by S3 contained in this Agreement nor any statement or certificate furnished or to be furnished by or on behalf of S3 to VIA or its representatives in connection herewith (other than the Monthly Financial Statements) or pursuant hereto contains any untrue statement of a material fact, or omits or will omit to state any material fact required to make the statements contained herein or therein not misleading. S3 has provided VIA with all material information relating to the Graphics Chip Business Assets, the Excluded Licenses, and the Intellectual Property Assets subject to the Intellectual Property Cross License Agreement, and the operation of the Graphics Chip Business.

ARTICLE 4.

REPRESENTATIONS AND WARRANTIES OF VIA

VIA represents and warrants to S3 as follows:

4.1 Authorization, etc.

(a) VIA has the corporate power and authority to execute and deliver the JV Transaction Agreements to which it will be a party, to perform fully its obligations thereunder, and to consummate the transactions contemplated thereby. The execution and delivery by VIA of this Agreement and the consummation of the transactions contemplated hereby have been, and

on the Closing Date the execution and delivery by VIA of the JV Transaction

Agreements to which it will be a party and the consummation of the transactions contemplated thereby will have been, duly authorized by all requisite corporate action of VIA. VIA has duly executed and delivered this Agreement and on the Closing Date will have duly executed and delivered the other JV Transaction Agreements to which it will be a party. This Agreement is, and on the Closing Date each JV Transaction Agreement to which VIA is a party will be, a legal, valid and binding obligation of VIA enforceable against it in accordance with its respective terms, except as may be limited by bankruptcy, insolvency, reorganization and similar Applicable Laws affecting creditors generally and by the availability of equitable remedies. Neither the execution and delivery of this Agreement or the JV Transaction Agreements, nor the consummation of the transactions contemplated hereby or thereby, is required to be approved by the stockholders of S3. The factual assumptions recited by S3's counsel in the opinion attached hereto as Exhibit 13 are true and correct in all material respects.

(b) VIA is a corporation duly organized, validly existing and in good standing under the laws of the jurisdiction of its incorporation, with full corporate power and authority to carry on its businesses.

4.2 No Conflicts, etc. The execution, delivery and performance by VIA of this Agreement and each JV Transaction Agreement and the Guaranty to which it is a party, and the consummation of the transactions contemplated hereby and thereby, do not and will not conflict with or result in a violation of or a default under (with or without the giving of notice or the lapse of time or both), create in any other Person a right or claim of termination, amendment, modification, acceleration or cancellation of, or result in the creation of any Encumbrance (or any obligation to create any Encumbrance) upon any of the properties or assets of VIA under (i) any Applicable Law, applicable to VIA or any of the properties or assets of VIA, (ii) the certificate of incorporation or by-laws or other organizational documents of VIA or (iii) except as set forth in Schedule 4.2, any contract, agreement or other instrument to which VIA is a party or by which VIA or any of its properties or assets may be bound or affected (except, in the case of clause (iii) for violations or defaults that, individually and in the aggregate, would not have a material adverse effect on the properties, businesses, or results of operations of VIA as currently conducted and would not materially impair the ability of VIA to perform its obligations hereunder and under the JV Transaction Agreements and the Guaranty to which it is a party). Except for approvals under the HSR Act, no Governmental Approval, or other Consent of any party is required to be obtained or made by VIA in connection with the execution and delivery of this Agreement or the JV Transaction Agreements or the Guaranty or the consummation of the transactions contemplated hereby or thereby.

4.3 Brokers, Finders, etc. All negotiations relating to this Agreement, the other JV Transaction Agreements and the transactions contemplated hereby and thereby have been carried on without the participation of any Person acting on behalf of VIA or Affiliates of VIA in such manner as to give rise to any valid claim against S3 for any broker's or finder's or similar fee or commission.

4.4 Purchase for Investment. VIA or its designee is acquiring the shares of JV Class B common stock, and the S3 Warrant solely for investment, with no present intention to resell such shares or warrant. VIA understands and represents that the person or entity to be

identified by VIA as the recipient of the JV Class C common stock will hold said shares solely for investment and has no present intention to resell such shares. VIA hereby acknowledges that the shares of JV Class B common stock, JV Class C common stock and the S3 common stock underlying the S3 Warrant have not been registered pursuant to Applicable Law and may not be transferred in the absence of such registration or an exemption therefrom, and that the stock certificates representing the shares issued to VIA will bear a restrictive legend to the foregoing effect.

4.5 Disclosure. To the knowledge of VIA, no representation or warranty by VIA contained in this Agreement nor any statement or certificate furnished or to be furnished by or on behalf of VIA to S3 or its representatives in connection herewith or pursuant hereto contains or will contain any untrue statement of a material fact, or omits or will omit to state any material fact required to make the statements contained herein or therein not misleading.

ARTICLE 5.

COVENANTS

5.1 Access and Information. From the date hereof until the earlier of the Closing Date or the termination of this Agreement in accordance with the terms hereof, S3 and Persons acting on its behalf will (and its respective accountants, counsel, consultants, employees and agents will) give VIA, its accountants, counsel, consultants, employees and agents, full access (except as to privileged communications) during normal business hours to, and furnish them with all documents, records, work papers and information with respect to, all of the Graphics Chip Business Assets and the properties, assets, books, contracts, commitments, reports and records relating to S3's Graphics Chip Business, as VIA shall from time to time reasonably request. In addition, S3 and Persons acting on its behalf will permit VIA, and its accountants, counsel, consultants, employees and agents, reasonable access (except as to privileged communications) to such personnel of S3's Graphics Chip Business and Persons acting on its behalf during normal business hours as may be necessary or useful to VIA in its review of the Graphics Chip Business Assets and business affairs of S3's Graphics Chip Business and the above-mentioned documents, records and information. S3 will keep VIA reasonably informed as to the affairs of S3's Graphics Chip Business through meetings conducted at least every two weeks from the date hereof to the Closing Date.

5.2 Confidentiality. It is hereby agreed that, except as otherwise expressly provided herein:

(a) Each Party and its Representatives (i) will keep all Information confidential and will not (except as required by Applicable Law, regulation or legal process, and only after compliance with paragraph (c) below), without the prior written consent of the affected Parties hereto, disclose any Information in any manner whatsoever, and (ii) will not use any Information other than in connection with the transactions contemplated hereby; provided, however, that a Party may reveal the Information to its Representatives (x) who need to know the Information for the purpose of evaluating the transactions contemplated hereby, (y) who are informed by such Party of the confidential nature of the Information and (z) who agree to act in accordance

with the terms hereof. Each Party will cause its Representatives to observe the terms hereof and will be responsible for any breach hereof by any of its Representatives.

(b) Each Party and its Representatives will not (except as required by Applicable Law or stock exchange regulation, and only after compliance with paragraph (c) below), without the prior written consent of the affected Parties, disclose to any Person the fact that the Information exists or has been made available, that such Party is considering the transactions contemplated hereby or any other similar transactions or that discussions or negotiations are taking or have taken place concerning the transactions contemplated hereby or any term, condition or other fact relating to the transactions contemplated hereby or such discussions or negotiations, including, without limitation, the status thereof.

(c) In the event that a Party or its Representatives is requested pursuant to, or required by, Applicable Law to disclose any of the Information to a third party, it will notify the other Parties hereto who are affected

thereby promptly so that they may seek a protective order or other appropriate remedy or, in their sole discretion, waive compliance with the terms hereof. In the event that no such protective order or other remedy is obtained, or that such Party waives compliance with the terms hereof, the other Party will furnish only that portion of the Information which it is advised by counsel is legally required and will exercise all reasonable efforts to obtain reliable assurance that confidential treatment will be accorded the Information.

(d) If this Agreement is terminated, at any time thereafter upon the request of a Party or any of its Representatives, the other Parties will either (i) promptly destroy all copies of the written Information in their or their Representatives' possession and confirm such destruction to the requesting Party in writing or (ii) promptly deliver to the requesting Party, at its expense, all copies of the written Information in its or its Representatives' possession. Any oral Information will continue to be subject to the terms hereof.

5.3 Public Announcements. Except as required by Applicable Law or stock exchange regulation applicable to the Parties, the Parties shall not, and shall not permit any Person acting on their behalf to, make any public announcement in respect of this Agreement or the transactions contemplated hereby without the prior written consent of the other Party.

5.4 Conduct of Graphics Chip Business. On and after the date hereof and until the Closing Date, except as expressly permitted or required by this Agreement or as otherwise expressly permitted by VIA in writing (after the date hereof), S3 and each of the S3 Subsidiaries will, with respect to the Graphics Chip Business, make commercially reasonable efforts to:

(a) carry on the Graphics Chip Business in the ordinary course and in substantially the same manner as heretofore conducted;

(b) preserve intact its present business organization, maintain its properties in good operating condition and repair, and preserve its relationship with customers, suppliers and others having business dealings with it;

(c) not terminate, other than for cause, the Transferred Employees;

(d) not delay payment of any trade payables or other obligations other than in the ordinary course of business;

(e) maintain all of the Graphics Chip Business Assets in good repair, working order and operating condition subject only to ordinary wear and tear;

(f) keep in full force and effect insurance comparable in amount and scope of coverage to insurance now carried by it in connection with the Graphics Chip Business;

(g) maintain its books of account and records of its business in the usual, regular and ordinary manner consistent with past policies and practice, and not change such policies or practices;

(h) comply in all material respects with all Applicable Laws applicable to the Graphics Chip Business;

(i) not make any material Tax elections with respect to the Graphics Chip Business that would be binding on JV or VIA after the Closing Date;

(j) maintain its good standing in its jurisdiction of incorporation and in the jurisdictions in which it is qualified to do and does operate its Graphics Chip Business as a foreign corporation and to maintain or obtain all Governmental Approvals and other Consents necessary for, or otherwise material to, the Graphics Chip Business;

(k) promptly advise VIA in writing of any event, circumstance, occurrence, fact, condition, change, development or effect that, individually or in the aggregate, could, to the knowledge of S3, reasonably be expected to have or result in a Material Adverse Effect or would cause a breach of this Section 5.4;

(l) perform in all material respects all of its obligations under all Contracts;

(m) not enter into any agreement, commitment or other transaction in connection with or relating to the Graphics Chip Business or make any capital expenditures or capital additions or improvements for or in the Graphics Chip Business or amend, modify or terminate any existing Contract entered into in connection with or relating to the Graphics Chip Business other than in the ordinary course of business and involving an expenditure of less than $100,000 (other than purchases of goods in the ordinary course of business), or enter into any agreement or commitment in connection with or relating to the Graphics Chip Business that, pursuant to its terms, is not cancelable without penalty on notice of 30 days' or less from the end of the first month following the Closing Date; provided, however, that S3 may purchase capital equipment or assets which would otherwise require VIA's consent pursuant to this Section 5.4(m) and retain such capital equipment or goods after the Closing, in which case such capital equipment or assets shall not be included within the definition of Contributed Assets and any accounts payable related to such purchaser(s) shall not be included within the definition of Assumed Liabilities;

(n) not pay or commit to pay any bonus, other incentive compensation, change of control or similar compensation to any Transferred Employee, or grant or commit to grant to any

Transferred Employee, any other increase in or additional compensation in any form except as consistent with past practice;

(o) not enter into, institute, adopt or amend or commit to enter into, institute, adopt or amend any employment, consulting, retention, change of control, collective bargaining, bonus or other incentive compensation, profit-sharing, health or other welfare, stock option or other equity, pension, retirement, vacation, severance, deferred compensation or other employment, compensation or benefit plan, policy, agreement, trust, fund or arrangement in respect of or for the benefit of any officer, director, employee, sales representative, agent, consultant (whether or not legally binding) in connection with the Transferred Employees, agents or consultants;

(p) not mortgage, pledge or otherwise cause or suffer any Encumbrance to attach to any of the Graphics Chip Business Assets that would interfere with JV's use thereof or rights therein;

(q) not sell any Graphics Chip Business Assets with a value in excess of $25,000 in each case or $500,000 in the aggregate, other than inventory in the ordinary course of business;

(r) not make any material changes in policies or practices relating to selling practices, returns, discounts or other terms of sale or accounting therefor or in policies of employment relating to the Graphics Chip Business;

(s) except with respect to N-Vidia, not transfer or grant any rights under, or enter into any settlement regarding the breach or infringement of, any Contributed Intellectual Property, or amend or modify any existing rights with respect to any of the Contributed Intellectual Property, which would or could affect any rights necessary to JV's utilization of such Contributed Intellectual Property;

(t) replenish the inventories and supplies of the Graphics Chip Business

in a normal and customary manner consistent with its prior practice and prudent business practices prevailing in the industry, and not make any purchase commitment for the Graphics Chip Business in excess of the normal, ordinary and usual requirements of its business or at any price or upon terms and conditions more onerous than those consistent with prior practices and customary in the industry, and, other than in the ordinary course of business, not make any change in its selling, pricing, or advertising practices in the Graphics Chip Business inconsistent with its prior practice and prudent business practices prevailing in the industry;

(u) except with respect to N-Vidia or in the Side Letters, not institute, settle or agree to settle any litigation, action or proceeding in connection with, or relating to, the Graphics Chip Business or any Graphics Chip Business Assets, before any court or governmental body other than in the ordinary course of business consistent with prior practices but not in any case involving amounts in excess of $200,000 or the deprivation of any rights which JV would or could have under such assets or licenses; and

(v) not resolve or commit to effect any act in contravention of any of the provisions of this Section 5.4.

If S3 believes that it will be unable to perform the obligations set forth in this Section 5.4 or that it must modify its business practices in a manner inconsistent with this Section 5.4, then S3 shall so notify VIA in writing. VIA shall have 10 business days within which to advise S3 with regard to such matter and to consent or object to S3's proposed action or respond to the situation which is the subject of the notice. If VIA does not respond to S3 within such 10-day period, then VIA shall be deemed to have consented to S3's proposed action or response, if any. Nothing in this Section 5.4 or this Agreement or the Transaction Agreements shall limit or affect S3's right to enter into a merger or similar transaction involving S3 as a whole or to sell the assets of its Spea subsidiary or division or the assets of its Diamond, Number 9 or other add-in card or board business (to the extent not specifically identified in the Schedules hereto as being transferred to JV.

5.5 Commercially Reasonable Efforts.

(a) Subject to the terms and conditions herein provided, S3 and VIA each hereby covenants to the other that it shall use its commercially reasonable efforts to take or cause to be taken as promptly as practicable all actions necessary or desirable on its part to permit the consummation of the transactions contemplated by this Agreement. S3 will use commercially reasonable efforts to obtain all Consents, waivers and clearances of all third parties necessary to consummate and make effective the transactions contemplated by this Agreement. If any Consent is required to assign any Contract at the Closing, S3 may, after it has used commercially reasonable efforts to obtain such Consent or a Waiver on or before the Closing, either continue to use its commercially reasonable efforts after the Closing to cause that Contract to be assigned to JV, or take commercially reasonable efforts (so long as permitted by law and not in violation of the Contract in question) to assure that the rights and obligations of S3 under such Contract shall be preserved for the benefit of JV and to facilitate receipt of the consideration to be received by S3 in and under any such Contract with respect to performance rendered or amounts that otherwise accrue after the Closing, which consideration S3 shall hold in trust for the benefit of, and upon request of JV, shall deliver to JV. If S3 elects pursuant to the preceding sentence to retain any Contract and preserve the benefits thereof for JV, S3 shall take all legal action requested by JV to segregate or otherwise secure for JV any cash or other assets received under or by virtue of such Contract or Contracts after the Closing. To the extent that any of the Contributed Assets are not capable of being validly assigned or transferred without the Consent or waiver of the other Party thereto or the issuer thereof, or if such assignment or transfer would constitute a breach thereof or a violation of any Applicable Law, this Agreement shall not constitute an

assignment or transfer thereof.

(b) From the date hereof until the earlier of (i) the termination of this Agreement pursuant to Article 7 hereof and (ii) the Closing Date, S3 will not and will instruct its directors, officers, employees, Representatives, investment bankers, agents and Affiliates not to, directly or indirectly, (i) solicit or encourage submission of, any proposals or offers by any person, entity or group (other than VIA and its Affiliates, agents and Representatives), or (ii) participate in any discussions or negotiations with, or (iii) disclose any information concerning the Graphics Chip Business to or afford any access to the properties, books or records of the Graphics Chip Business, other than in the context of the sale of S3 as a whole or any other portion of its business or (iv) enter into any agreement or understanding with, any Person other than VIA and its Affiliates, agents and Representatives, in connection with any Acquisition Proposal, as

defined herein. S3 will immediately cease any and all existing activities, discussions or negotiations with any parties conducted heretofore with respect to any of the foregoing. S3 will (i) notify VIA as promptly as practicable if any inquiry or proposal is made or any information or access is requested in connection with an Acquisition Proposal or potential Acquisition Proposal and (ii) as promptly as practicable, notify VIA of the significant terms and conditions of any such Acquisition Proposal. In addition, from and after the date hereof until the earlier of (i) the termination of this Agreement pursuant to Article 7 and (ii) the Closing Date, S3 will not and will instruct its directors, officers, employees, Representatives, investment bankers, agents and Affiliates not to, directly or indirectly, make or authorize any public statement, recommendation or solicitation in support of any Acquisition Proposal made by any Person other than VIA. For the purposes of this Agreement, the term "Acquisition Proposal" shall mean any proposal or offer relating to any transaction, regardless of form, relating to S3's Graphics Chip Business or the Graphics Chip Business Assets, and the Excluded Licenses, other than transactions which involve the acquisition of S3 as a whole or any other portion of its business; provided, however, that nothing herein shall prohibit S3's Board of Directors from taking and disclosing to S3 stockholders a position with respect to any tender offer pursuant to Rules 14d-9 and 14e-2 promulgated under the Exchange Act. Nothing herein shall prohibit VIA from seeking injunctive or other equitable relief for any breach of this Section 5.5(b).

(c) In the event (i) S3 breaches the provisions of Section 5.5(b), or (ii) S3, prior to the Closing Date, engages in transactions or conduct of the type described in Section 5.5(b) which results in the termination of the Intel License prior to the Closing Date and if, as a result of either (i) or (ii), the transactions contemplated by this Agreement are not consummated in accordance with this Agreement, S3 shall, within 48 hours of VIA's demand, pay VIA a break-up fee of $12 million which shall fully and completely compensate VIA for costs and expenses incurred in connection with VIA's due diligence investigation, the preparation of documents in connection with the transactions contemplated by this Agreement and any other matters contemplated by this Agreement. Except for injunctive or other equitable relief which VIA may seek to enforce the provisions of Section 5.5(b), the break-up fee shall be VIA's sole and exclusive remedy for any claims, losses or damages arising out of or relating to a failure to consummate the transactions contemplated by this Agreement for the reasons set forth in this Section 5.5(c).

5.6 Intel License.

(a) If JV is Enjoined from Utilizing the Intel License (as defined in Section 5.6(h) below), because on or after the Closing Date S3 (i) engaged in transactions or conduct effecting a "Merge" (sic) or "Change of Control" of S3 (as those terms are defined in Section 6 of the Intel License) (other than entering into or consummating the transactions contemplated by this Agreement and the JV Transaction Agreements), or (ii) affirmatively engaged in acts or

conduct whether by commission or omission (other than entering into or consummating the transactions contemplated by this Agreement and the JV Transaction Agreements or entering into a settlement agreement with Intel), then the following liquidated damages shall apply to compensate JV and VIA for any and all losses they may suffer as a result thereof, subject to the Maximum Damage Cap set forth in Article 9 below, and such liquidated damages shall be VIA's and JV's sole and exclusive remedy against S3 for any and all damages and claims relating to the matters set forth in this Section 5.6 (a). S3 shall be entitled to first setoff any amount owing to JV or VIA under this Section against any amounts due S3 pursuant to Section 8.3 or 8.4 and such

amount shall be credited against such payment otherwise due by S3 or any royalty payments made by S3 pursuant to Section 5.6(e).

(i) If JV is Enjoined from Utilizing the Intel License Agreement commencing during the first 5 years following the Closing Date, then following the conclusion of said period, for each day of such 365 day period that occurred during the 5-year period following the Closing Date, S3 shall pay JV $191,780.82, within 30 days of written demand by JV, as liquidated damages; and

(ii) If such 365 day period commences or ends during the sixth year following the Closing Date, then following the conclusion of said 365 day period, for each day of such 365 day period that occurred during the sixth year period following the Closing Date, S3 shall pay JV $123,287.67, within 30 days of written demand by JV, as liquidated damages.

(b) If during the first 5 years after the Closing Date (i)S3 entered into a settlement agreement with Intel such that JV can no longer operate under the Intel License, then the following liquidated damages shall apply to compensate JV and VIA for any and all losses they may suffer as a result thereof, subject to the Maximum Damage Cap set forth in Article 9 below, and such liquidated damages shall be VIA's and JV's sole and exclusive remedy against S3 for any and all damages and claims relating to the matters set forth in this Section 5.6 (b). S3 shall be entitled to first setoff any amount owing to JV or VIA under this Section against any amounts due S3 pursuant to Section 8.3 or 8.4 and such amount shall be credited against such payment otherwise due by S3 or any royalty payments made by S3 pursuant to Section 5.6(e).

(i) If as a result of entering into a settlement agreement with Intel, S3 loses the Intel License, then S3 shall pay JV $35 million within 30 days after the date that S3 enters into such settlement agreement, provided, that S3 may setoff against up to $35 million of such payment, 50% of any damages or other payments that S3 is required to pay to Intel as consideration for such settlement.

(ii) If S3 does not lose the Intel License as a result of entering into a settlement agreement with Intel, then: (A) if such settlement is a Settlement With Release (as defined below), S3 shall pay JV $45 Million within 30 days after the date that S3 enters into such settlement agreement, provided, however, S3 may setoff against up to $35 million of such payment 50% of any damages or other payments, after the first $20 million of such damages or other payments that S3 is required to pay to Intel as consideration for such settlement, or (B) if such settlement is not a Settlement With Release, S3 shall pay JV $70 million within 30 days after the date that S3 enters into such settlement.

For purposes hereof, a Settlement With Release means that a settlement by S3 with Intel provides a release through the settlement date for all past manufacture and/or distribution of JV's products (including the inventory purchased from S3). For purposes of clauses (i) and (ii), JV's share of "damages or other payments that S3 is required to pay to Intel as consideration for such

settlement" shall only apply in a Settlement With Release, and in such instance only to such damages or other payments related to the transactions contemplated hereby (including the

transfer of the Graphics Business Assets to JV), JV's products (including the inventory purchased from S3), or any action or omission by JV, VIA or any Affiliate thereof, and shall not include pre-payment of royalties for JV products after such date. Liquidated damages under this Section 5.6(b) shall be paid by S3 as of the later of 30 days after: (i) the date of S3's settlement with Intel, or (ii) the fourth anniversary of the Closing.

(c) If JV is Enjoined from Utilizing the Intel License (as defined in Section 5.6(h) below) because of the acts or omissions of either or both of the parties prior to, or associated with, entering into or consummating the transactions contemplated by this Agreement and the JV Transaction Agreements (the "Transaction-Related Acts or Omissions"), then the following liquidated damages shall apply to compensate JV and VIA for any and all losses they may suffer as a result thereof, subject to the Maximum Damage Cap set forth in Article 9 below, and such liquidated damages shall be VIA's and JV's sole and exclusive remedy against S3 for any and all damages and claims relating to the matters set forth in this Section 5.6(c):

(i) If such 365 day period commences or ends during the first 5 years following the Closing Date, then following the conclusion of said 365 day period, for each day of such 365 day period that occurred during the 5 year period following the Closing Date, S3 shall pay JV $95,895.41 within 30 days of written demand by JV, as liquidated damages; and

(ii) No liquidated damages will be due under this Section 5.6(c) with respect to days outside the five (5) year period that commences on the Closing Date.

(d) Notwithstanding anything to the contrary herein, in no event shall VIA or JV be entitled to any damages (liquidated or otherwise) as set forth in this Section 5.6 if, on or after the Closing Date or prior to the effective date of any act or omission which would otherwise give rise to S3's liability pursuant to Section 5.6(a), (b) or (c), the Intel License terminates or ceases to cover the manufacture, sale or use by JV as a Subsidiary of S3 or otherwise of any products in the Graphics Chip Business, or (ii) JV is Enjoined from Utilizing the Intel License, due, in either (i) or (ii) to an act or omission by JV or VIA (other than the Transaction-Related Acts or Omissions that are subject to Section 5.6(c) above, provided that such Transaction-Related Acts or Omissions are undertaken in good faith).

(e) If, on or after the Closing Date, S3 engages in transactions or other affirmative conduct which causes the Intel License to become royalty bearing pursuant to Section 6.7 of the Intel License, then the Parties agree (i) to allocate the Revenue Cap (as defined in the Intel License) equally between S3 and JV and (ii) that S3 shall be responsible for the payment of royalties due under the Intel License on account of the operations of the Graphics Chip Business conducted by JV after the Closing until such time as the maximum amount available under the Maximum Damage Cap set forth in Article 9 is exhausted and JV shall be responsible thereafter and shall pay S3 in cash for the royalties related to the operations of the Graphics Chip Business by JV prior to the due date to Intel. S3 may setoff any royalty amounts owed on account of the Graphics Chip Business, pursuant to this Section 5.6(e), against amounts owed to S3 by JV or VIA under the Guaranty or Sections 8.3 or 8.4 hereof. Notwithstanding the foregoing, if S3's

revenue from operations that is subject to the Revenue Cap is less than its 50% allocation, then S3 shall reallocate any unused portion to JV.

(f) JV hereby agrees in writing to be subject to the terms, conditions and obligations of the Intel License, to the extent necessary to derive any benefits therefrom.

(g) S3, VIA or JV, as the case may be, shall, at its sole cost and expense use commercially reasonable efforts to defend any claim or cause of action for damages, rescission or other legal or equitable relief brought against it arising from or relating to the transactions contemplated by this Agreement or the Intel License which could impair JV's utilization thereof. Each party shall provide the other parties notice of any such claim or cause of action within 5 business days after the disclosing party's receipt of notice thereof. S3 shall consult with JV and VIA concerning the joint defense of such claim or action, all subject to the terms of a mutually agreeable joint defense and confidentiality agreement to be agreed upon by S3, VIA and JV. After making a payment under Section 5.6(a), 5.6(b) or 5.6(c), S3 will have no further liability or obligation under this Section 5.6.

(h) "Enjoined from Utilizing the Intel License" shall mean that: (i) a court has entered an order holding, or S3 has entered into a written agreement with Intel agreeing that, the Intel License does not cover the manufacture, sale or use by JV as a subsidiary of S3 or otherwise, of any products in the Graphics Chip Business or (ii) a court has, at the request of Intel, entered an order enjoining the sale by JV of such products including without limitation any importation bans thereon, provided, that if S3 appeals such order described in (i) or (ii) of this Section 5.6(h), JV shall only be deemed to have been "Enjoined from Utilizing the Intel License" if such order is maintained for a contiguous 365 day period beginning after the Closing Date, or if the order is stayed or dropped and within 30 days thereafter the order is reinstated, then if the old and new orders are maintained for a cumulative period of 365 days excluding the intervening period, then the "Enjoined from Utilizing the Intel License" event shall be deemed to be effective for purposes of determining S3's payment obligations hereunder on the last day of such 365 day period.

(i) In no event shall S3 be required to make more than 1 payment pursuant to Section 5.6(a), 5.6(b) or 5.6(c), whether JV is Enjoined from Utilizing the Intel License more than once during the 5 year period referenced therein or otherwise, nor shall S3 after making a single payment under any of Section 5.6(a), 5.6(b) or 5.6(c) be required to make any further payments under any of Section 5.6(a), 5.6(b) or 5.6(c) under any circumstances; if S3 makes a payment under any clause of Section 5.6(b), it cannot be required to make any payment under any other clause of that Section. Any payment due under Section 5.6(a), 5.6(b) or 5.6(c) shall be net of any royalty payments made by S3 (except those paid to S3 by JV) under Section 5.6(e).

(j) Except as set forth in this Section 5.6, S3 and its Affiliates shall use commercially reasonable efforts to maintain and keep in full force and effect the Excluded Licenses and to secure for the benefit of JV all such Licenses to the extent permitted therein, and shall not Transfer any of the Excluded Licenses other than in connection with a merger or consolidation of S3 or the sale of all or substantially all of its assets, as a whole, or a sale of any division or line of business of S3.

5.7 Filings. The Parties shall use their respective best efforts to promptly take all such action as may be necessary under United States federal, state and other laws applicable to or necessary for the consummation of the transactions contemplated hereby, and will file and, if appropriate, use their best efforts to have declared effective or approved all documents and notifications with all governmental or regulatory authorities that it deems necessary or appropriate for the consummation of the transactions contemplated

hereby, including all filings necessary under the HSR Act and the Exxon-Florio Amendment to Section 721 of the Defense Production Act of 1950. If either Party fails to file any necessary amendments to its current HSR application that are necessary to reflect this Agreement on or before a date two weeks after the date of this Agreement, then such defaulting Party shall promptly pay on demand $5 million to the other Party.

5.8 Expenses. Except as otherwise provided herein, all costs and expenses incurred in connection with this Agreement and the transactions contemplated hereby (including fees and disbursements of financial advisors, accountants and attorneys) shall be paid (i) by S3, if such costs or expenses are incurred by or on behalf of S3 (and such costs and expenses shall not be considered Assumed Liabilities if incurred by S3), and (ii) by VIA, if such costs or expenses are incurred by or on behalf of VIA.

5.9 Stamp Taxes, Duties, etc. All sales, transfer, filing, recordation and similar taxes and fees (including all real estate transfer taxes and conveyance and recording fees, if any), and all stamp taxes, registration taxes, duties or other similar charges arising from or associated with the transactions contemplated hereby shall be borne by JV. The parties agree to reasonably cooperate with each other in good faith to minimize any such taxes or fees.

5.10 Required Notices. At all times prior to the Closing Date, S3 and VIA shall promptly, upon obtaining knowledge thereof, give written notice to each other of (i) any facts or circumstances or the occurrence of any event or the failure of any event to occur, which will, or could reasonably be expected to, result in (x) a Material Adverse Effect, (y) a material adverse effect on such person's or any of its Affiliates' ability to consummate the transactions contemplated hereby or to satisfy its obligations hereunder, or (z) a material breach of any representation or warranty made by such person or any of its Affiliates in this Agreement, (ii) any failure by such person or any of its Affiliates to comply in all material respects with any covenant, condition or agreement contained in this Agreement, (iii) any material complaints, investigations, proceedings or hearings of any Governmental Authority or agency with respect to this Agreement, S3, the Contributed Assets or the transactions contemplated hereby, and (iv) any institution or threat of institution of any litigation or similar action with respect to this Agreement, S3, the Contributed Assets or the consummation of the transactions contemplated hereby.

5.11 Insurance. S3 shall keep all insurance policies currently insuring the Contributed Assets or substantially equivalent insurance policies in full force and effect up to the Closing Date and S3 shall pay all premiums in respect thereto covering all periods up to and including the Closing Date. S3 shall assign to JV all its assignable rights and claims under all insurance policies of S3. To the extent that any claim that S3 has or may have pursuant to such insurance policies is not assignable, JV and S3 shall cooperate to pursue such claim and all amounts recovered by S3 pursuant to such policies shall immediately be paid to JV.

5.12 Employee Matters. From and after the Closing Date, JV shall provide Transferred Employees comparable employment at the same base compensation rate and with generally similar responsibilities as applicable to such Transferred Employees immediately prior to the Closing Date. JV shall establish employment policies and procedures substantially similar to those in effect at S3 as of the date of this Agreement and shall establish substantially similar welfare benefit plans for such employees.

5.13 Option Obligations. If, after the Closing Date, a Transferred Employee exercises a stock option to purchase S3 common stock, then, within 5 business days of such exercise, JV shall pay S3 the difference between the exercise price of such stock option held by the Transferred Employee and a price per share equal to the lowest closing price for S3 common stock on the Nasdaq National Market during the 5 business days preceding the date of this Agreement.

5.14 Historically Audited Financial Statements of Graphics Chip Business. On or before a date which is 90 days from the Closing Date, S3 shall, at its sole cost and expense, deliver to JV audited financial statements of the Graphics Chip Business as conducted by S3 for its last three fiscal years, along with the unqualified audit report of Ernst & Young LLP thereon.

5.15 Monthly Financial Statements. Within 15 days following each month end between the date of this Agreement and the Closing Date, S3 shall prepare and deliver to VIA unaudited financial statements of the Graphics Chip Business as of the month then ended.

5.16 Closing Balance Sheet. S3 shall prepare and deliver a Closing Balance Sheet to JV within 14 days after the Closing Date, prepared in accordance with GAAP applied on a consistent basis, reflecting only the Graphics Chip Business Assets and the Assumed Liabilities and Additional Capital Assets (if any).

5.17 Intentionally Deleted.

5.18 Updated S3 Schedules. S3 shall prepare and deliver to VIA updated Schedules under this Agreement 4 business days prior to the Closing Date (the "Updated S3 Schedules") and shall cooperate with the Outside Auditor in taking a physical inventory on or before the Closing Date.

5.19 Retention Plan. VIA shall adopt and implement a retention plan applicable to Transferred Employees only and shall be responsible for the costs of such plan; provided, that if the Closing does not occur solely as a result of action or inaction by S3, then S3 shall promptly reimburse VIA for all such costs up to a maximum amount of $8,000,000.

5.20 Rights Agreement. The S3 Rights Agreement dated as of May 14, 1997 between the First National Bank of Boston and S3 (the "Rights Agreement") shall be amended if VIA at any time after the Closing ceases to hold S3 stock representing at least 15% of all voting interests in S3 to delete the effect of the amendment referenced in the next sentence. On or before the Closing, the Board of Directors of S3 shall take, or cause to be taken, all requisite corporate action to insure that VIA shall not, by virtue of its acquisition of shares of S3 at the Closing pursuant to the Warrant, become an "Acquiring Person" as defined in S3's Rights Agreement, dated as of May 14, 1997, between S3 and The First National Bank of Boston (the "Rights Agreement"), and that no "Distribution Date" as defined in such agreement, shall occur, or be deemed to have occurred, by virtue of the foregoing acquisition of shares by VIA.

5.21 Investor Rights Agreement. The Amended and Restated Investor Rights Agreement, dated February 18, 2000, between S3 and VIA shall be further amended and restated to include the shares of S3 Common Stock purchased by VIA upon exercise of the S3 Warrant.

5.22 Additional Capital Assets. Schedule 5.21 sets forth a list of capital assets with respect to which S3 has placed an order to purchase but has not yet received delivery. Schedule 5.21 shall be amended prior to the Closing Date to add any other assets whose purchase is approved by VIA pursuant to Section 5.4(m). On or before the Closing Date, VIA will designate those assets listed on Schedule 5.21, which shall become additional Contributed Assets ("Additional Capital Assets"). S3 shall retain any such assets which VIA has not designated as Contributed Assets. If S3 has received delivery of an Additional Capital Asset, the liability relating to that asset, if any, shall be assumed by JV on the Closing Date as an Assumed Liability. If S3 has not received delivery of an Additional Capital Asset, it shall transfer its rights and obligations under the applicable contract or purchase order to JV at Closing.

5.23 Covenant Not to Sue. From and after the date of this Agreement

until the earlier of either (a) termination of this Agreement by either party or (b) January 30, 2001, S3 will not, on behalf of itself, or in cooperation or participation with any other person, firm, entity, corporation, institute, or government agency, file, refile, or in any manner participate in or prosecute any claim, charge, grievance, complaint, or action of any sort against any party to the Release before any local, state or federal court, arbitrator, administrative agency, board or tribunal concerning any matter arising out of or in connection with the failure to close the transactions contemplated by the Investment Agreement, dated as of April 10, 2000, between VIA and S3, and the exhibits and schedules thereto, including without limitation the application submitted by VIA to the government of Taiwan in connection with said Investment Agreement and VIA's failure to obtain the Taiwanese government's approval of such application.

5.24 Insurance. S3 will file and diligently prosecute claims for loss of Contributed Assets due to fire, theft or other casualty covered by insurance maintained by S3.

ARTICLE 6.

CONDITIONS TO CLOSING

6.1 Conditions to the Obligations of VIA. The obligations of VIA under this Agreement shall be subject to the satisfaction at or prior to the Closing of each of the following conditions, unless waived as provided in Section 10.1:

(a) Representations, Warranties and Agreements. All representations and warranties made herein by S3 shall be true and correct in all respects on the date hereof and (except as contemplated hereby) at and as of the Closing Date with the same effect as though made at and as of such date, except to the extent due to the acts or failure to act by VIA (without the concurrence of S3) pursuant to the Management Agreement, and S3 shall have performed in all respects all covenants and agreements required by this Agreement and the other JV Transaction Agreements to be performed by it at or prior to the Closing Date except for such changes in the representations and warranties, and failure of performance, that individually or in the aggregate do not have a Material Adverse Effect on the Graphics Chip Assets, as of the Closing Date. VIA shall have received from S3 certificates, dated the Closing Date and signed by authorized officers of S3, to the foregoing effect.

(b) Authorizations, Approvals and Consents. The mandatory waiting period under the HSR Act (including any extension thereof) shall have expired, the approval of VIA's Board of Directors and S3's Board of Directors shall have been received, and the authorizations, approvals, consents and other items required in connection with the execution and delivery of this Agreement and the other JV Transaction Agreements or the consummation of the transactions contemplated hereby or thereby shall have been obtained.

(c) No Injunction, etc. Consummation of the transactions contemplated hereby shall not have been restrained, enjoined or otherwise prohibited by any Applicable Law, including any order, injunction, degree or judgment of any Governmental Authority. No Governmental Authority shall have determined any Applicable Law to make illegal the consummation of the transactions contemplated hereby or by the other JV Transaction Agreements.

(d) Execution of JV Transaction Agreements. The JV Transaction Agreements shall have been executed and delivered by all Parties thereto (other than VIA) and shall be in full force and effect.

(e) Opinion of Counsel to S3. VIA shall have received an opinion or opinions, dated as of the Closing Date, from counsel to S3 substantially in the form attached hereto as Exhibit 13.

(f) Updated S3 Schedules. VIA shall have received the Updated S3 Schedules and the changes reflected therein from the original S3 Schedules delivered upon the signing of this Agreement shall not constitute a Material Adverse Effect.

6.2 Conditions to the Obligations of S3. The obligations of S3 under this Agreement shall be subject to the satisfaction at or prior to the Closing of each of the following conditions, unless waived as provided in Section 10.1:

(a) Representations, Warranties and Agreements. All representations and warranties made herein by VIA shall be true and correct in all respects on the date hereof and (except as contemplated hereby) at and as of the Closing Date, with the same effect as though made at and as of such date, and VIA shall have performed in all respects all covenants and agreements required by this Agreement and the other JV Transaction Agreements to be performed by it at or prior to the Closing Date. S3 shall have received from VIA certificates, dated the Closing Date and signed by authorized officers of S3, to the foregoing effect. S3 shall have received from VIA certificates, dated the Closing Date and signed by authorized officers of S3 to the effect all representations and warranties made herein by VIA shall be true and correct in all material respects on the Closing Date.

(b) Authorization, Approvals and Consents. The mandatory waiting period under the HSR Act (including any extensions thereof) shall have expired, the approval of S3's Board of Directors shall have been received and the authorizations, approvals, consents and other items required in connection with the execution and delivery of this Agreement and the other JV Transaction Agreements or the consummation of the transactions contemplated hereby or thereby shall have been obtained.

(c) No Injunction, etc. Consummation of the transactions contemplated hereby shall not have been restrained, enjoined or otherwise prohibited by any Applicable Law, including any order, injunction, degree or judgment of any Governmental Authority. No Governmental Authority shall have determined any Applicable Law to make illegal the consummation of the transactions contemplated hereby or by the other JV Transaction Agreements.

(d) Execution of JV Transaction Agreements. The JV Transaction Agreements shall have been executed and delivered by all Parties thereto (other than S3) and shall be in full force and effect.

ARTICLE 7.

TERMINATION

7.1 Bases for Termination. This Agreement may be terminated at any time prior to the Closing:

(a) by mutual written consent of S3 and VIA;

(b) by either S3 or VIA, if the Closing shall not have occurred by the Scheduled Closing Date or such later date as S3 and VIA shall agree in writing, otherwise than on account of a breach of this Agreement by the terminating Party;

(c) by VIA, if there has been a material breach of any representation, warranty, covenant or agreement on the part of S3 giving rise to or resulting in a Material Adverse Effect;

(d) by either S3 or VIA, if a Governmental Authority (other than the government of Taiwan or any agency or committee or subdivision thereof) shall have issued an order, decree or ruling or taken any other action, in any case having the effect of permanently restraining, enjoining or otherwise prohibiting the Closing or any of the transactions contemplated hereby or by the JV Transaction Agreements, which order, decree or ruling is final and non-appealable;

(e) by either S3 or VIA, if S3 is required to pay a break-up fee pursuant to Section 5.5(c).

7.2 Effect of Termination. Any termination of this Agreement under Article 7 will be effective immediately upon the delivery of written notice of the terminating Party to the other parties hereto. Upon any termination of this Agreement by either S3 or VIA as provided in Section 7.1, this Agreement shall forthwith become null and void ab initio and there shall be no liability or obligation on the part of S3 or VIA or their respective Affiliates, officers, directors or employees and except that the provisions of Section 5.2, 5.3, 5.5(c), 5.8, 5.9 and 7.2 shall survive any termination of this Agreement.

7.3 Failure to Close; Escrow. If the Closing shall not have occurred by January 3, 2001, and if the failure to close is due solely as a result of action taken or inaction by S3, where, but for such action or inaction, the Closing would have occurred, then S3 shall pay VIA $20,000,000. Such amount shall be paid on the termination of this Agreement. If the Closing shall not have occurred by the Scheduled Closing Date, and if the failure to close is not solely due to action or inaction taken by S3, VIA shall immediately pay S3 either $60,000,000 in cash or 6,000,000 shares of S3 common stock or any linear combination thereof. As security for such payment, concurrent with the execution of this Agreement, VIA shall execute the Escrow Agreement and shall deliver to S3 or its agent for deposit into escrow $60,000,000 in cash or 6,000,000 shares of S3 common stock or any linear combination thereof (the "Escrow Assets"). The payment provided by Section 5.7 and the payments provided in this Section 7.3 shall constitute the sole and exclusive remedy of any Party for damages resulting from the failure to timely file a HSR application under Section 5.7 and the failure to close under this Section 7.3.

ARTICLE 8.

INDEMNIFICATION, CONTRIBUTION AND SURVIVAL

8.1 Survival of Representations and Warranties. The representations and warranties of S3 and VIA set forth in this Agreement or in any certificate delivered by either of them pursuant to this Agreement, except those set forth in Sections 3.6 and 3.19 which shall survive for the appropriate statute of limitations, shall survive the Closing Date and the consummation of the transactions contemplated hereby for a period of 1 year after the Closing Date and will then and thereupon terminate. No claim shall be made by any Person by virtue of or arising out of or resulting from or relating to the breach of any such representation or warranty unless written notice of such claim shall have been given on or prior to the date on which such representation or warranty shall expire, in which event each such representation and warranty shall, solely with respect to such claim and all other claims arising out of the same specific facts or circumstances, survive until such claims are resolved and all obligations with respect thereto are satisfied. All covenants and agreements of the Parties herein shall survive the Closing without any limitation.

The Parties agree that any amounts owing by S3 on account of, or as a result of, a breach of any of its representations or warranties shall be first setoff against amounts owed by JV under this Agreement, or by VIA under the Guaranty, VIA agrees that such setoff by S3 against amounts owed by JV and VIA shall

satisfy any obligation owing by S3 to JV or VIA as a result of such breach.

8.2 Indemnification by S3. S3 hereby agrees to indemnify and hold harmless VIA and JV (and each of their respective directors, officers and Affiliates and their respective successors and permitted assigns) from and against any and all losses, obligations, deficiencies, liabilities, claims, damages, costs and expenses (including without limitation the amount of any settlement of any claim subject of this indemnification and all reasonable legal and other expenses incurred in connection with the investigation, prosecution or defense of any matter indemnified pursuant hereto) (collectively, "Damages") which any such indemnified Party may sustain, suffer or incur directly or indirectly and which result from, arise out of, are caused by or relate to (a) the breach by S3 of any representation, warranty, covenant or agreement made by it in this Agreement or in any agreement or instrument executed and delivered by it pursuant hereto (b) any liability, whether absolute or contingent, arising out of or related to the ownership or to the operation of the Graphics Chip Business prior to the Closing Date and not included in the Assumed Liabilities or (c) any liability arising under the Warner Act as it may apply to the transactions contemplated by this Agreement and the JV Transaction Agreements and S3's termination of any of its employees; provided, however that any breach or liability arising from acts or failure to act by VIA pursuant to the Management Agreement, and any liability arising from the termination of employment of any Transferred Employee subsequent to the Closing, is not subject to this clause (c).

8.3 Indemnification by VIA. VIA hereby agrees to indemnify and hold harmless S3 and JV (and each of their respective directors, officers and Affiliates and their respective successors and permitted assigns) from and against any and all Damages which any such indemnified Party may sustain, suffer or incur directly or indirectly and which result from any breach by VIA of any representation, warranty, covenant or agreement made by it in this Agreement or in any agreement or instrument executed and delivered by it pursuant hereto and any failure by JV to pay, when due, any of the Assumed Liabilities.

8.4 Indemnification by JV. JV hereby agrees to indemnify and hold harmless S3 and VIA (and each of their respective directors, officers and Affiliates and their respective successors and permitted assigns) from and against any and all Damages which any such indemnified Party may sustain, suffer or incur directly or indirectly and which result from any breach by JV of any representation, warranty, covenant or agreement made by it in this Agreement or in any agreement or instrument executed and delivered by JV pursuant hereto, including, without limitation, any failure by JV to pay, when due, any of the Assumed Liabilities.

8.5 Claims. Any claim for indemnity under Section 8.2, 8.3 or 8.4 hereof shall be made by written notice from the indemnified Party to the indemnifying Party specifying in reasonable detail the basis of the claim. When an indemnified Party seeking indemnification under Section 8.2, 8.3 or 8.4 receives notice of any Third Party Claims which is to be the basis for a claim for indemnification hereunder, the indemnified Party shall give written notice within a reasonable period thereof to the indemnifying Party reasonably indicating (to the extent

known) the nature of such claims and the basis thereof. Any failure by the indemnified Party to provide such notice shall not affect the indemnifying Party's obligations hereunder, except to the extent of any material liability caused by such delay. Upon notice from the indemnified Party, the indemnifying Party may, but shall not be required to, assume the defense of any such Third Party Claim, including its compromise or settlement, and the indemnifying Party shall pay all reasonable costs and expenses thereof and shall be fully responsible for the outcome thereof; provided, however, that the indemnifying Party may not settle or compromise any Third Party Claim without the indemnified Party's prior written consent (which consent shall not be unreasonably

withheld). The indemnifying Party shall give written notice to the indemnified Party as to its intention to assume the defense of any such Third Party Claim within ten (10) business days after the date of receipt of the indemnified Party's notice in respect of such Third Party Claim. If an indemnifying Party does not, within ten (10) business days after the indemnified Party's notice is given, give written notice to the indemnified Party of its assumption of the defense of the Third Party Claim, the indemnifying Party shall be deemed to have waived its rights to control the defense thereof. If the indemnified Party assumes the defense of any Third Party Claim because of the failure of the indemnifying Party to do so in accordance with this Section 8.5, the indemnifying Party shall pay all reasonable costs and expenses of such defense and shall be fully responsible for the outcome thereof. The indemnifying Party shall have no liability with respect to any compromise or settlement thereof effected without its prior written consent (which consent shall not be unreasonably withheld).

8.6 Limitation of Liabilities. Neither S3, nor JV nor VIA shall be obligated to provide indemnification under Sections 8.2, 8.3 or 8.4, respectively, unless the aggregate amount of all claims for which any Party is liable under Section 8.2, 8.3 or 8.4, respectively, exceeds $500,000, in which case such Party shall be liable for all such amounts. Further, the Parties agree that the aggregate maximum liability of S3 or VIA, as the case may be, from or on account of a breach of representations and warranties or on an account of any indemnification obligations arising under Sections 8.2 (excepting 8.2(b) and 8.2(c)), 8.3 and 8.4 shall be capped at $30 million, provided, however, that such cap shall not apply to any liability arising from any failure by VIA or JV to discharge or pay the Assumed Liabilities, when due. Notwithstanding anything to the contrary herein, such limit shall not apply to, and be exclusive of, VIA or JV's obligations to S3 pursuant to Section 5.13(a) hereof. In the case of S3, any obligation arising under Sections 5.6(a) through (c), 5.6(e) and 8.2 shall first be satisfied through setoff against amounts owed by JV or VIA to S3 under Section 8.3 or 8.4 hereof. In the case of VIA or JV, any obligation under Section 8.3 or 8.4 hereof, as the case may be, shall first be satisfied through setoff against amounts owed to JV or VIA by S3 under Sections 5.6(a) through (c), 5.6(e) and Section 8.2.

ARTICLE 9.

MAXIMUM DAMAGES CAP

The Parties agree that the total liability of S3 on the one hand (including its aggregate payment obligations under Sections 2.5, 5.6, 5.8, 5.13(b), and Article 8) and JV and VIA, on the other hand, on account of any breach of this Agreement or of the JV Transaction Agreements, of whatever kind or nature and for whatever reason, shall be limited to a maximum amount of $70 million; provided, however, that with respect to VIA's and JV's liability to S3 such limit

shall not apply to, and shall be exclusive of, (i) any amounts owed under Sections 2.2(c) and (d) of this Agreement or the Guaranty, or (ii) any amounts owed or liability incurred by JV to S3 pursuant to Section 5.13 of this Agreement, or (iii) any amounts payable by JV under Section 5.6(e), or (iv) any amounts owed by VIA or JV to S3 under Section 8.3 or 8.4 or otherwise as a consequence of JV's or VIA's failure to pay or discharge the Assumed Liabilities, when due. The Parties further agree that S3's obligation to pay certain royalties, pursuant to Section 5.6(e), shall be limited to and capped at an amount equal to the difference between $70 million less (i) any amounts theretofore set off by S3 against the amounts owing by JV to S3 under this Agreement, pursuant to the terms of this Agreement, and (ii) any amounts theretofore paid in cash by S3 to JV or VIA pursuant to Sections 5.6(a) through (c); provided, however, that there shall not be any duplication for such setoffs and any such payment made directly by S3 to JV or VIA. None of the Parties' obligations under Section 5.7 or 7.3 shall be subject to this Article 9.

ARTICLE 10.

MISCELLANEOUS

10.1 Amendments and Waivers. This Agreement may be amended or modified in whole or in part at any time prior to the Closing by an instrument in writing executed by each of the Parties in the same manner as this Agreement. In addition, any Party may, at its option, by an instrument in writing executed in the same manner as this Agreement, waive or extend the time for the fulfillment of any or all of the conditions herein contained to which its obligations hereunder are subject. No failure by any Party to take any action with respect to a breach of this Agreement or a default by another Party shall constitute a waiver of the former Party's right to enforce any provision of this Agreement or to take action with respect to such breach or default or any subsequent breach or default. Waiver by any Party of any breach or failure to comply with any provision of this Agreement by another Party shall not be construed as, or constitute, a continuing waiver of such provisions, or a waiver of any other breach of or failure to comply with any other provisions of this Agreement.

10.2 Notices. All notices, requests, consents, demands, instructions, approvals and other communications hereunder shall be delivered to all parties hereto, shall be in writing and shall be validly given, made or served, if delivered personally or sent by mail, recognized courier service, telex or telefax (confirmed by mail or recognized courier service in the case of telefaxes), and shall be deemed effective when actually received, as follows (or as designated in writing by any Party from time to time):

If to S3, to:

S3 Incorporated
2841 Mission College Blvd.
Santa Clara, California 95054
Attention: President
Fax: (408) 588-8050

With copies to:

Pillsbury Madison & Sutro LLP
2550 Hanover Street
Palo Alto, California 94304
Attention: Jorge A. Del Calvo, Esq.
Fax: (650) 233-4545

If to VIA, to:

VIA Technologies, Inc.
8F, No. 553 Chung-Cheng Road
Hsing-Tien, Taipei
Taiwan
Attention: President
Telecopier: 886-2-2218-7970

With copies to:

Heller Ehrman White & McAuliffe LLP
525 University Avenue
Palo Alto, California 94301-1900
Attention: Sarah A. O'Dowd, Esq.
Fax: (415) 324-0638

If to JV, to:

JV
2841 Mission College Blvd.
Santa Clara, California 95054
Attention: President
Fax: (408) 588-8050

With copies to:

Heller Ehrman White & McAuliffe LLP
525 University Avenue
Palo Alto, California 94301-1900
Attention: Sarah A. O'Dowd, Esq.
Fax: (415) 324-0638

10.3 Assignment. Except as otherwise expressly provided herein, none of the Parties shall assign this Agreement or any rights, benefits or obligations hereunder without the prior written consent of the other Parties. Any attempt to so assign or delegate any of the foregoing without such consent shall be void.

10.4 Governing Law. This Agreement shall be governed by and construed in accordance with the internal laws of the State of Delaware. For purposes of any action or proceeding

involving this Agreement, JV hereby expressly submits to the jurisdiction of all federal and state courts located in the State of California and consents to be served with any process or paper by registered mail or by personal service within or without the State of California.

10.5 Section and Other Headings. Headings of the articles, sections and subsections of this Agreement are inserted for convenience only and shall not be deemed to constitute a part hereof.

10.6 Counterparts. This Agreement may be executed in any number of counterparts, all of which taken together shall constitute one and the same instrument, and each fully executed counterpart shall be deemed an original.

10.7 Entire Agreement. This Agreement (including the Schedules hereto) and the other JV Transaction Agreements constitute the entire and only agreement between the Parties relating to the subject matter hereof. Any and all prior arrangements, representations, promises, understandings and conditions in connection with said matter and any representations, promises or conditions not expressly incorporated herein or expressly made a part hereof shall not be binding upon any Party.

10.8 Severability. In the event that any one or more of the provisions contained in this Agreement or in any other instrument referred to herein, shall, for any reason, be held to be invalid, illegal or unenforceable, such illegality, invalidity or unenforceability shall not affect any other provisions of this Agreement.

10.9 Benefits Only to Parties. Other than as set forth in Article 8 hereof, nothing expressed by or mentioned in this Agreement is intended or shall be construed to give any Person other than the Parties and JV and their respective successors or assigns any legal or equitable right, remedy or claim under or in respect of this Agreement or any provision herein contained, this Agreement and all conditions and provisions hereof being intended to be and being for the sole and exclusive benefit of the Parties and JV and their respective successors and assigns and for the benefit of no other Person.

<PAGE> 46

IN WITNESS WHEREOF, each of the Parties has caused this Agreement to be duly executed on its behalf by one of its officers thereunto duly authorized, all as of the date and year first above written.

S3 Incorporated

By: /s/ Ken Potashner

Name: Ken Potashner
Title: Chief Executive Officer

VIA Technologies, Inc.

By: /s/ Wen-Chi Chen

Name: Wen-Chi Chen
Title: President and Chief Executive Officer

JV

By:

Name:
Title:

</TEXT>
</DOCUMENT>

Exhibit 14

CBI 10-241

THOMAS L. JARVIS
202.408.4093
tom.jarvis@finnegan.com

May 28, 2010

VIA HAND DELIVERY

The Honorable Marilyn Abbott
Secretary
U.S. International Trade Commission
500 E Street, S.W.
Washington, D.C. 20436

Re: *Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software*

Dear Secretary Abbott:

Enclosed for filing on behalf of Complainants S3 Graphics Co., Ltd., and S3 Graphics, Inc. (collectively "S3G" or "Complainants") are the following documents in support of S3G's request that the Commission commence an investigation pursuant to Section 337 of the Tariff Act of 1930, as amended. A separate request for confidential treatment of Confidential Exhibits Nos. 19C-34C, is included with this filing.

Accordingly, S3G submits the following documents for filing:

1. An original and twelve (12) copies of the verified Complaint and an original and six (6) copies of the accompanying exhibits, with the Confidential Exhibits segregated from the other material submitted (original and (1) copy unbound, without tabs (Rules 201.6(c), 210.4(f)(3)(i), and 210.8(a));

2. One (1) additional copy of both the Complaint and accompanying non-confidential exhibits for service upon the proposed respondent. (Rules 210.4 (f)(3)(i), 210.8(a), and 210.11(a));

3. One (1) additional copy of the Confidential Exhibits;

4. Certified copies of United States Letters Patent Nos. 7,043,087 ("the '087 patent"), 6,775,417 ("the '417 patent"), and 6,683,978 ("the '978 patent"), included as Exhibits 1-3 in the original Complaint, copies thereof included as Exhibits 1-3 in all copies of the Complaint, and copies of United States

Letters Patent 6,658,146 ("the '146 patent), included as Exhibit 4 (collectively the "Asserted Patents"), (S3G has not yet obtained a certified copy of the '146 patent, but will supplement this filing with a certified copy of the '146 patent and copies thereof upon receipt);

5. Certified copies of the assignments involving the '087, '417, '978, and '146 patents, are included as Exhibit 5 in the original Complaint, and copies thereof included as Exhibit 5 in all copies of the Complaint;

6. Certified copies and three (3) copies thereof of the prosecution histories of each of the '087, '417, and '978 patents, included as Appendices A-C (Rule 210.12(c)(1)) and a copy of the prosecution history of the '146 patent as Appendix D (S3G has not yet obtained a certified copy of the prosecution history for the '146 patent, but will supplement this filing with a certified copy of the prosecution history of the '146 patent upon receipt);

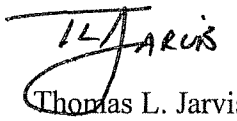
7. Four (4) copies of each reference document mentioned in the prosecution histories of the applications leading to the issuance of the Asserted Patents included as Appendices E-H (Rule 210.12(c)(2));

8. Physical samples of products-in-issue included as Physical Exhibits 1-7C;

9. A letter and certification pursuant to Commission Rules 201.6(b) and 210.5(d) requesting confidential treatment of confidential Exhibits Nos. 19C-34C and 7C.

Thank you for your attention to this matter.

Respectfully submitted,



Thomas L. Jarvis

Enclosures

THOMAS L. JARVIS
202.408.4093
tom.jarvis@finnegan.com

May 28, 2010

VIA HAND DELIVERY

The Honorable Marilyn Abbott
Secretary
U.S. International Trade Commission
500 E Street, S.W.
Washington, D.C. 20436

Re: *Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software*

Dear Secretary Abbott:

This firm represents Complainants S3 Graphics Co., Ltd., and S3 Graphics, Inc. (collectively "S3G" or "Complainants"), who are concurrently filing a complaint pursuant to Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337.

In accordance with Commission Rules 201.6, 210.5, 19 C.F.R. §§ 201.6, and 210.5, Complainants request confidential treatment of the confidential business information contained in Confidential Exhibit Nos. 19C-34C and 7C.

The information for which confidential treatment is sought is proprietary commercial information not otherwise publicly available. Specifically, Confidential Exhibits 19C-34C contain proprietary commercial information concerning Complainants' products, licensing of the Asserted Patents, and investments in the domestic industry.

The information described above qualifies as confidential business information pursuant to Rule 210.6(a) because:

1. it is not available to the public;

2. unauthorized disclosure of such information could cause substantial harm to the competitive position of Complainants; and

3. the disclosure of which could impair the Commission's ability to obtain information necessary to perform its statutory function.

Please contact me if you have any questions about this request, or if this request is not granted in full.

We appreciate your assistance in this matter.

Respectfully submitted,

Thomas L. Jarvis

Enclosures

Washington, DC

Subscribed and sworn to me this 28th day of May, 2010.

Notary Public

My commission expires: November 30, 2014

(SEAL)

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

In the Matter of	
CERTAIN ELECTRONIC DEVICES WITH IMAGE PROCESSING SYSTEMS, COMPONENTS THEREOF, AND ASSOCIATED SOFTWARE	**Investigation No. 337-TA-____**

COMPLAINT OF S3 GRAPHICS CO., LTD. AND S3 GRAPHICS, INC. UNDER SECTION 337 OF THE TARIFF ACT OF 1930, AS AMENDED

COMPLAINANT

S3 Graphics Co., Ltd.
2nd Fl., Zephyr House
Mary St., P.O. Box 709
Grand Cayman
Grand Cayman Islands
British West Indies
Telephone: (510) 683-3300

S3 Graphics, Inc.
1025 Mission Court
Fremont, CA 94539
Telephone: (510) 683-3300

Counsel for Complainant:

Thomas L. Jarvis
Thomas W. Winland
John R. Alison
Paul C. Goulet
John M. Williamson
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, LLP
901 New York Avenue, N.W.
Washington, D.C. 20001-4413
Telephone: (202) 408-4000
Facsimile: (202) 408-4400

PROPOSED RESPONDENT

Apple Inc., a/k/a Apple Computer, Inc.
1 Infinite Loop
Cupertino, CA 95014
Telephone: (408) 996-1010

TABLE OF CONTENTS

TABLE OF EXHIBITS

Exh.	Document
Exh. 18(G)	Fenney, "Texture Compression using Low-Frequency Signal Modulation"
Exh. 18(H)	3D graphics decompression source code, "PVRTDecompress.cpp"
Exh. 18(I)	Apple document entitled, "iPhone Development Guide"
Exh. 18(J)	Apple webpage containing technical specifications of MacBook models
Exh. 18(K)	Technical specifications of iMac
Exh. 18(L)	Technical specifications of Mac Pro
Exh. 18(M)	Technical specifications of Mac mini
Exh. 18(N)	Apple document entitled, "Image I/O Programming Guide"
Exh. 18(O)	The TIFF standard, revision 6.0
Exh. 18(P)	Apple webpage entitled "iPhone OS Overview"

Confidential Exhs.	Document
Exh. 19C	Identification of Licensees
Exh. 20C	S3G Domestic Industry claim chart for U.S. Patent No. 7,043,087
Exh. 21C	S3G Domestic Industry claim chart for U.S. Patent No. 6,775,417
Exh. 22C	S3G Domestic Industry claim chart for U.S. Patent No. 6,683,978
Exh. 23C	S3G Domestic Industry claim chart for U.S. Patent No. 6,658,146
Exh. 24C	Exemplary S3G licensee Domestic Industry claim chart for U.S. Patent No. 7,043,087
Exh. 25C	Exemplary S3G licensee Domestic Industry claim chart for U.S. Patent No. 6,775,417
Exh. 26C	Exemplary S3G licensee Domestic Industry claim chart for U.S. Patent No. 6,683,978
Exh. 27C	Exemplary S3G licensee Domestic Industry claim chart for U.S. Patent No. 6,658,146
Exh. 28C	S3G investments in engineering, research, and development
Exh. 29C	S3G investments in labor and capital
Exh. 30C	S3G investments in plant and equipment

Exh. 31C	S3G investment in licensing
Exh. 32C	Domestic Industry Investments of licensees
Exh. 32C (A)	Exemplary S3G licensee's Form 10-K for the Fiscal Year Ended June 30, 2009
Exh. 33C (A)	Developer documentation related to compression technology
Exh. 33C (B)	Developer documentation related to compression technology
Exh. 33C (C)	Developer documentation related to compression technology
Exh. 33C (D)	Developer documentation related to compression technology
Exh. 33C (E)	Developer documentation related to compression technology
Exh. 33C (F)	Developer documentation related to compression technology
Exh. 33C (G)	Developer documentation related to compression technology
Exh. 33C (H)	Developer documentation related to compression technology
Exh. 33C (I)	Confidential S3 architecture specification
Exh. 33C (J)	Confidential S3 source code
Exh. 33C (K)	Confidential S3 source code
Exh. 33C (L)	Confidential S3 product overview
Exh. 33C (M)	Confidential S3 source code
Exh. 34C	Photograph of Confidential Physical Exhibit 7C and screenshot of exemplary S3G license's software development kit ("SDK") and sample texture file

Physical Exhs.	
Physical Exh. 1	Apple iPhone (in box with packaging)
Physical Exh. 2	Apple iPad (in box with packaging)
Physical Exh. 3	Apple iPod Touch (in box with packaging)
Physical Exh. 4	Apple MacBook Pro (in box with packaging)
Physical Exh. 5	Domestic Industry Exhibit (S3G Chrome)

Physical Exhs.

Physical Exh. 6	Compact disc containing three software applications for the Apple iPhone

Confidential Physical Exhs.

Physical Exh. 7C	Compact disc containing exemplary S3G licensee's Software Development Kit and texture file

APPENDICES

Appendix	Document
App. A	Certified copy of the prosecution history of U.S. Patent No. 7,043,087 and three copies thereof
App. B	Certified copy of the prosecution history of U.S. Patent No. 6,775,417 and three copies thereof
App. C	Certified copy of the prosecution history of U.S. Patent No. 6,683,978 and three copies thereof
App. D	Copy of the prosecution history of U.S. Patent No. 6,658,146 and three copies thereof
App. E	Four copies of each technical reference identified in the prosecution history of U.S. Patent No. 7,043,087
App. F	Four copies of each technical reference identified in the prosecution history of U.S. Patent No. 6,775,417
App. G	Four copies of each technical reference identified in the prosecution history of U.S. Patent No. 6,683,978
App. H	Four copies of each technical reference identified in the prosecution history of U.S. Patent No. 6,658,146

Confidential Appendix	Document
Conf. App. I	Three copies of each known current license involving the Asserted Patents

I. INTRODUCTION

1. This Complaint is filed by S3 Graphics, Inc. and S3 Graphics Co, Ltd. (collectively, "S3G") under Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, based on the unlawful importation into the United States, the sale for importation, and the sale within the United States after importation, by proposed Respondent Apple Inc., ("Apple") of certain electronic devices with image processing systems, and components thereof, and associated software that infringe one or more of claims 1, 6, or 7 of United States Patent No. 7,043,087 ("the '087 patent"); one or more of claims 1, 7, 8, 12, 13, 15 or 23 of United States Patent No. 6,775,417 ("the '417 patent"); one or more of claims 11, 14, or 16 of United States Patent No. 6,683,978 ("the '978 patent"); and one or more of claims 2, 4, 8, 13, 16, 18, or 19 of United States Patent No. 6,658,146 ("the '146 patent") (collectively, the "Asserted Claims" of the "Asserted Patents").

2. Certified copies of the Asserted Patents are attached as Exhibit Nos. 1 through 4, respectively.[1] S3 Graphics Co., Ltd., owns all right, title, and interest in each of the Asserted Patents. S3 Graphics, Inc., a wholly owned subsidiary of S3 Graphics Co. Ltd., holds a nonexclusive license, with a right to grant sublicenses, to the Asserted Patents. (Confidential Appendix I). Certified copies of recorded assignments demonstrating the chain of title of the Asserted Patents are attached as Exhibit No. 5.

3. The proposed respondent is Apple Inc. The Accused Products are certain electronic devices with image processing systems, components thereof, and associated software including, but not limited to multimedia devices, smart phones, personal computers, and software for use

[1] S3G has not yet obtained a certified copy of the '146 patent. Exhibit No. 4, therefore, is not a certified copy of the '146 patent. S3G will supplement Exhibit No. 4 with a certified copy of the '146 patent upon receipt.

with such devices (collectively the "Accused Products"). Examples of the Accused Products are the Apple iPod Touch, iPhone, iPad, Apple computers such as the MacBook used in conjunction with an Apple software development kit ("SDK"), and other application software. The Accused Products are imported into the United States and sold after importation into the United States by Apple.

4. An industry as required by 19 U.S.C. § 1337(a)(2) and (3) exists in the United States relating to the technology protected by the Asserted Patents.

5. As set forth more fully in paragraph 119, S3G seeks as relief, a permanent exclusion order barring from entry into the United States all infringing Apple electronic devices with image processing systems, components thereof, and associated software sold for importation into the United States, imported, or sold after importation. S3G also seeks, as relief, a cease and desist order prohibiting Apple's sale for importation into the United States, importation, sale after importation into the United States, offer for sale, solicitation of sales, advertising, testing, technical support and other commercial activity related to Apple electronic devices with image processing systems, components thereof, and/or associated software that infringe one or more Asserted Claims of the Asserted Patents.

II. COMPLAINANTS

6. S3 Graphics, Inc., is a Delaware corporation with its principal place of business at 1025 Mission Court, Fremont, CA 94539. S3 Graphics Co., Ltd. is a Cayman Islands corporation with its principal place of business at 2nd Fl., Zephyr House, Mary St., P.O. Box 709, Grand Cayman, Grand Cayman Islands, British West Indies. S3 Graphics Co., Ltd. holds all right, title, and interest in the Asserted Patents. (Exhibit No. 5). S3G provides innovative graphics visualization technologies and GPU (graphics processing unit) products for mobile devices, desktop computers, and embedded systems.

7. S3G's image processing technologies enable coding of image attributes into data files that can be more efficiently stored and later displayed. Many software developers use S3G image processing technology to convert very large color image data files, particularly animated (motion) images, into compressed data files that can be efficiently distributed to and displayed by end users of the software. For example, video games typically implement life-like animation by the rapid display of a sequence of progressively modified still images to achieve the illusion of movement. Game developers can use S3G's image processing technology to encode the image data into compressed formats that are convenient for distribution and can be decoded and displayed by consumers. S3G's image processing technology is licensed by some of the largest computer hardware and software companies in the world.

8. S3G engages in research, development, engineering, and product design activities at S3 Graphics, Inc.'s principal place of business in Fremont, California including research, development, and product design for products utilizing S3G image compression technology, including the S3G Chrome series graphics products.

9. S3G operates a licensing business from S3 Graphics, Inc.'s principal place of business in Fremont, California that includes formulation of licensing strategies, identification of products and companies that currently do, or prospectively could, utilize S3G image processing technology, analyzing those products and companies for potential licensing opportunities, negotiating licenses under the S3G patent portfolio, and monitoring and enforcing compliance with those licenses and S3G patent rights.

10. On information and belief, S3G's licensees conduct in the United States certain research, development, engineering, manufacturing, and technical support of products with S3G image processing technology.

III. PROPOSED RESPONDENT

11. On information and belief, respondent Apple Inc. is a corporation organized under the laws of the State of California with its principal place of business at 1 Infinite Loop, Cupertino, CA 95014. (Exhibit No. 6).

12. On information and belief, Apple is involved in the design, development, manufacture, sale for importation, importation, and sale after importation of the Accused Products. Further, on information and belief, Apple performs several services to support the importation and sale of Accused Products into and within the United States, including marketing of the Accused Products, repair of the Accused Products, technical support, and other after-sale services, such as supporting and configuring the Accused Products, as well as interfacing with U.S.-based customers and distributors to conform the Accused Products to purchaser requests.

IV. THE TECHNOLOGY AND PRODUCTS AT ISSUE

13. The technologies at issue relate generally to apparatuses, methods, and data formats for encoding and decoding, including compressing image data, storing of compressed image data, and decompressing of such data. The Asserted Patents generally relate to aspects of an image processing system for encoding and decoding, including compressing image data files into a more compact form, a format for storing that compressed data, and a system for decompressing that data for display as an image.

14. The Asserted Patents disclose an image compression technology including an image decomposer, an encoder for computing image data values and generating codeword reference values, and a construction module for creating indices that map each image data value to a set of colors generated from the codewords. The resulting codewords and indices form an encoded image block.

15. The Asserted Patents also disclose a format for storage of encoding or compressing image data that includes a portion for storage of multiple codewords from which a set of colors can be computed and a portion for storage of indices for mapping pixel color to a computed color.

16. The Asserted Patents also disclose an image data decoding or decompressing technology that includes a decomposer for processing the encoded image data stream into a header and a plurality of encoded image bocks, a header converter for generating an output image header, one or more block data decoders for generating from the codewords and indices pixel image attributes such as color and for mapping those attributes to pixels, and an image composer that reassembles data blocks for a display device and/or a data file.

17. On information and belief, Apple provides an SDK specifically adapted for use with Apple computers to compress and decompress image data files using the technology disclosed and claimed in the Asserted Patents.

18. On information and belief, Apple's SDK and computers generate encoded image files in the format disclosed and claimed in the Asserted Patents.

19. On information and belief, Apple sells a variety of imported products, including the Apple iPod Touch, iPhone, iPad, Apple computers such as the MacBook, certain applications for those products, and associated software that incorporate the image data compression, decompression, and/or data format disclosed and claimed in the Asserted Patents.

20. The identification of a specific model, trade name, or type of electronic device with image processing systems and/or the identification of specific software or components is not intended to limit the scope of this Investigation. The remedy sought in this Complaint should

extend to all infringing electronic devices with image processing systems, components thereof, and associated software.

V. THE ASSERTED PATENTS AND NON-TECHNICAL DESCRIPTION OF THE INVENTIONS

A. Four Patents from a Single Original Application

21. On October 2, 1997, S3 Incorporated (a predecessor company to S3G) filed United States Patent Application Serial Number. 08/942,860 ("U.S. Pat. App. Ser. No. 08/942,860"). From that single original application, through continuation and continuation-in-part applications, all four of the patents at issue in this investigation were issued.

B. U.S. Patent No. 7,043,087

1. Identification and Ownership of the '087 Patent

22. United States Patent No. 7,043,087, entitled "Image Processing System," issued on May 9, 2006, to inventors Zhou Hong, Konstantine I. Iourcha, and Krishna S. Nayak. (Exhibit No. 1). The '087 patent issued from Application No. 10/893,084, filed on July 16, 2004, that claims priority from the original U.S. Pat. App. Ser. No. 08/942,860. *Id.*

23. The '087 patent has 1 independent claim and 7 dependent claims. S3G is asserting claims 1, 6, and 7 of the '087 patent in this Investigation.

24. The Asserted Claims of the '087 patent are valid, enforceable, and currently in full force and effect until its expiration on October 2, 2017.

25. S3 Graphics Co., Ltd., owns by assignment the entire right, title, and interest in and to the '087 patent. (Exhibit No. 5).

26. Pursuant to Commission Rule 210.12(c), this Complaint is accompanied by a certified copy of the prosecution history of the '087 patent and three copies thereof.

(Appendix A). Further, this Complaint is accompanied by four copies of each technical reference identified in the prosecution history of the '087 patent (Appendix E).

2. Non-Technical Description of the Invention Claimed in the '087 Patent

27. The '087 patent discloses aspects of an image processing system for encoding and decoding image data, including compressing image data files into a more compact form, a format for storing that compressed data, and a system for decoding and/or decompressing that data for display as an image and/or for storage. Asserted Claims 1, 6, and 7 of the '087 patent are directed to aspects of an engine for decoding image data files. A nontechnical description of that decoding engine is that it includes: (a) a decomposer for converting encoded image data files into a modified header and at least one encoded or compressed image block, where each image block is associated with at least one codeword and index values for a plurality of pixels; (b) at least one block decoder for decoding or decompressing image blocks by generating a set of quantized image data values and mapping the index value to one of the quantized image data values from the set of quantized image data values; and (c) at least one decoder configured for decoding or decompressing each of the image blocks. This nontechnical description does not limit or interpret the claims of the '087 patent.

3. Foreign Counterparts

28. The foreign patents and patent applications reported as related to the '087 patent are identified in Exhibit No. 7. On information and belief, no other foreign applications or patents corresponding to the '087 patent have been filed, abandoned, or rejected.

4. Licenses

29. As required under Commission Rule 210.12(a)(9)(iii), a list of licensed entities is attached to this Complaint as Confidential Exhibit No. 19C. On information and belief, there are no other current licenses involving the '087 patent.

C. U.S. Patent No. 6,775,417

1. Identification and Ownership of the '417 Patent

30. United States Patent No. 6,775,417 (the "'417 patent"), entitled "Fixed-Rate Block-Based Image Compression with Inferred Pixel Values," issued on August 10, 2004, to inventors Zhou Hong, Konstantine I. Iourcha, and Krishna S. Nayak. (Exhibit No. 2). The '417 patent issued from Application No. 10/052,613, filed on January 17, 2002, that claims priority from the original U.S. Pat. App. Ser. No. 08/942,860. *Id.*

31. The '417 patent has 8 independent claims and 22 dependent claims. S3G is asserting claims 1, 7, 8, 12, 13, 15 and 23 of the '417 patent in this Investigation.

32. The Asserted Claims of the '417 patent are valid, enforceable, and currently in full force and effect until its expiration on March 16, 2018.

33. S3 Graphics Co., Ltd., owns by assignment the entire right, title, and interest in and to the '417 patent. (Exhibit No.5).

34. Pursuant to Commission Rule 210.12(c), this Complaint is accompanied by a certified copy of the prosecution history of the '417 patent and three copies thereof. (Appendix B). Further, this Complaint is accompanied by four copies of each technical reference identified in the prosecution history of the '417 patent (Appendix F).

2. Non-Technical Description of the Invention of the '417 Patent

35. The '417 patent discloses aspects of an image processing system for encoding and decoding image data, including compressing image data files into a more compact form, a format