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CLERK U.S. DISTRICT COURT
CENTRAL DIST. OF CALIF.
LOS ANGELES

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ATTORNEYS FOR PLAINTIFF
CALIFORNIA INSTITUTE OF TECHNOLOGY

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA, WESTERN DIVISION

CV10 9099 GAF (JEMx)

CALIFORNIA INSTITUTE OF TECHNOLOGY

Plaintiff,

VS.

STMICROELECTRONICS NV, STMICROELECTRONICS, INC., SETI CO., LTD., SILICONFILE TECHNOLOGIES, INC., TOSHIBA CORP., TOSHIBA AMERICA ELECTRONIC COMPONENTS,

CASE NO.

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

INC., LG ELECTRONICS, INC., LG ELECTRONICS MOBILECOMM U.S.A., INC., LG ELECTRONICS U.S.A., INC., NOKIA CORP., NOKIA, INC., PANTECH CO., LTD., AND PANTECH WIRELESS, INC.

Defendants.

Plaintiff California Institute of Technology brings this action for patent infringement against STMicroelectronics NV; STMicroelectronics, Inc.; SETi Co., Ltd.; Siliconfile Technologies, Inc.; Toshiba Corp.; Toshiba America Electronic Components, Inc.; LG Electronics, Inc.; LG Electronics Mobilecomm U.S.A., Inc.; LG Electronics U.S.A., Inc.; Nokia Corp.; Nokia, Inc.; Pantech Co., Ltd.; and Pantech Wireless, Inc. (collectively, "Defendants") as follows:

I. JURISDICTION AND VENUE

1. This is an action for patent infringement arising under the patent laws of the United States, Title 35, United States Code. The Court's jurisdiction is proper under the above statutes, including 35 U.S.C. § 271 *et. seq.*, and 28 U.S.C. §§ 1331 and 1338(a).

2. This Court has personal jurisdiction over each Defendant. Each Defendant has conducted and does conduct business within the State of California. Each Defendant, directly or through intermediaries (including distributors, retailers, and others), ships, distributes, offers for sale, and sells its products in the United States, the State of California, and the Central District of California. Each Defendant has purposefully and voluntarily placed one or more of its infringing products, as described below, into the stream of commerce with the expectation that they will be purchased by consumers in the Central District of California. These infringing products have been and continue to be purchased by consumers in the Central District of California. Each Defendant has committed the tort of patent

infringement within the State of California and, more particularly, within the Central District of California.

3. Venue is proper in this district under 28 U.S.C. §§ 1391(b), (c), and/or (d), as well as 28 U.S.C. § 1400(b).

II. THE PARTIES

4. Plaintiff California Institute of Technology ("Caltech") is a private university having a principal address of 1200 East California Boulevard, Pasadena, California 91125.

5. Upon information and belief, Defendant STMicroelectronics NV is organized under the laws of the Netherlands with its principal place of business at 39 Chemin du Champ des Filles, C. P. 21, CH 1228 Plan-Les-Ouates, Geneva, Switzerland.

3. Upon information and belief, Defendant STMicroelectronics, Inc. is a Delaware corporation with its principal place of business at 1310 Electronics Dr., Carrollton, Texas 75006. STMicroelectronics, Inc. is registered to do business in California, Filing No. C1012786, and has designated CT Corporation System, 818 W. 7th St., Los Angeles, California 90017, as its agent for service of process. STMicroelectronics, Inc. is a wholly owned subsidiary of STMicroelectronics NV.

4. Collectively, STMicroelectronics NV and STMicroelectronics, Inc. are referred to as "STMicroelectronics."

5. Upon information and belief Defendant SETi Co., Ltd. ("SETi") is organized under the laws of the Republic of Korea with its principal place of business at 3F, Leaders Bldg. 342-1, Yatap-Dong, Bun dang- Gu Sungam-Shi, Gyeounggi-Do, Republic of Korea.

6. Upon information and belief Defendant Siliconfile Technologies, Inc. ("Siliconfile") is organized under the laws of the Republic of Korea with its principal place of business at 9F, Yewon Bldg., 75-1, Yangjae-Dong, Seocho-Gu, Seoul, Republic of Korea.

7. Upon information and belief, Defendant Toshiba Corp. is organized under the laws of Japan with its principal place of business at 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan.

8. Upon information and belief, Defendant Toshiba America Electronic Components, Inc. is a California corporation with its principal place of business at 19900 Mac Arthur Blvd., Suite 400, Irvine, California 92612-2443. Toshiba America Electronic Components, Inc. is registered to do business in California, Filing No. CA02028433, and has designated CT Corporation System, 818 W. 7th Street, Los Angeles, California 90017, as its agent for service of process.

9. Collectively, Toshiba Corp. and Toshiba America Electronic Components, Inc. are referred to as "Toshiba."

10. Upon information and belief, Defendant LG Electronics, Inc. is a corporation organized under the laws of the Republic of Korea with its principal place of business at LG Twin Towers, 20 Yeouido-dong, Yeoungdeungpo-gu, Seoul, 150-7-21, Republic of Korea.

11. Upon information and belief, Defendant LG Electronics Mobilecomm U.S.A., Inc. is a subsidiary of Defendant LG Electronics, Inc. and is a California corporation within its principal place of business at 1010 Old Grove Road, San Diego, California 92131. LG Electronics Mobilecomm U.S.A., Inc. is registered to do business in California, Filing No. CA01972973, and has designated Alan K. Tse, 10101 Old Grove Road, San Diego, California 92131 as its agent for service of process.

12. Upon information and belief, Defendant LG Electronics U.S.A., Inc. is a subsidiary of Defendant LG Electronics, Inc. and is a Delaware corporation with its principal place of business at 1000 Sylvan Avenue, Englewood Cliffs, New Jersey 07632. LG Electronics U.S.A., Inc. is registered to do business in California, Filing No. CA01061050, and has designated CSC – Lawyers Incorporating Service, 2730 Gateway Oaks Drive, Suite 100, Sacramento, California 95833 as its agent for

service of process.

13. Collectively, LG Electronics, Inc.; LG Electronics Mobilecomm U.S.A., Inc.; and LG Electronics U.S.A., Inc. are referred to as "LG."

14. Upon information and belief, Defendant Nokia Corp. is incorporated under the laws of Finland and has its principal place of business at Keilalahdenti 4, Espoo, Finland.

15. Upon information and belief, Defendant Nokia, Inc. is a Delaware corporation with its principal place of business at 102 Corporate Park Drive, White Plains, New York 10604. Nokia, Inc. is registered to do business in California, Filing No. C1916566, and has designated National Registered Agents, Inc., 2875 Michelle Dr., Ste. 100, Irvine, California 92606 as its agent for service of process.

16. Collectively, Nokia Corp. and Nokia, Inc. are referred to as "Nokia."

17. Upon information and belief, Defendant Pantech Co., Ltd. is incorporated under the laws of the Republic of Korea and has its principal place of business at Pantech R&D Center, 1-2 DMC Sangam-dong, Mapo-gu, Seoul, Republic of Korea.

18. Upon information and belief, Defendant Pantech Wireless, Inc. is a Georgia corporation with its principal place of business 5607 Glenridge Drive, Suite 500, Atlanta, Georgia 30342 and has designated Kathleen Jones as its agent for service of process who resides at the same address.

19. Collectively, Pantech Co., Ltd. and Pantech Wireless, Inc. are referred to as "Pantech."

III. PATENTS-IN-SUIT

23. On November 23, 1999, the United States Patent and Trademark Office ("USPTO") issued U.S. Patent No. 5,990,506 entitled "Active Pixel Sensors with Substantially Planarized Color Filtering Elements" (hereinafter "the '506 patent"). A true and correct copy of the '506 patent is attached hereto as Exhibit A.

24. On September 24, 2002, the USPTO issued U.S. Patent No. 6,456,326

entitled "Single Chip Camera Having Double Sampling Operation" (hereinafter "the '326 patent"). A true and correct copy of the '326 patent is attached hereto as Exhibit B.

25. On April 15, 2003, the USPTO issued U.S. Patent No. 6,549,235 entitled "Single Substrate Camera Device with CMOS Image Sensor" (hereinafter "the '235 patent"). A true and correct copy of the '235 patent is attached hereto as Exhibit C.

26. On August 12, 2003, the USPTO issued U.S. Patent No. 6,606,122 entitled "Single Chip Camera Active Pixel Sensor" (hereinafter "the '122 patent"). A true and correct copy of the '122 patent is attached hereto as Exhibit D.

27. On April 29, 2004, the USPTO issued U.S. Patent No. 6,555,842 entitled "Active Pixel Sensor with Intra-pixel Charge Transfer" (hereinafter "the '842 patent"). A true and correct copy of the '842 patent is attached hereto as Exhibit E.

28. On May 27, 2003, the USPTO issued U.S. Patent No. 6,570,617 entitled "CMOS Active Pixel Sensor Type Imaging System on a Chip" (hereinafter "the '617 patent"). A true and correct copy of the '617 patent is attached hereto as Exhibit F.

29. On June 1, 2004, the USPTO issued U.S. Patent No. 6,744,068 entitled "Active Pixel Sensor with Intra-pixel Charge Transfer" (hereinafter "the '068 patent"). A true and correct copy of the '068 patent is attached hereto as Exhibit G.

30. On September 13, 2005, the USPTO issued U.S. Patent No. 6,943,838 entitled "Active Pixel Sensor Pixel Having a Photodetector Whose Ouptut is Coupled to an Output Transistor Gate" (hereinafter "the '838 patent"). A true and correct copy of the '838 patent is attached hereto as Exhibit H.

31. On May 6, 2008, the USPTO issued U.S. Patent No. 7,369,166 entitled "Single Substrate Camera Device With CMOS Image Sensor" (hereinafter "the '166 patent"). A true and correct copy of the '166 patent is attached hereto as Exhibit I.

32. Collectively, the '506 patent, the '326 patent, the '235 patent, the '122 patent, the '842 patent, the '617 patent, the '068 patent, the '838 patent, and the '166 patent are referred to as "the Caltech patents."

33. Caltech is the owner of all right, title, and interest in and to the Caltech patents by assignment, with full right to bring suit to enforce each of the patents, including the right to recover for past infringement damages.

IV. PATENT INFRINGEMENT

34. Caltech repeats and re-alleges the allegations in paragraphs 1- 33 as though fully set forth herein.

35. The Caltech patents are valid and enforceable.

36. All requirements under 35 U.S.C. § 287 have been satisfied with respect to the Caltech patents.

37. STMicroelectronics has been and is infringing the Caltech patents, either literally or under the doctrine of equivalents, by making, using, selling, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of the claims of the Caltech patents, including but not limited to the products bearing the following identification numbers: S852AC, VS6556AA, S724BA, S725BA, S871AA, and S851BA.

38. STMicroelectronics has been and is continuing to induce infringement of the Caltech patents under 35 U.S.C. § 271(b) and contributes to the infringement of the Caltech patents under 35 U.S.C. § 271(c), in conjunction with such acts of making, using, offering for sale, and/or importing in or into the United States, without authority, instrumentalities that fall within the scope of one or more claims of each of the Caltech patents. STMicroelectronics contributes to and induces the direct infringement of the Caltech patents by manufacturers and distributors, including, but not limited to Nokia, who make, use, sell, offer for sale, and/or import instrumentalities in or into the United States that fall within the scope of the claims of the Caltech patents. The infringing instrumentalities have no substantial non-

infringing uses.

39. STMicroelectronics had and continues to have actual knowledge of or a deliberate disregard for the known risk of the Caltech patents and their coverage of STMicroelectronics's infringing instrumentalities, but has nonetheless engaged in the infringing conduct. STMicroelectronics's infringement of the Caltech patents was and continues to be willful.

40. SETi has been and is infringing the Caltech patents, either literally or under the doctrine of equivalents, by making, using, selling, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of the claims of the Caltech patents, including but not limited to the products bearing the following identification numbers: SIM120-B4/SETi-1.3M and SIV100/SETi-VGA.

41. SETi has been and is continuing to induce infringement of the Caltech patents under 35 U.S.C. § 271(b) and contributes to the infringement of the Caltech patents under 35 U.S.C. § 271(c), in conjunction with such acts of making, using, offering for sale, and/or importing in or into the United States, without authority, instrumentalities that fall within the scope of one or more claims of each of the Caltech patents. SETi contributes to and induces the direct infringement of the Caltech patents by manufacturers and distributors, including, but not limited to Pantech, who make, use, sell, offer for sale, and/or import instrumentalities in or into the United States that fall within the scope of the claims of the Caltech patents. The infringing instrumentalities have no substantial non-infringing uses.

42. SETi had and continues to have actual knowledge of or a deliberate disregard for the known risk of the Caltech patents and their coverage of SETi's infringing instrumentalities, but has nonetheless engaged in the infringing conduct. SETi's infringement of the Caltech patents was and continues to be willful.

43. Siliconfile has been and is infringing the Caltech patents, either literally or under the doctrine of equivalents, by making, using, selling, offering for sale,

and/or importing in or into the United States, without authority, products that fall within the scope of the claims of the Caltech patents, including but not limited to the products bearing the following identification numbers: NOON130PC20, NOON130PC52, and NOON030PC20.

44. Siliconfile has been and is continuing to induce infringement of the Caltech patents under 35 U.S.C. § 271(b) and contributes to the infringement of the Caltech patents under 35 U.S.C. § 271(c), in conjunction with such acts of making, using, offering for sale, and/or importing in or into the United States, without authority, instrumentalities that fall within the scope of one or more claims of each of the Caltech patents. Siliconfile contributes to and induces the direct infringement of the Caltech patents by manufacturers and distributors, including, but not limited to LG, who make, use, sell, offer for sale, and/or import instrumentalities in or into the United States that fall within the scope of the claims of the Caltech patents. The infringing instrumentalities have no substantial non-infringing uses.

45. Siliconfile had and continues to have actual knowledge of or a deliberate disregard for the known risk of the Caltech patents and their coverage of Siliconfile's infringing instrumentalities, but has nonetheless engaged in the infringing conduct. Siliconfile's infringement of the Caltech patents was and continues to be willful.

46. Upon information and belief, Toshiba has been and is infringing the Caltech patents, either literally or under the doctrine of equivalents, by making, using, selling, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of the claims of the Caltech patents, including but not limited to the products bearing the following identification numbers: HE95, HEJO/NJOV1, HEM2, TA65B, HEF2/NF2V1, A3V3P/HEA3, HEF3A60A/HEF3A56A/HEF3A58A/HEF3A62B, HEK8, HER4, and HEN3A63A.

47. Toshiba has been and is continuing to induce infringement of the Caltech patents under 35 U.S.C. § 271(b) and contributes to the infringement of the

Caltech patents under 35 U.S.C. § 271(c), in conjunction with such acts of making, using, offering for sale, and/or importing in or into the United States, without authority, instrumentalities that fall within the scope of one or more claims of each of the Caltech patents. Toshiba contributes to and induces the direct infringement of the Caltech patents by manufacturers and distributors, including, but not limited to Nokia and LG, who make, use, sell, offer for sale, and/or import instrumentalities in or into the United States that fall within the scope of the claims of the Caltech patents. The infringing instrumentalities have no substantial non-infringing uses.

48. Toshiba had and continues to have actual knowledge of or a deliberate disregard for the known risk of the Caltech patents and their coverage of Toshiba's infringing instrumentalities, but has nonetheless engaged in the infringing conduct. Toshiba's infringement of the Caltech patents was and continues to be willful.

49. LG has been and is infringing the Caltech patents, either literally or under the doctrine of equivalents, by making, using, selling, offering for sale, and/or importing in or into the United States, without authority, products incorporating components that fall within the scope of the claims of the Caltech patents, including but not limited to the mobile devices known as the LG Invision, the LG GU295, the LG Remarq, the LG Cosmos, the LG CE110, the LG VX5500, the LG CF360, the LG Shine, the LG Venus, the LG evV2, the LG Neon, and the LG Chocolate.

50. LG had and continues to have actual knowledge of or a deliberate disregard for the known risk of the Caltech patents and their coverage of LG's infringing instrumentalities, but has nonetheless engaged in the infringing conduct. LG's infringement of the Caltech patents was and continues to be willful.

51. Nokia has been and is infringing the Caltech patents, either literally or under the doctrine of equivalents, by making, using, selling, offering for sale, and/or importing in or into the United States, without authority, products incorporating components that fall within the scope of the claims of the Caltech patents, including but not limited to the products known as the Nokia X3, the Nokia Slide, the Nokia

2680s-2b, the Nokia N90, the Nokia 6085h, the Nokia N97, the Nokia N96, the Nokia N86, and the Nokia 2330.

52. Nokia had and continues to have actual knowledge of or a deliberate disregard for the known risk of the Caltech patents and their coverage of Nokia's infringing instrumentalities, but has nonetheless engaged in the infringing conduct. Nokia's infringement of the Caltech patents was and continues to be willful.

53. Pantech has been and is infringing the Caltech patents, either literally or under the doctrine of equivalents, by making, using, selling, offering for sale, and/or importing in or into the United States, without authority, products incorporating components supplied by one of the other above-captioned Defendants that fall within the scope of the claims of the Caltech patents, including but not limited to the products known as the Pantech Link, the Pantech Matrix, the Pantech CDM8950, the Pantech Razzle, and the Pantech Breeze.

54. Pantech had and continues to have actual knowledge of or a deliberate disregard for the known risk of the Caltech patents and their coverage of Pantech's infringing instrumentalities, but has nonetheless engaged in the infringing conduct. Pantech's infringement of the Caltech patents was and continues to be willful.

55. As a direct and proximate result of Defendants' acts of patent infringement, Caltech has been and continues to be injured and has sustained and will continue to sustain substantial damages.

56. Unless Defendants are enjoined by this Court from continuing their infringement of the Caltech patents, Caltech will suffer additional irreparable harm and impairment of the value of its patent rights.

57. Caltech has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute create an exceptional case within the meaning of 35 U.S.C. § 285, and Caltech is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

//

V. PRAYER FOR RELIEF

Caltech prays for the following relief:

A. A judgment that each Defendant has infringed the Caltech patents as alleged herein, directly and/or indirectly by way of inducing or contributing to infringement of the Caltech patents;

B. A judgment and order requiring each Defendant to pay Caltech damages under 35 U.S.C. § 284, including treble damages for willful infringement as provided by 35 U.S.C. § 284, and supplemental damages for any continuing post-verdict infringement up until entry of the final judgment with an accounting as needed;

C. A judgment and order requiring each Defendant to pay Caltech pre-judgment and post-judgment interest on the damages awarded;

D. A judgment and order finding this to be an exceptional case and requiring each Defendant to pay the costs of this action (including all disbursements) and attorneys' fees as provided by 35 U.S.C. § 285;

E. A preliminary and thereafter a permanent injunction against each Defendant's direct infringement, active inducements of infringement, and/or contributory infringement of the Caltech patents, as well as against each Defendant's agents, employees, representatives, successors, and assigns, and those acting in privity or in concert with them; and

F. In the event a final injunction is not awarded, a compulsory ongoing royalty; and

G. Such other and further relief as the Court deems just and equitable.

VI. JURY DEMAND

Caltech hereby demands that all issues to be determined by jury.

DATED: November 23, 2010

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(*pro hac vice* to be filed)
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(*pro hac vice* to be filed)
DEREK N. JOHNSON
(*pro hac vice* to be filed)
TIMOTHY T. WANG
(*pro hac vice* to be filed)

SCHEPER KIM & HARRIS LLP
MARC S. HARRIS
ALEXANDER H. COTE

By: Marc S Harris by AHC
Marc S. Harris
Attorneys for Plaintiff
CALIFORNIA INSTITUTE OF TECHNOLOGY

EXHIBIT A

US005990506A

United States Patent [19]

Fossum et al.

[11] Patent Number: 5,990,506

[45] Date of Patent: Nov. 23, 1999

[54] **ACTIVE PIXEL SENSORS WITH SUBSTANTIALLY PLANARIZED COLOR FILTERING ELEMENTS**

[75] Inventors: **Eric R. Fossum; Sabrina E. Kemeny,** both of La Crescenta, Calif.

[73] Assignee: **California Institute of Technology,** Pasadena, Calif.

[21] Appl. No.: **08/821,157**

[22] Filed: **Mar. 20, 1997**

Related U.S. Application Data

[60] Provisional application No. 60/013,700, Mar. 20, 1996.

[51] **Int. Cl.**[6] **H01L 21/339**

[52] **U.S. Cl.** **257/294**; 257/222; 257/225; 257/226; 257/227; 257/228; 257/232; 257/233; 257/234; 257/290; 257/291; 257/292; 257/293; 257/294; 250/14; 250/27; 250/357; 250/365

[58] **Field of Search** ..... 257/222, 225, 257/226, 227, 228, 232, 233, 234, 290–293, 239 W, 294; 349/78–80, 97, 104–109; 250/14, 27, 357, 365

[56] **References Cited**

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5,412,705	5/1995	Snoeren et al.	250/487.1
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5,541,402	7/1996	Ackland et al.	250/208
5,576,763	11/1996	Ackland	348/308
5,654,202	8/1997	Daly et al.	430/70
5,656,202	8/1997	Daly et al.	438/70

OTHER PUBLICATIONS

Fossum et al. Application of the Active Pixel Sensor Concept to Guidance and Navigation, SPIE, vol. 1949 paper 30 (1993).

Mendis et al., CMOS Active Pixel Image Sensor, IEEE Transactions on Electrons Devices, 41(3) 452–453.

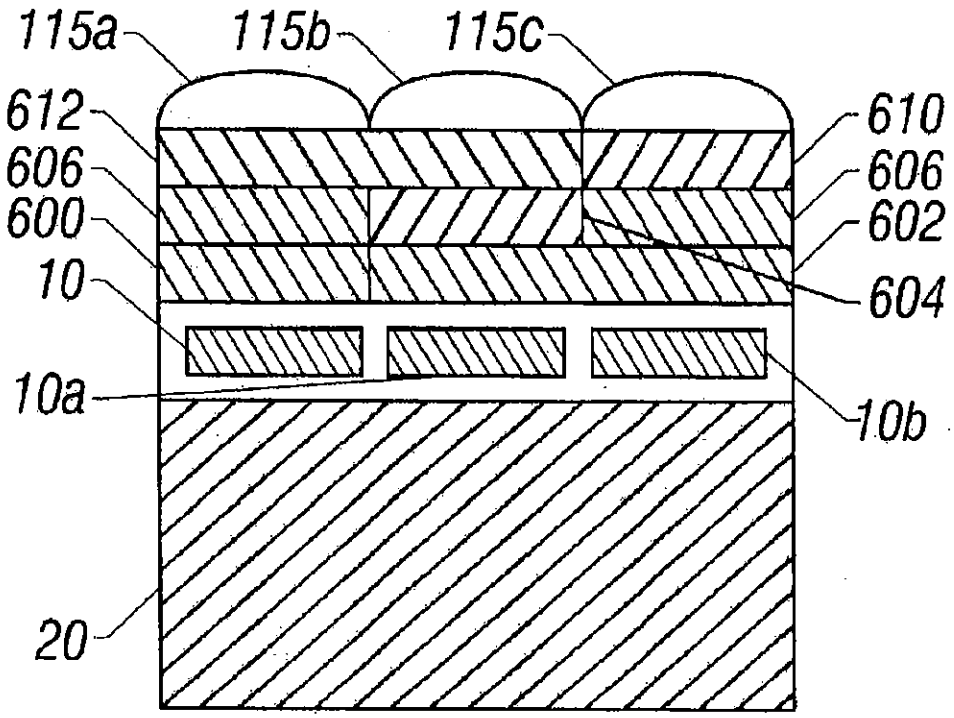
Mendis et al., Progress in CMOS Active Pixel Image Sensors, SPIE vol. 2172:1–11 (1994).

Primary Examiner—Fetsum Abraham
Attorney, Agent, or Firm—Fish & Richardson P.C.

[57] **ABSTRACT**

A semiconductor imaging system preferably having an active pixel sensor array compatible with a CMOS fabrication process. Color-filtering elements such as polymer filters and wavelength-converting phosphors can be integrated with the image sensor.

19 Claims, 5 Drawing Sheets



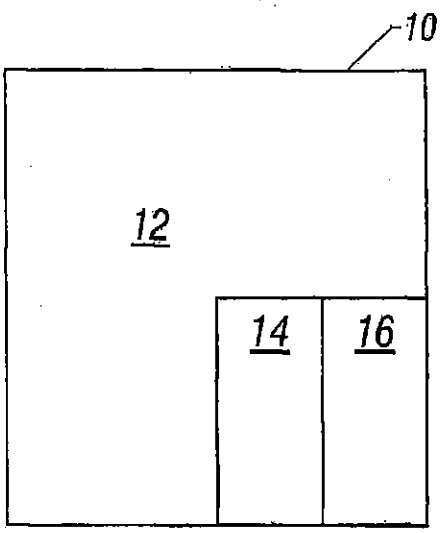


FIG. 1

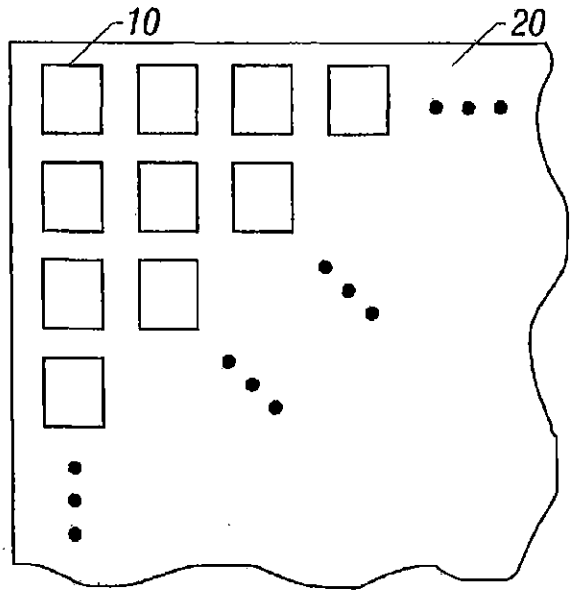
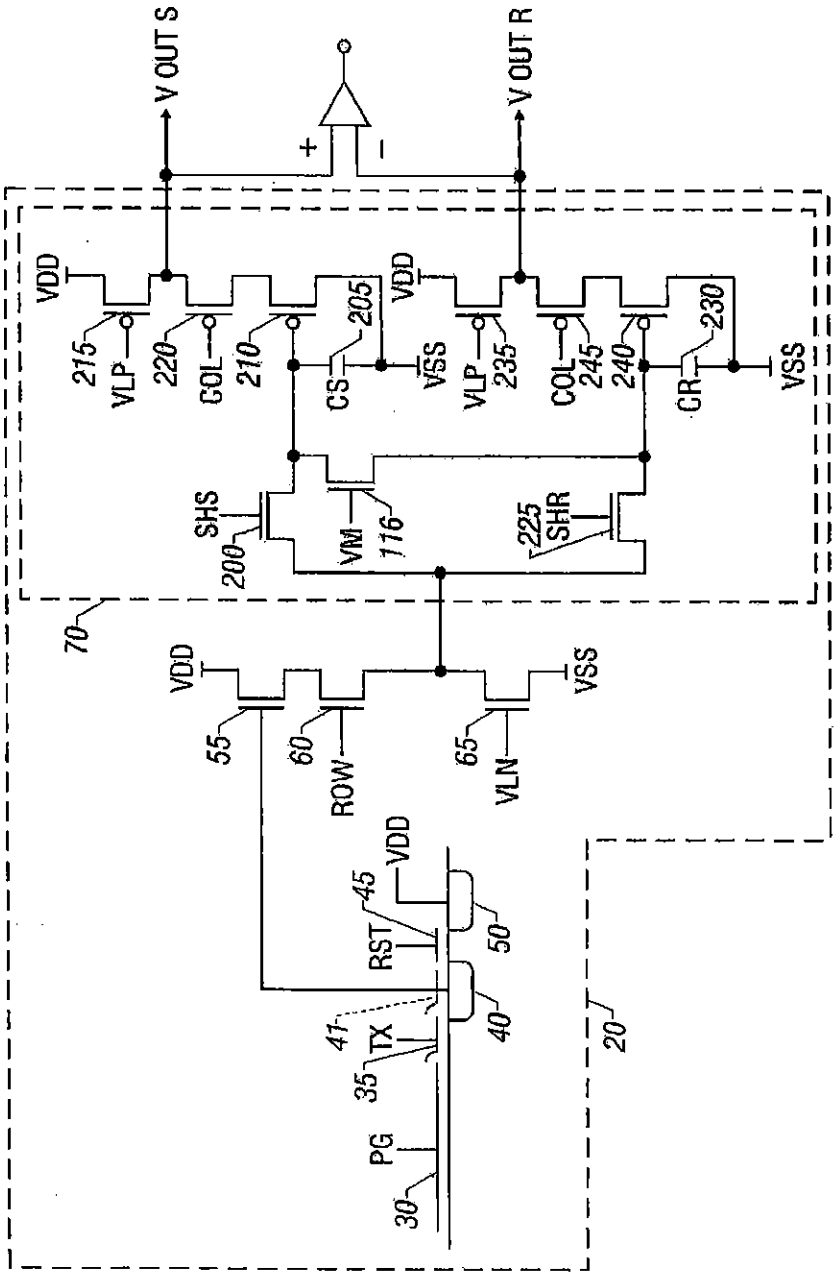


FIG. 2


V OUT S
V OUT R
+
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VDD
215
VLP
220
COL
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205
CS
VSS
VDD
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240
230
CR
VSS
SHS
200
VM
116
225
SHR
70
VDD
55
60
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VLN
VSS
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RST
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PG
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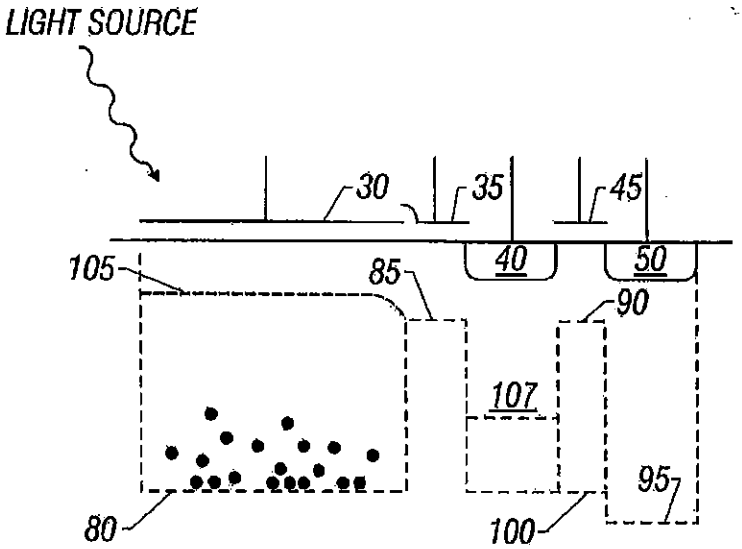
FIG. 3


LIGHT SOURCE
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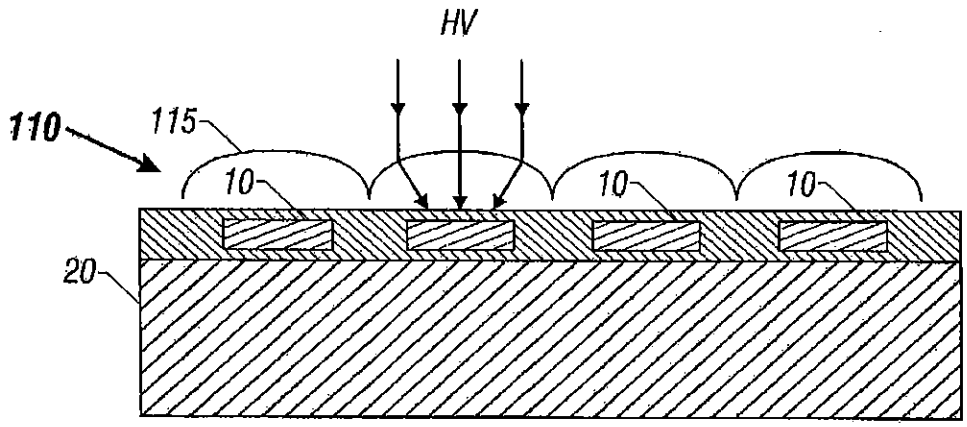
35
45
40
50
105
85
90
107
95
80
100

FIG. 4


HV
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115
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10
10
20

FIG. 5

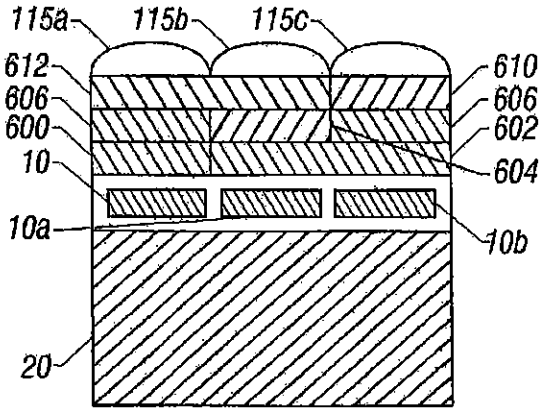

FIG. 6A

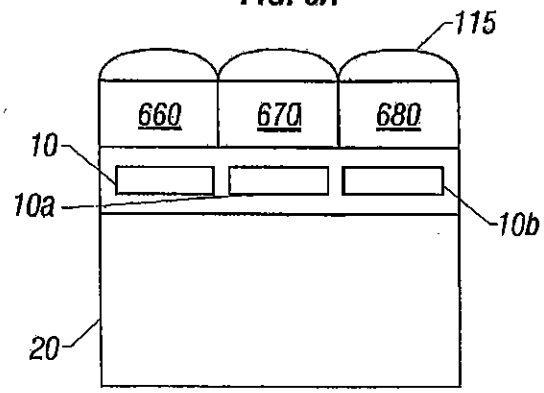

FIG. 6B

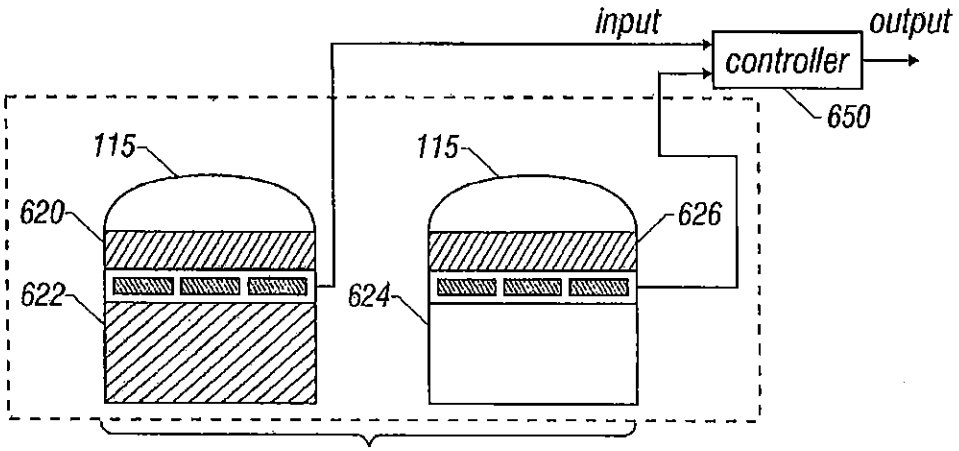

FIG. 6C

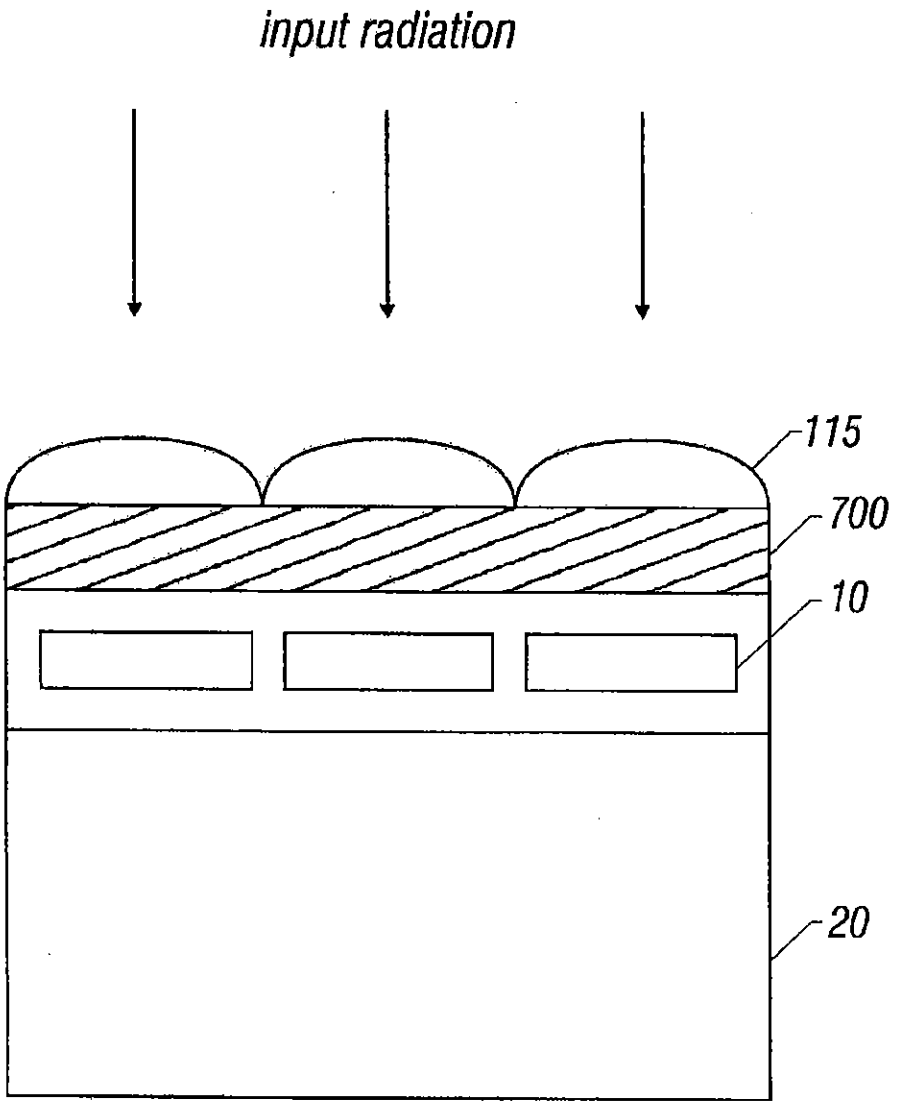

FIG. 7

ACTIVE PIXEL SENSORS WITH SUBSTANTIALLY PLANARIZED COLOR FILTERING ELEMENTS

This Application claims the benefit of the U.S. Provisional Application Ser. No. 60/013,700, filed on Mar. 20, 1996, the entirety of which is incorporated herewith by reference.

ORIGIN OF THE INVENTION

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

FIELD OF THE INVENTION

The invention is related to semiconductor imaging devices and in particular to an imaging device which can be fabricated using a standard CMOS process.

BACKGROUND AND SUMMARY OF THE INVENTION

An active pixel sensor ("APS") is a special kind of light sensing device. Each active pixel includes a light sensing element and one or more active transistors within the pixel itself. The active transistors amplify and buffer the signals generated by the light sensing elements in the pixels. One type of such APS devices is disclosed in U.S. Pat. No. 5,471,515 by Fossum et al., the disclosure of which is incorporated herein by reference.

APS devices represent an emerging technology in a wide range of imaging applications. APS has a number of significant advantages in comparison with the well-developed and widely used charge coupled devices (CCDs) and other imaging technologies including photodiode arrays, charge injection devices and hybrid focal plane arrays.

CCD devices have a number of advantages because they are an incumbent technology, they are capable of large formats and very small pixel size and they facilitate noiseless charge domain processing techniques (such as binning and time delay integration). However, CCD imagers suffer from a number of disadvantages. For example, CCD imagers operates with destructive signal read-out and their signal fidelity decreases as the charge transfer efficiency raised to the power of the number of stages. The latter requires a CCD imager to have a nearly perfect charge transfer efficiency. CCD devices are also particularly susceptible to radiation damage and usually require carefully-designed light shielding to avoid smear. Furthermore, CCD imagers usually have high power dissipation for large arrays and limited spectral responsivity range.

In order to ameliorate the charge transfer inefficiency problem, CCD imagers are fabricated with a specialized CCD semiconductor fabrication process to maximize their charge transfer efficiency. One limitation is that the standard CCD process is incompatible with complementary metal oxide semiconductor (CMOS) process, while the image signal processing electronics required for the imager are best fabricated in CMOS. Accordingly, it is impractical to integrate on-chip signal processing electronics in a CCD imager. Thus, the signal processing electronics is off-chip. Typically, each column of CCD pixels is transferred to a corresponding cell of a serial output register, whose output is amplified by a single on-chip amplifier (e.g., a source follower transistor) before being processed in off-chip signal processing electronics. As a result, the read-out frame rate is limited by the rate at which the on-chip amplifier can handle charge packets divided by the number of pixels in the imager.

The other types of imager devices have problems as well. For example, photodiode arrays usually exhibit high noise due to so-called kTC noise which makes it very difficult to reset a diode or capacitor node to the same initial voltage at the beginning of each integration period. Photodiode array, also suffer from lag. Charge injection devices usually exhibit high noise, but enjoy the advantage of non-destructive readout over CCD devices. Hybrid focal plane arrays exhibit low noise but are prohibitively expensive for many applications and have relatively small array sizes (e.g., 512-by-512 pixels).

In contrast, an APS device receives and processes input signals with the active pixel itself, thus eliminating the charge transfer over distances that are inherent in CCDs. Consequently, many drawbacks associated with CCDs are avoided in APS devices. For example, the performance of APS devices can be maintained as the array size increases. The APS readout rate is usually higher than that of CCDs. Since CMOS circuitry is often associated with the image sensor, the power consumption can be significantly reduced. APS devices are inherently compatible with CMOS processes, allowing reduced cost of manufacturing. Many on-chip operations and controls can be relatively easily implemented including timing and analog-to-digital conversion. APS devices are also less vulnerable to radiation damage and can be designed for non-destructive readout. Moreover, the active pixels of APS devices allow random access and on-chip signal processing.

The invention is embodied in an imaging device formed as a monolithic CMOS integrated circuit in an industry standard CMOS process, the integrated circuit including a focal plane array of pixel cells, each one of the cells including a photogate overlying the substrate for accumulating photo-generated charge in an underlying portion of the substrate, a readout circuit including at least an output field effect transistor formed in the substrate, and a charge coupled device section formed on the substrate adjacent the photogate having a sensing node connected to the output transistor and at least one charge coupled device stage for transferring charge from the underlying portion of the substrate to the sensing node.

In a preferred embodiment, the sensing node of the charge coupled device stage includes a floating diffusion, and the charge coupled device stage includes a transfer gate overlying the substrate between the floating diffusion and the photogate. This preferred embodiment can further include apparatus, for periodically resetting a potential of the sensing node to a predetermined potential, including a drain diffusion connected to a drain bias voltage and a reset gate between the floating diffusion and the drain diffusion, the reset gate connected to a reset control signal.

Preferably, the output transistor is a field effect source follower transistor, the floating diffusion being connected to a gate of the source follower transistor. Preferably, the readout circuit further includes a double correlated sampling circuit having an input node connected to the output transistor. In the preferred implementation, the double correlated sampling circuit samples the floating diffusion immediately after it has been reset at one capacitor and then, later, at the end of the integration period at another capacitor. The difference between the two capacitors is the signal output. In accordance with a further refinement, this difference is corrected for fixed pattern noise by subtracting another

calibration signal which is a difference sensed between the two capacitors while they are temporarily shorted.

One aspect of the present invention is an implementation of color filtering. Color filters such as polymer filters are preferably integrated with an APS sensor for color separation. Alternatively, a plurality of APS sensors each having a color filter for a different color may to used to achieve maximum imaging resolution.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and advantages of the present invention will become more apparent in the light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawing, in which:

FIG. 1 is a diagram illustrating the architecture of an individual focal plane cell of the invention.

FIG. 2 is a plan view of an integrated circuit constituting a focal plan array of cells of the type illustrated in FIG. 1.

FIG. 3 is a schematic diagram of the cell of FIG. 1.

FIG. 4 is a graph of the surface potential in the charge transfer section of the cell of FIG. 3.

FIG. 5 is a cross-sectional view of an alternative embodiment of the focal plane array of FIG. 2 including a microlens layer.

FIG. 6A shows a first embodiment of a single APS sensor with three sets of polymer filters.

FIG. 6B shows another embodiment of a single APS sensor with three sets of polymer filters.

FIG. 6C shows a second embodiment of a plurality of APS sensors each having a different polymer filter.

FIG. 7 shows an APS device with an integrated phosphor layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a simplified block diagram of one pixel cell **10** of a focal plane array of many such cells formed in an integrated circuit shown in FIG. 2. Each cell **10** includes a photogate **12**, a charge transfer section **14** adjacent to the photogate **12**, and a readout circuit **16** adjacent to the charge transfer section **14**. FIG. 3 is a simplified schematic diagram of a preferred configuration of cell **10**. FIG. 3 shows the photogate **12** with a relatively large photogate electrode **30** overlying the substrate **20**. The charge transfer section **14** includes a transfer gate electrode **35** adjacent to the photogate electrode **30**, a floating diffusion **40**, a reset electrode **45** and a drain diffusion **50**. The readout circuit **16** includes a source follower field effect transistor (FET) **55**, a row select FET **60**, a load FET **65** and a correlated double sampling circuit **70**.

FIG. 4 shows the surface potential diagram cell **10**. The photogate electrode **30** is held by a photogate signal PG at a positive voltage to form a potential well **80** in the substrate **20** in which photo-generated charge is accumulated during an integration period. The transfer gate electrode **35** is initially held at a less positive voltage by a transfer gate signal TX to form a potential barrier **85** adjacent to the potential well **80**. The floating diffusion **40** is connected to the gate of the source follower FET **55** whose drain **50** is connected to a drain supply voltage VDD. The reset electrode **45** is initially held by a reset signal RST at a voltage corresponding to the voltage on the transfer gate **30** to form a potential barrier **90** thereunder. The drain supply voltage VDD connected to the drain diffusion **50** creates a constant potential well **95** underneath the drain diffusion **50**.

A preferred operation sequence of cell **10** of FIG. **3** is described as follows. During an integration period, electrons accumulate in the potential well **80** in proportion to photon flux incident on the substrate **20** beneath the photogate electrode **30**. At the end of the integration period, the surface potential beneath the floating diffusion **40** is quickly reset to a potential level **100** slightly above the potential well **95**. This is accomplished by the reset signal RST temporarily increasing to a higher positive voltage to temporarily remove the potential barrier **90** and provide a downward potential staircase from the transfer gate potential barrier **85** to the drain diffusion potential well **95**, as indicated in FIG. **4**.

After the reset gate **45** is returned to its initial potential (restoring the potential barrier **90**), the readout circuit **70** briefly samples the potential of the floating diffusion **40**, and then the cell **10** is ready to transfer the photo-generated charge from beneath the photogate electrode **30**. For this purpose, the photogate signal PG deceases to a less positive voltage to form a potential barrier **105** beneath the photogate electrode **30** and thereby provides a downward staircase surface potential from the photogate electrode **30** to the potential well **100** beneath the floating diffusion **40**. This transfers all of the charge from beneath the photogate electrode **30** to the floating diffusion **40**, changing the potential of the floating diffusion **40** from the level **100** at which it was previously reset to a new level **107** indicative of the amount of charge accumulated during the integration period. This new potential of the floating diffusion **40** is sensed at the source of the source follower FET **55**. However, before the readout circuit **70** samples the source of the source follower FET **55**, the photogate signal PG returns to its initial (more positive) voltage. The entire process is repeated for the next integration period.

The readout circuit **70** has a signal sample and hold (S/H) circuit including an S/H FET **200** and a signal store capacitor **205** with a first side connected through the S/H FET **200** and through the row select FET **60** to the source of the source follower FET **55**. A second side of the capacitor **205** is connected to a source bias voltage VSS. The first side of the capacitor **205** is also connected to the gate of an output FET **210**. The drain of the output FET **210** is connected through a column select FET **220** to a signal sample output node VOUTS and through a load FET **215** to the drain voltage VDD. A signal called "signal sample and hold" (SHS) briefly turns on the S/H FET **200** after the charge accumulated beneath the photogate electrode **30** has been transferred to the floating diffusion **40**, so that the capacitor **205** stores the source voltage of the source follower FET **55** indicating the amount of charge previously accumulated beneath the photogate electrode **30**.

The readout circuit **70** also has a reset sample and hold (S/H) circuit including an S/H FET **225** and a signal store capacitor **230** with a first side connected through the S/H FET **225** and through the row select FET **60** to the source of the source follower FET **55**. The second side of the capacitor **230** is connected to the source bias voltage VSS. The first side of the capacitor **230** is also connected to the gate of an output FET **240**. The drain of the output FET **240** is connected through a column select FET **245** to a reset sample output node VOUTR and through a load FET **235** to the drain voltage VDD. A signal called "reset sample and hold" (SHR) briefly turns on the S/H FET **225** immediately after the reset signal RST has caused the resetting of the potential of the floating diffusion **40**, so that the capacitor **230** stores the voltage at which the floating diffusion has been reset to.

The readout circuit 70 provides correlated double sampling of the potential of the floating diffusion. The charge accumulated beneath the photogate 12 in each integration period is obtained at the end of each integration period from the difference between the voltages at the output nodes VOUTS and VOUTR of the readout circuit 70. This eliminates the effects of kTC noise because the difference between VOUTS and VOUTR is independent of any variation in the reset voltage RST, a significant advantage.

The focal plane array corresponding to FIGS. 1–4 is preferably implemented in CMOS silicon using an industry standard CMOS fabrication process. Preferably, each of the FETs is a MOSFET, the FETs 55, 60, 65, 200 and 225 being n-channel devices and the FETs 210, 220, 225, 230, 240, 245 being p-channel devices. The n-channel MOSFETS and the CCD channel underlying the gate electrodes 30, 35, 45 and the diffusions 40 and 50 may be located in a p-well while the remaining (p-channel) devices are located outside of the p-well. The gate voltage VLP applied to the gates of the p-channel load FETs 215 and 235 is a constant voltage on the order of +2.5 volts. The gate voltage VLN applied to the n-channel load FET 65 is a constant voltage on the order of +1.5 volts.

The dopant concentrations of the n-channel and p-channel devices and of the various diffusions are preferably in accordance with the above preferred industry standard CMOS process. In one prototype implementation, the area of the L-shaped photogate 12 (i.e., the photogate electrode 30) was about 100 square microns; the transfer gate electrode 35 and the reset gate electrode were each about 1.5 microns by about 6 microns; the photogate signal PG was varied between about +5 volts (its more positive voltage) and about 0 volts (its less positive voltage; the transfer gate signal TX was about +2.5 volts; the reset signal RST was varied between about +5 volts (its more positive voltage) and about +2.5 volts (its less positive voltage); the drain diffusion 50 was held at about +5 volts.

Since the charge transfer section 14 involves only one equivalent single CCD stage between the photogate 12 and the floating diffusion 40 in the specific embodiment of FIG. 3, there is no loss due to charge transfer inefficiency and therefore there is no need to fabricate the device with a special CCD process. As a result, the readout circuit 70 as well as the output circuitry of the FETs 55, and 60 and 65 can be readily implemented as standard CMOS circuits, making them extremely inexpensive. However, any suitable charge coupled device architecture may be employed to implement the charge transfer section 14, including a CCD having more than one stage. For example, two or three stages may be useful for buffering two or three integration periods.

Another feature of the invention which is useful for eliminating fixed pattern noise due to variations in FET threshold voltage across the substrate 20 is a shorting FET 116 across the sampling capacitors 205, 230. After the accumulated charge has been measured as the potential difference between the two output nodes VOUTS and VOUTR, a shorting signal VM is temporarily applied to the gate of the shorting FET 116 and the VOUTS-to VOUTR difference is measured again. This latter difference is a measure of the disparity between the threshold voltages of the output FETs 210, 240, and may be referred to as the fixed pattern difference. The fixed pattern difference is subtracted from the difference between VOUTS and VOUTR measured at the end of the integration period, to remove fixed pattern noise.

The inventors found that a light coupling device can be formed on the sensor array to improve the performance thereof. This is shown in FIG. 5. A transparent refractive microlens layer 110 may be deposited over the top of the focal plane array of FIG. 2. The microlens layer 110 consists of spherical portion 115 centered over each of the cells 10 and contoured so as to focus light toward the center of each photogate 12 in each pixel. This has the advantage of using light that would otherwise fall outside of the optically active region of the photogate 12. For example, at least some of the light ordinarily incident on either the charge transfer section 14 or the readout circuit 16 (FIG. 1) would be sensed in the photogate area with the addition of the microlens layer 110.

FIGS. 6A–6C show alternative embodiments of the invention which use color filtering. Color filtering enables spatial separation of color in an imaging device. CCD devices, for example, commonly use color filtering for color separation in this way.

A first preferred system as illustrated in FIG. 6A allows a plurality of pixels to have different color filtering properties to provide a color filtering effect. Typically this is done by using color filters in some array form, for example, alternate green filters interspersed with red and blue filters. An exemplary filter operation would use a plurality of color filters in a sequence such as green/red/green/blue/green/red/green/blue with that pattern continuing for the length of the array.

The system in FIG. 6A uses a polymer color filter array. Such polymer color filter arrays are well-known in the art and are described in various publications, for example, "Solid State Imaging with Charge Coupled Devices", by Albert Theuwissen, Kluwer Academic Press, 1995. Layer 600 is preferably a red layer, and is first deposited over the entire chip having an array of sensing pixels (e.g., 10, 10*a*, and 10*b*) on substrate 20. Subsequent to deposition, an etching technique is used to remove the red filter area 600 from everywhere except over the desired pixel 10. A planarization layer 602 formed with a transparent polymeric material covers the removed areas to thereby planarize that surface. Blue filter 604 is next deposited over the flat surface formed by red filter 600 and planarization layer 602. Blue filter 604 is similarly etched such that it only covers the desired pixel 10*a*. The remaining area is again planarized by a second planarization layer 606. Finally, a green filter 610 is formed over that planarized layer, covering pixel 10*b*. Planarization layer 612 flattens the resulting area so that green filter 610 only covers the pixel 10*b*.

Alternatively, the above processing method can use masks so that a desired color filter only forms at one or more selected pixel locations. Another way of forming color filters is to form a first color filtering layer on the entire sensor array. Then the first color filtering layer is patterned to a first desired spatial pattern to expose the rest of the sensor array that is not covered by the patterned first color filtering layer (a mask can be used to achieve the same and then the masking layer is etched). Next, a second color filtering layer is formed in a second spatial pattern in the exposed areas on the sensor array with a mask. Lastly, a third color filtering layer of a third spatial pattern is formed in the remaining area with a mask. Thus, a single color filtering layer is formed on the sensor array with a desired distribution of different filtering materials. This is shown in FIG. 6B.

Also, other color combinations can be used instead of primary colors red, green, and blue. For example, filters for colors cyan, yellow and magenta may be used. Furthermore, other sequence of forming color filtering parts may be used. For example, blue filter can be first formed, then the green, and then the red filter.

According to this embodiment of the present invention, each pixel, including the polymer layers for color filtering, can be covered by microlens **115A**, **155B** and **115C**. The microlenses modify the incoming light in conjunction with the polymer layers. The light is therefore changed by both microlenses **115A–115C** and color filtering parts **612**, **606**, and **600**. Each pixel, therefore, preferably receives light that has been doubly modified in this way.

This polymer color filter array causes the device to lose a certain amount of resolution of the scene being imaged since some of the pixels are dedicated to a different color. For example, if three neighboring pixels are combined to represent one color image element, the effective image resolution will be reduced by a factor of three.

A second embodiment shown in FIG. **6C** does not lose resolution, but instead requires multiple chips to form an image. This alternative embodiment uses a plurality of APS chips that are substantially identical to one another. Each APS chip is coated with a different color filtering film. For example, an AOPS device **622** has a green filter **620** in the system of FIG. **6C**. Therefore, two other APS devices are also necessary for a full color operation, each of which acts a different color filter. Device **624**, for example, includes a blue filter **626**. This arrangement allows device **622** to receive a different color than device **626**. Each device is preferably covered by microlens **115**. The different color images from different sensors such as **622** and **624** can be correlated to produce a final image. An electronic controller **650** can be implemented to perform the image correlation. The controller **650** receives images of different colors from different sensors such as **622** and **624** to form the final image.

The inventors further contemplate that a wavelength-converting phosphor can be implemented with an APS device. This is necessary in some applications since the spectral response of an APS device is limited. For example, many silicon-based APS devices are limited in visible or near infrared spectral bands and not efficient in detecting blue, UV, or X-ray bands. A wavelength-converting phosphor is typically tuned to accept radiation of a desired wavelength, e.g., ultra-violet or x-ray. Therefore, the phosphor, when receiving this radiation, emits a photon of the proper type to properly excite the underlying silicon.

The wavelength-converting phosphor could be deposited atop of a sensor array in an APS device so that a radiation signal outside the spectral response range of the APS can still be detected. Thus, the advantages of an APS device can be utilized.

FIG. **7** shows one preferred embodiment of such a system. A layer of a suitable phosphor **700** is formed on the top of the sensor array having active pixels **10** on substrate **20**. Different phosphors can be used depending on the wavelength range of the input signal. The phosphor layer **700** receives the input radiation and emits photons that are detectable by the pixels **10**. Therefore, the signals from the pixels **10** can be converted into an image indicative of the input radiation. One application of this system is X-ray sensors.

Although the present invention has been described in detail with reference to the preferred embodiments, one ordinarily skilled in the art to which this invention pertains will appreciate that various modifications and enhancements may be predictable.

For example, the floating diffusion **40** may instead be a floating gate electrode. Such a floating gate is indicated schematically in FIG. **3** by a simplified dashed line floating gate electrode **41**. The signal and reset sample and hold circuits of the readout circuit **70** may be any suitable sample and hold circuits. Moreover, shielding of the type well-known in the art may be employed defining an aperture surrounding the photogate **12**. Also, the invention may be implemented as a buried channel device.

What is claimed is:

1. An integrated semiconductor imaging device, comprising:

a sensor array having a plurality of pixel circuits disposed relative to one another on a semiconductor substrate, each of said pixel circuits including an optical sensor to receive light and an electronic element having at least one active transistor to convert said light into an electrical signal, wherein said pixel circuits are operable to generate an indicia indicative of an input scene;

a first color filtering layer formed on said sensor array to cover a first portion of said sensor array and configured to transmit light in at least a first selected spectral bandwidth and absorb light that is substantially outside said first selected bandwidth, said optical sensor in each of said pixel circuits in said first portion being responsive in said first selected spectral bandwidth; and

a first transparent layer, formed on said sensor array and displaced relative to said first color filtering layer to cover a remaining portion of said sensor array that is not covered by said first color filtering layer, said first transparent layer and said first color filtering layer being substantially of a same thickness and forming a first planarized layer which has a substantially flat upper surface on said first sensor array to cover said pixel circuits.

2. A device as in claim **1**, further comprising:

a second color filtering layer formed over said first planarized layer and disposed relative to said first color filtering layer to cover a second portion of said sensor array, said second color filtering layer operating to transmit light in at least a second selected spectral bandwidth and absorb light that is substantially outside said second selected bandwidth, said optical sensor in each of said pixel circuits in said second portion being responsive in said second selected spectral bandwidth;

a second transparent layer, formed over said first planarized layer, displaced relative to said second color filtering layer to cover a remaining portion of said first planarized layer that is not covered by said second color filtering layer, said second transparent layer and said second color filtering layer being substantially of a same thickness and forming a second planarized layer over said first planarized layer;

a third color filtering layer formed over said second planarized layer and disposed relative to said first and second color filtering layers to cover a third portion of said sensor array, said third color filtering layer operating to transmit light at least in a third selected spectral bandwidth and absorb light that is substantially outside said third selected bandwidth, said optical sensor in each of said pixel circuits in said third portion being responsive in said third selected spectral bandwidth; and

a third transparent layer, formed over said second planarized layer and displaced relative to said third color filtering layer to cover a remaining portion of said second planarized layer that is not covered by said third color filtering layer, said third transparent layer and said third color filtering layer being substantially of a

same thickness and forming a third planarized layer over said second planarized layer, whereby each optical sensor in each of said pixel circuits receives a light beam that only transmits through one of said first, second and third color filtering layers.

3. A device as in claim 2, wherein said first color filtering layer has a first spatial pattern, said second color filtering layer has a second spatial pattern, and said third color filtering layer has a third spatial pattern.

4. A device as in claim 3, wherein said first, second, and third spatial patterns are arranged with respect to one another so that one of said pixels receiving light filtered by one of said three color filtering layers has two neighboring pixels each receiving light filtered by one of other two of said three color filtering layers.

5. A device as in claim 2, wherein at least one of said first, second, and third color filtering layers is made of a polymeric material.

6. A device as in claim 2, wherein at least one of said first, second, and third transparent layers is made of a polymeric material.

7. A device as in claim 2, further comprising a light coupling array of microlenses formed on said third planarized layer, each microlens in said light coupling array being positioned over a pixel circuit of said sensor array so that light received by said optical sensor passes through one of said microlenses and one of said color filtering layers.

8. An imaging system capable of color filtering, comprising:

a plurality of semiconductor substrates separated from one another;

a plurality of sensor arrays respectively formed on said substrates and each having a plurality of pixel circuits, each pixel circuit in each sensor array including an optical sensor to receive light and an electronic element having at least one active transistor to convert said light into an electrical signal, said sensor arrays disposed relative to one another to receive an input image and operable to respectively generate indicia of different colors of the input image; and

an electronic controller, coupled to said sensor arrays to correlate said indicia of different colors from said sensor arrays to compose a final image of said input image.

9. A device as in claim 8, wherein each of said sensor arrays comprises a light coupling array of microlenses formed over said pixel circuits, each microlens in said light coupling array being positioned over a pixel circuit of said first sensor array to couple light to said optical sensor in said pixel circuit.

10. A system as in claim 8, wherein said plurality of sensor arrays include:

a first sensor array having a first color filtering layer formed to cover respective pixel circuits, operating to transmit light in a first selected spectral bandwidth and absorb light that is substantially outside said first selected bandwidth, said first sensor array producing a first image representing said input image in said first selected bandwidth;

a second sensor array having a second color filtering layer formed to cover respective pixel circuits, operating to transmit light in a second selected spectral bandwidth different from said first selected bandwidth and absorb light that is substantially outside said second selected bandwidth, said second sensor array producing a second image representing said input image in said second selected bandwidth; and

a third sensor array having a third color filtering layer formed to cover respective pixel circuits, operating to transmit light in a third selected spectral bandwidth different from said first and second selected bandwidths and absorb light that is substantially outside said third selected bandwidth, said third sensor array producing a third image representing said input image in said third selected bandwidth, wherein said electronic controller correlates said first, second, and third images to form said final image with colors based on said first, second, and third selected bandwidths.

11. A system as in claim 10, wherein at least one of said first, second, and third color filtering layers is made of a polymeric material.

12. An integrated imaging sensor, comprising:

an active pixel sensor array, having a plurality of active pixels responsive to photons in a first spectral range, each of said active pixels having at least one active transistor and operating to covert said photons into an electrical signal; and

a phosphor layer formed on top of said sensor array, operable to convert radiation in a second spectral range into said first spectral range, said second spectral range being out of said first spectral range, whereby said integrated imaging sensor is operable to detect a signal in said second spectral range.

13. A sensor as in claim 12, wherein said first spectral range is within a range in which a silicon-based photosensor is responsive.

14. A sensor as in claim 12, wherein said second spectral range is within ultraviolet range or in X-ray range.

15. An integrated semiconductor imaging device, comprising:

a sensor array having a plurality of active pixel circuits disposed relative to one another on a semiconductor substrate, each of said active pixel circuits including an optical sensor to receive light and at least one active transistor to convert said light into an electrical signal, wherein said pixel circuits are operable to generate an indicia indicative of an input scene; and

a substantially planarized color filtering layer formed on said sensor array to cover said active pixel circuits and configured to effect color filtering and color separation on said input scene, said color filtering layer formed of an array of color filtering regions which are arranged relative to one another in said color filtering layer and have an one-to-one correspondence to said active pixel circuits, wherein said color filtering regions include at least three different types corresponding to three different transmitted colors.

16. Device as in claim 15, further comprising a light coupling array of microlenses formed over said color filtering layer, each microlens in said light coupling array being positioned over an active pixel circuit of said first sensor array to couple light to said optical sensor in said active pixel circuit through said color filtering layer.

17. A method for constructing and operating an integrated semiconductor imaging device, comprising:

forming a plurality of pixel circuits disposed relative to one another on a semiconductor substrate to provide a sensor array, each of said pixel circuits including an optical sensor to receive light and an electronic element having at least one active transistor to convert said light into an electrical signal, wherein said pixel circuits are operable to generate an indicia indicative of an input scene; and

separating frequency components in said input scene into three different frequency ranges by using first, second and third color filtering layers sequentially formed on said sensor array, wherein each of said color filtering layers includes a plurality of color filtering regions covering selected pixel circuits of said sensor array and a plurality of transparent regions disposed relative to said color filtering regions to form a planarized layer and to cover pixel circuits that are not covered by said color filtering regions, and color filtering regions in one layer being of a same type that is different from color filtering regions of another layer.

18. A method as in claim 17, further comprising forming a microlens array over said third color filtering layer to couple said input scene to said pixel circuits through said third, second and first color filtering layers.

19. A method for constructing and operating an integrated semiconductor imaging device, comprising:

forming a plurality of pixel circuits disposed relative to one another on a semiconductor substrate to provide a sensor array, each of said pixel circuits including an optical sensor to receive light and an electronic element having at least one active transistor to convert said light into an electrical signal, wherein said pixel circuits are operable to generate an indicia indicative of an input scene;

separating frequency components in said input scene into three different frequency ranges by using a substantially planarized color filtering layer formed on said sensor array to cover said pixel circuits, said color filtering layer formed of an array of color filtering regions which are arranged relative to one another in said color filtering layer and have an one-to-one correspondence to said pixel circuits, wherein said color filtering regions include at least three different types corresponding to said three different frequency ranges; and

forming a microlens array over said third color filtering layer to couple said input scene to said pixel circuits through said third, second and first color filtering layers.

* * * * *

EXHIBIT B

US006456326B2

(12) **United States Patent**
Fossum et al.

(10) **Patent No.: US 6,456,326 B2**
(45) **Date of Patent: Sep. 24, 2002**

(54) **SINGLE CHIP CAMERA DEVICE HAVING DOUBLE SAMPLING OPERATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Jan. 2, 2001**

Related U.S. Application Data

(62) Division of application No. 09/120,856, filed on Jul. 21, 1998, which is a continuation of application No. 08/789,608, filed on Jan. 24, 1997, now Pat. No. 5,841,126, which is a continuation-in-part of application No. 08/558,521, filed on Nov. 16, 1995, now Pat. No. 6,101,232, which is a continuation of application No. 08/188,032, filed on Jan. 28, 1994, now Pat. No. 5,471,515.

(60) Provisional application No. 60/010,678, filed on Jan. 26, 1996.

(51) **Int. Cl.**[7] **H04N 5/335**

(52) **U.S. Cl.** **348/308**; 348/241

(58) **Field of Search** 348/294, 295, 348/297, 300, 301, 302, 303, 308, 241; H04N 5/335

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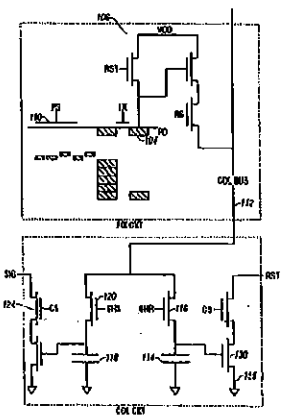
(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(57) **ABSTRACT**

A single chip camera device is formed on a single substrate including an image acquisition portion for control portion and the timing circuit formed on the substrate. The timing circuit also controls the photoreceptors in a double sampling mode in which are reset level is first read and then after an integration time a charged level is read.

18 Claims, 10 Drawing Sheets



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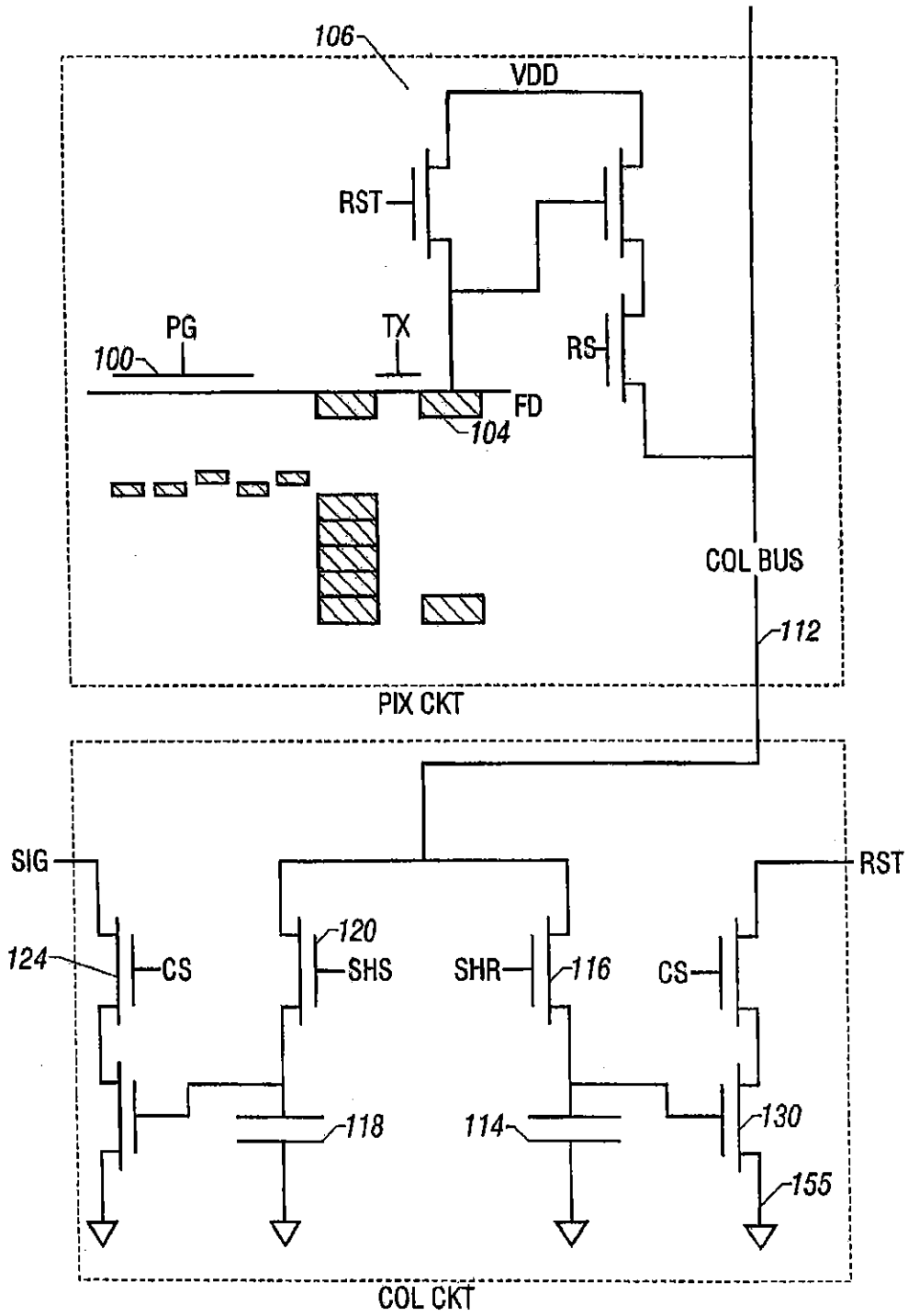
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118
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130
155
COL CKT

FIG. 1

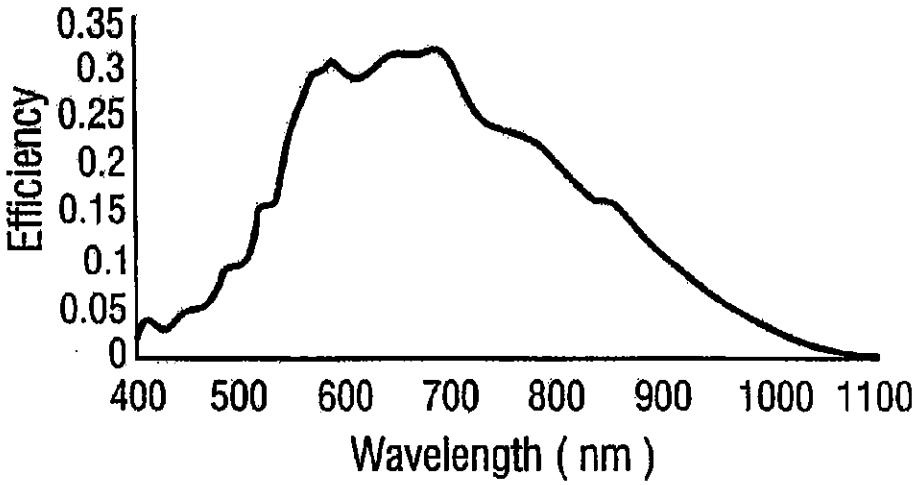
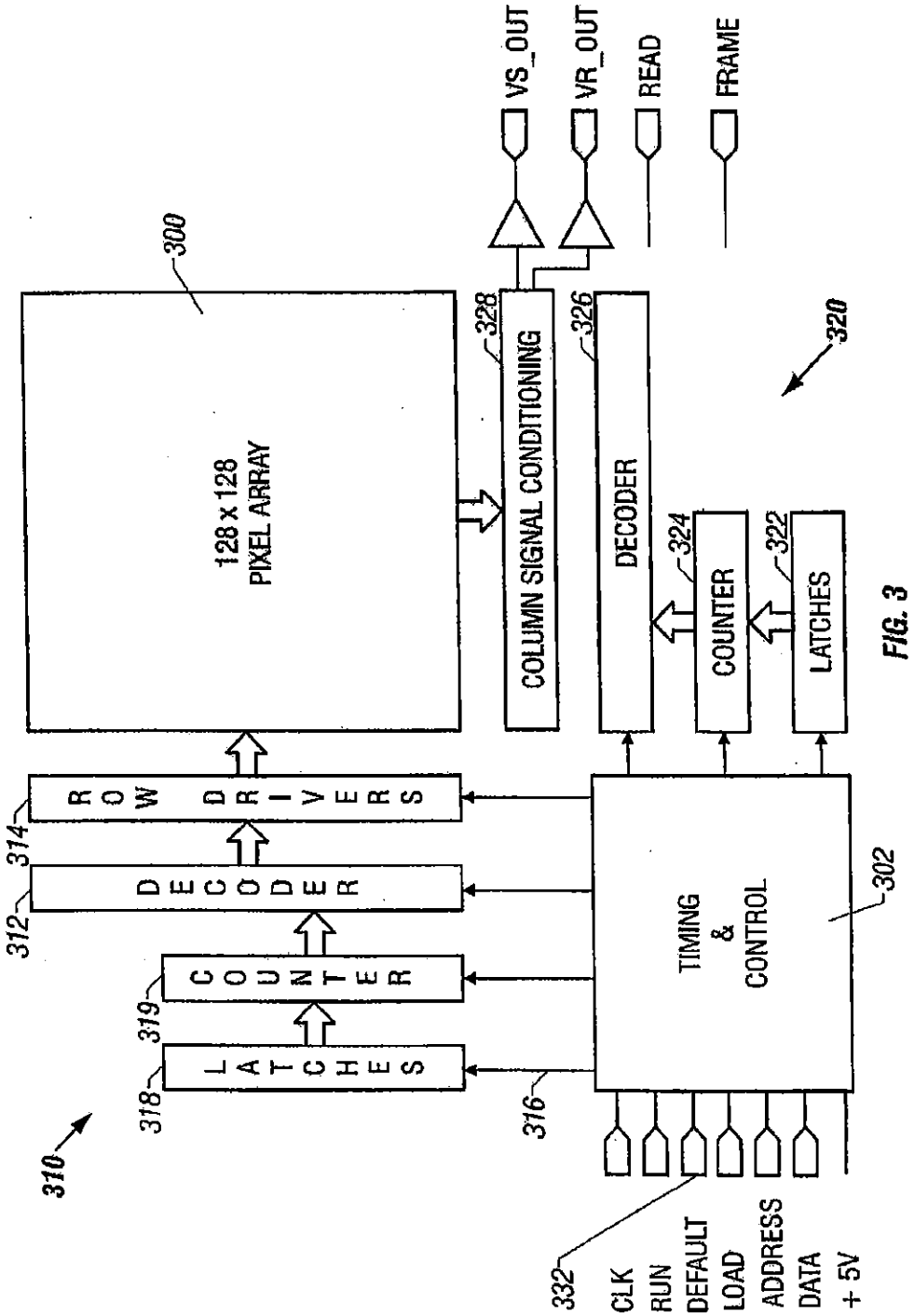

Efficiency
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
400
500
600
700
800
900
1000
1100
Wavelength (nm)

FIG. 2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VR_OUT
READ
FRAME
300
128 x 128 PIXEL ARRAY
328
COLUMN SIGNAL CONDITIONING
326
DECODER
320
324
COUNTER
322
LATCHES
ROW DRIVERS
314
DECODER
312
COUNTER
319
LATCHES
318
310
316
TIMING & CONTROL
302
332
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
+ 5V

FIG. 3

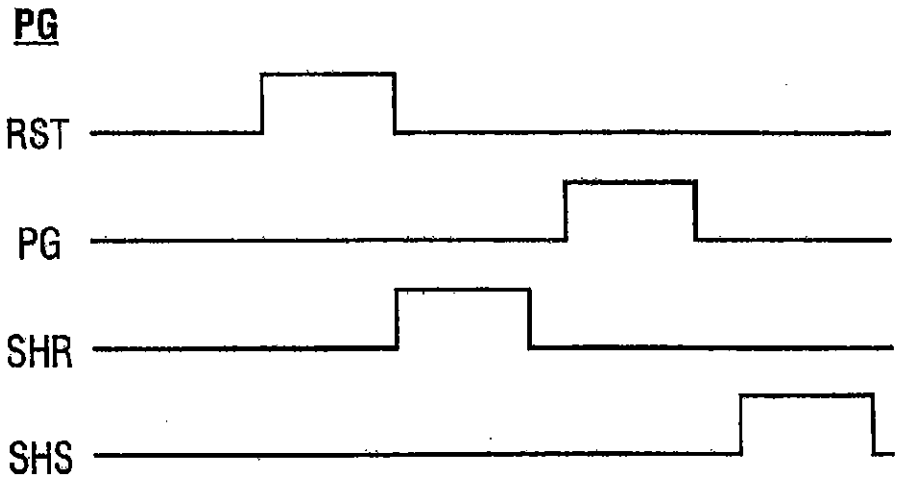


FIG. 4A

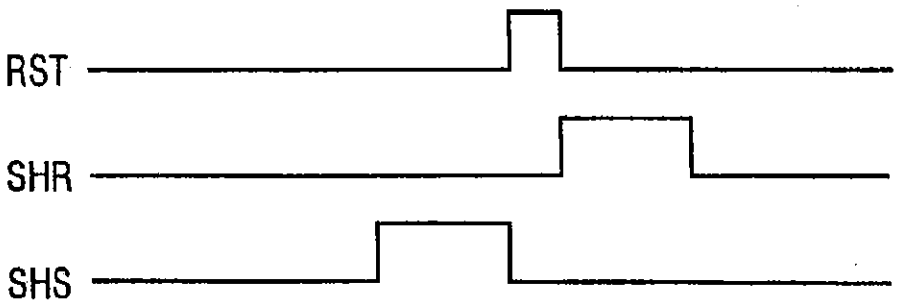
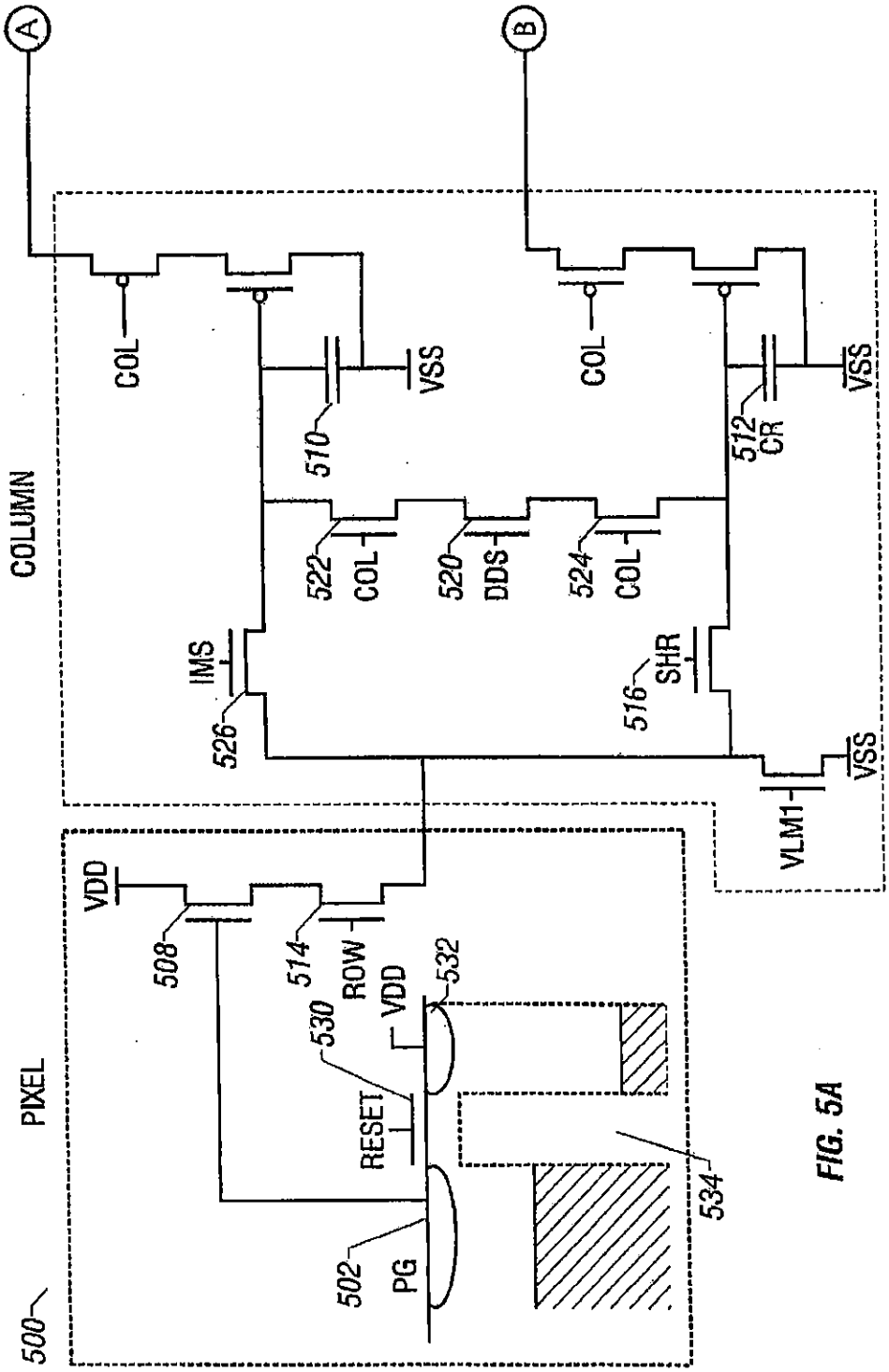


FIG. 4B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CR
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522
COL
520
DDS
524
COL
IMS
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SHR
516
VSS
VLM1
VDD
508
514
ROW
VDD
532
530
RESET
534
PIXEL
502
PG
500

FIG. 5A

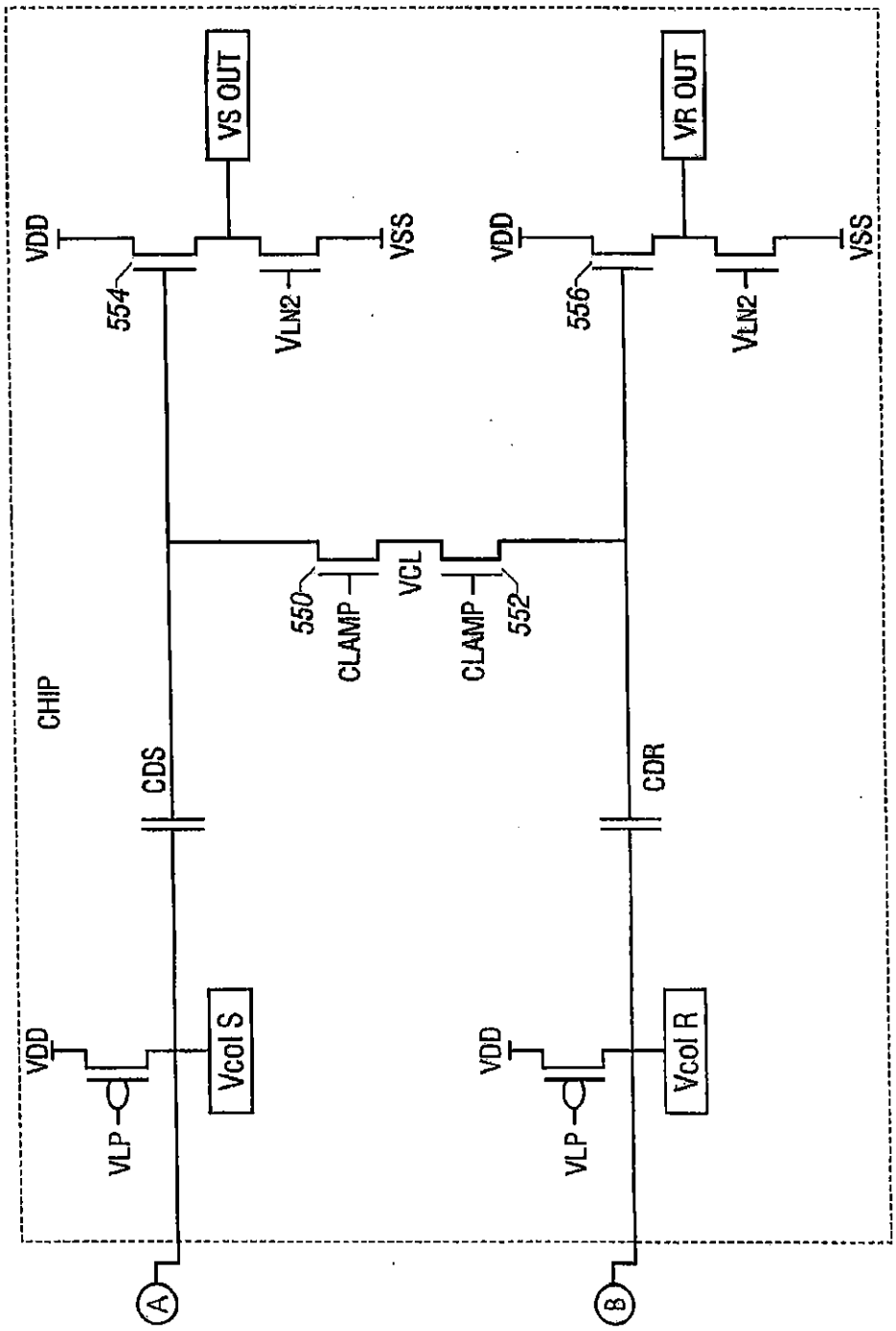

VS OUT
VR OUT
VDD
VSS
554
556
VLN2
550
552
CLAMP
VCL
CHIP
CDS
CDR
VLP
Vcol S
Vcol R
A
B

FIG. 5B

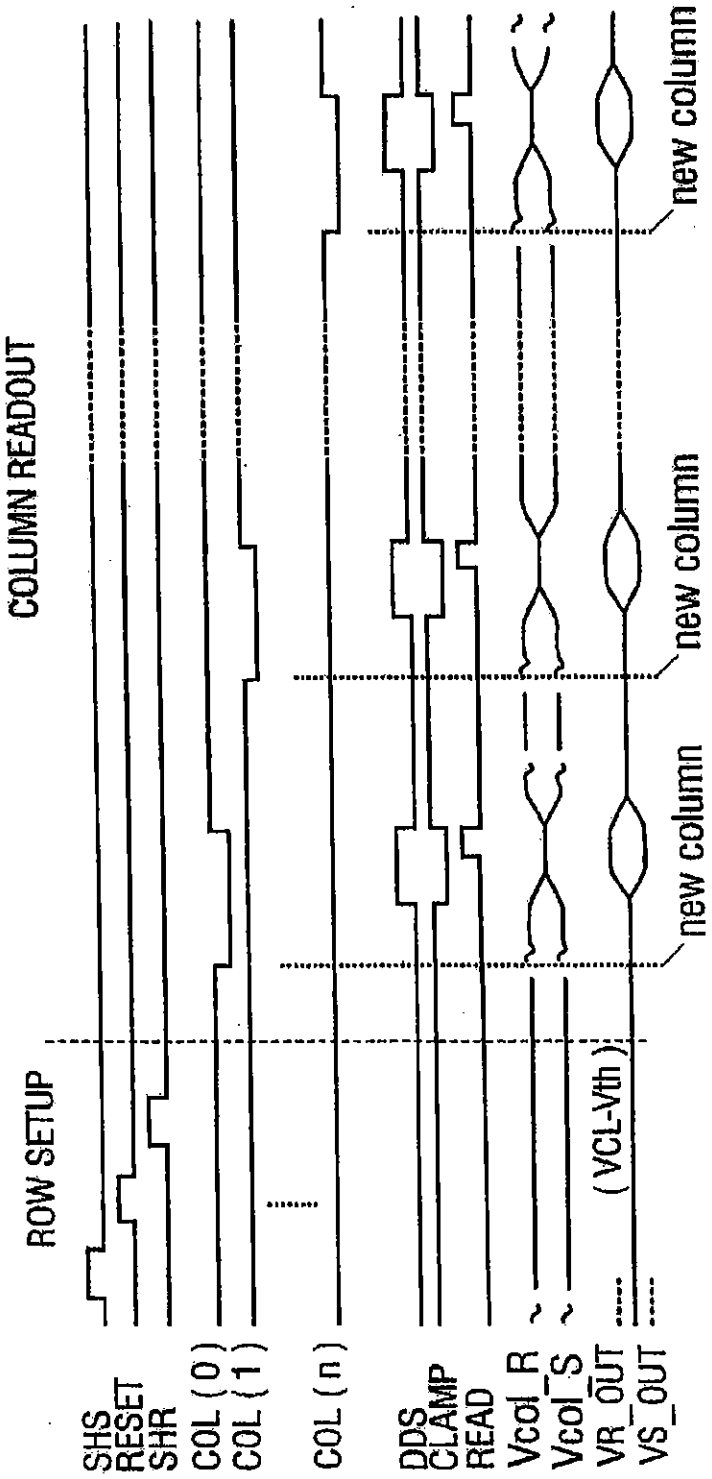

COLUMN READOUT
ROW SETUP
SHS
RESET
SHR
COL(0)
COL(1)
COL(n)
DDS
CLAMP
READ
Vcol_R
Vcol_S
VR_OUT
VS_OUT
(VCL-Vth)
new column
new column
new column

FIG. 6

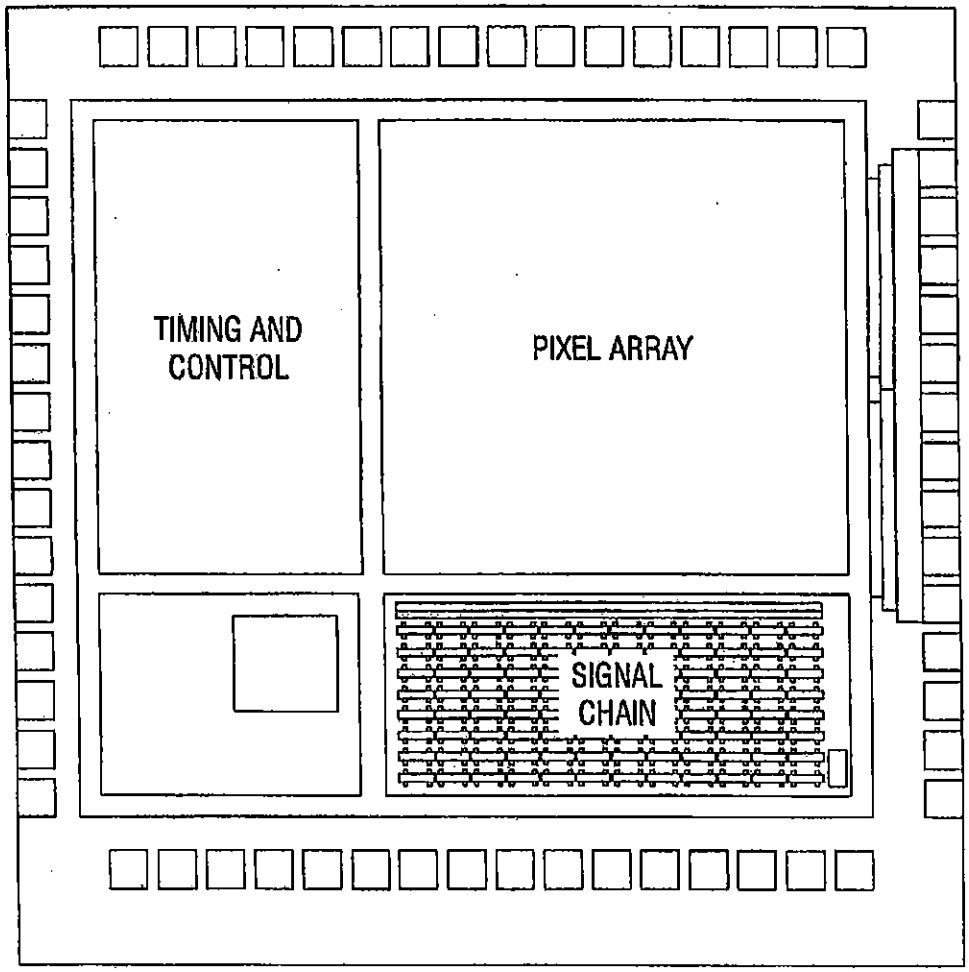


FIG. 7

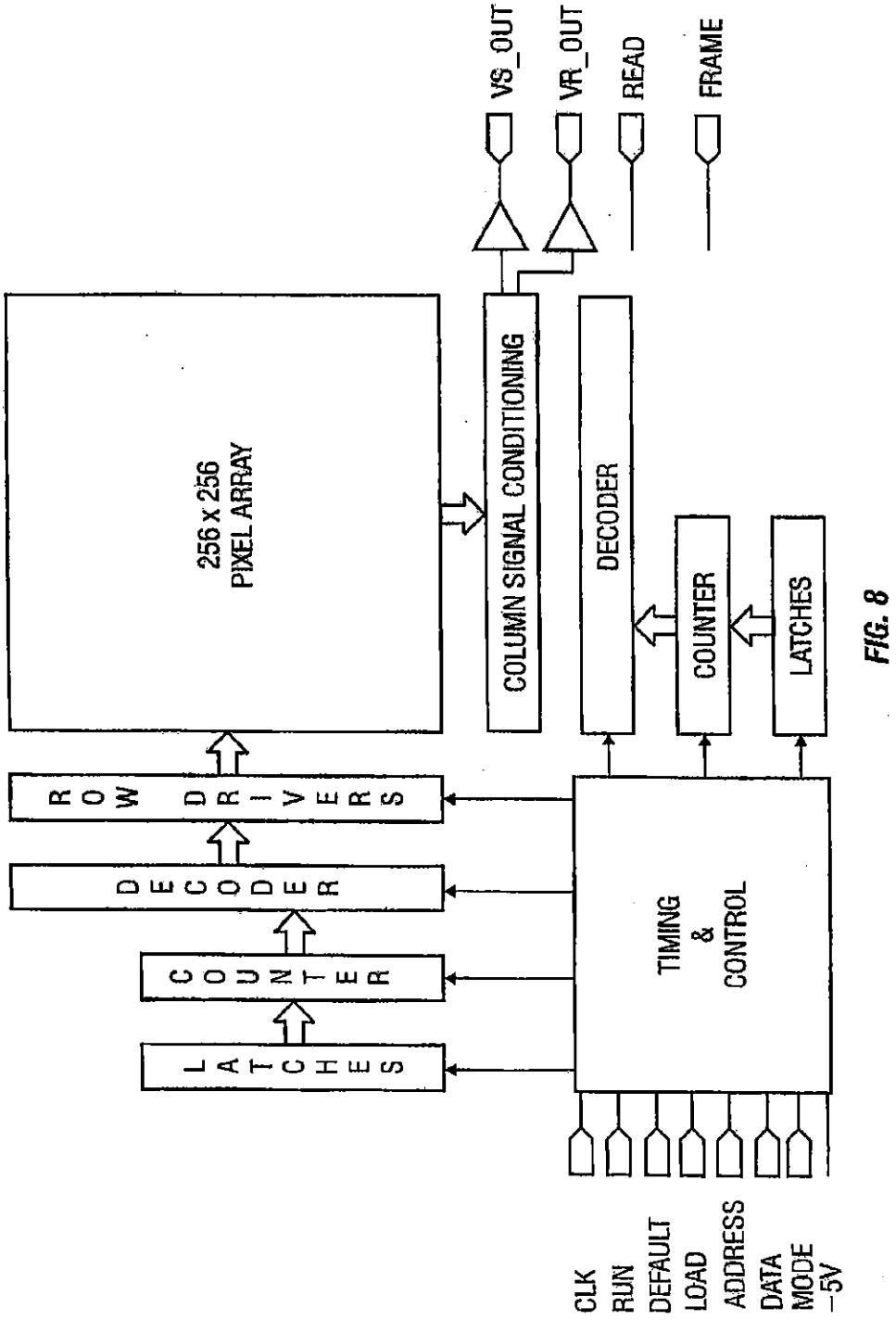
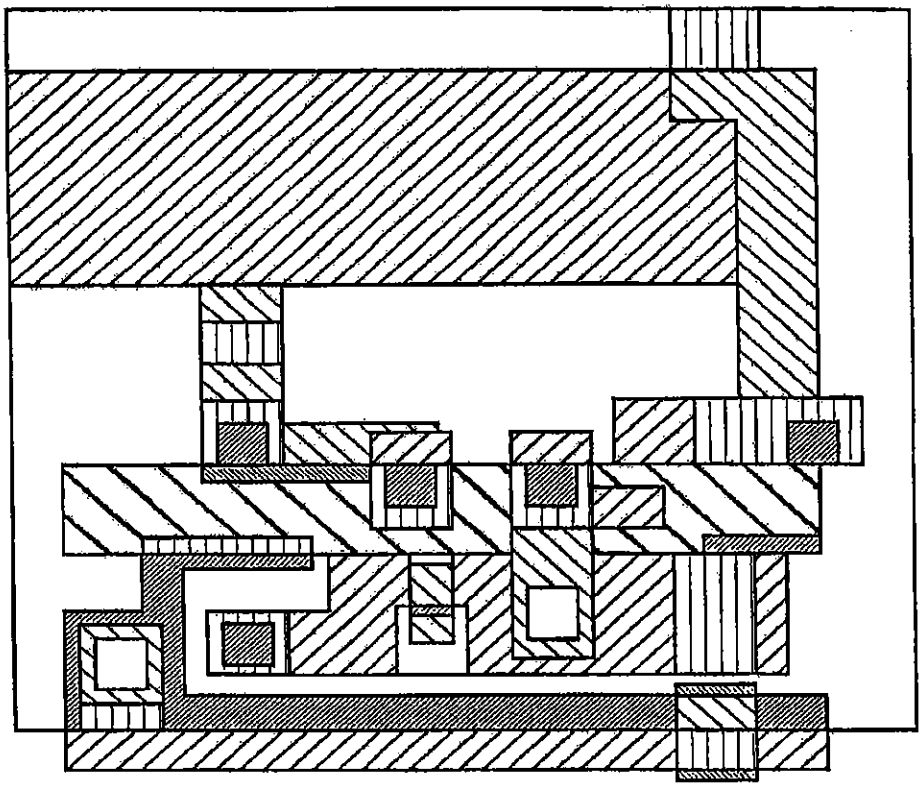

VS_OUT
VR_OUT
READ
FRAME
256 x 256 PIXEL ARRAY
COLUMN SIGNAL CONDITIONING
DECODER
COUNTER
LATCHES
ROW DRIVERS
DECODER
COUNTER
LATCHES
TIMING & CONTROL
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
MODE
−5V

FIG. 8



Array Size	256 x 256
Pixel Size	20.4 μm
Technology	1.2 μm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16 x 10^9 clock periods or 1600 secs at 10 MHz

FIG. 9

SINGLE CHIP CAMERA DEVICE HAVING DOUBLE SAMPLING OPERATION

This is a divisional of U.S. application Ser. No. 09/120,856, filed Jul. 21, 1998, which is a continuation of U.S. application Ser. No. 08/789,608, filed Jan. 24, 1997 U.S. Pat. No. 5,841,126 which is a continuation-in-part of U.S. application Ser. No. 08/558,521, filed Nov. 16, 1995, U.S. Pat. No. 6,101,232 which is a continuation of U.S. application Ser. No. 08/188,032, filed Jan. 28, 1994, now U.S. Pat. No. 5,471,515, and claim priority from Provisional application Ser. No. 60/010,678, filed Jan. 26, 1996.

ORIGIN

The invention described herein was made in performance of work under NASA contract and is subject to the provisions of Public Law 96–517 (35 USC 202) in which the contractor has elected to retain title.

FIELD OF THE INVENTION

The present invention relates to a single chip imaging sensor.

BACKGROUND AND SUMMARY OF THE INVENTION

Imaging technology is the science of converting an image to a signal indicative thereof. Imaging systems have broad applications in many fields, including commercial, consumer, industrial, medical, defense and scientific markets.

The original image sensors included an array of photosensitive elements in series with switching elements. Each photosensitive element received an image of a portion of the scene being imaged. That portion is called a picture element or pixel. The image obtaining elements produce an electrical signal indicative of the image plus a noise component. Various techniques have been used in the art to minimize the noise, to thereby produce an output signal that closely follows the image.

Size minimization is also important. The development of the solid state charge coupled device ("CCD") in the early 1970's led to more compact image systems. CCDs use a process of repeated lateral transfer of charge in an MOS electrode-based analog shift register. Photo-generated signal electrons are read after they are shifted into appropriate positions. However, the shifting process requires high fidelity and low loss. A specialized semiconductor fabrication process was used to obtain these characteristics.

CCDs are mostly capacitive devices and hence dissipate very little power. The major power dissipation in a CCD system is from the support electronics. One reason for this problem is because of the realities of forming a CCD system.

The specialized semiconductor fabrication process alluded to above is not generally CMOS compatible. Hence, the support circuitry for such a CCD has been formed using control electronics which were not generally CMOS compatible. The control electronics have dissipated an inordinate percentage of the power in such imaging devices. For example, CCD-based camcorder imaging systems typically operate for an hour on an 1800 mA-hr 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Approximately 8 watts of this is dissipated in the imaging system. The rest is used by the tape recording system, display, and autofocus servos.

Space-based imaging systems often have similar problems. The space based systems operate at lower pixel rates,

but with a lower degree of integration, and typically dissipate 20 watts or more.

The CCD has many characteristics which cause it to act like a chip-sized MOS capacitor. The large capacitance of the MOS device, for example, requires large clock swings, ΔV, of the order of 5–15 V to achieve high charge transfer efficiency. The clock drive electronics dissipation is proportional to $C\Delta V^2 f$, and hence becomes large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with their attendant inefficiencies in conversion.

Signal chain electronics that perform correlated double sampling ("CDS") for noise reduction and amplification, and especially analog to digital converters (ADC), also dissipate significant power.

The inventors also noted other inefficiencies in imaging systems. These inefficiencies included Fill factor inefficiencies, fixed pattern noise, clock pick up, temporal noise and large pixel size.

Active pixel sensors, such as described in U.S. Pat. No. 5,471,515, the disclosure of which is incorporated by reference herein, use special techniques to integrate both the photodetector and the readout amplifier into the pixel area or adjacent the pixel area. This allows the signal indicative of the pixel to be read out directly. These techniques have enabled use of a logic family whose fabrication processes are compatible with CMOS. This has enabled the controlling circuitry to be made from CMOS or some other low power-dissipating logic family.

The inventors of the present invention have recognized techniques and special efficiencies that are obtained by specialized support electronics that are integrated onto the same substrate as the photosensitive element. Aspects of the present invention include integration, timing, control electronics, signal chain electronics, A/D conversion, and other important control systems integrated on the same substrate as the photosensitive element.

It is hence an object of the present invention to provide for the integration of an entire imaging system on a chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a basic block diagram of a CMOS active pixel circuit;

FIG. 2 shows a graph of typical APS quantum efficiency;

FIG. 3 shows the block diagram of the overall chip including drivers and controlling structures;

FIGS. 4A and 4B show the timing diagrams for photogate operation and photodiode operation, respectively;

FIG. 5 shows a schematic of the active pixel sensor unit cell and readout circuitry;

FIG. 6 shows a timing diagram for setup and readout;

FIG. 7 shows a drawing of an actual layout of the pixel and control circuitry;

FIG. 8 shows a block diagram of a CMOS APS chip; and

FIG. 9 shows an exemplary pixel layout.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An active pixel sensor is herewith described with reference to FIGS. 1–4.

A block diagram of a CMOS active pixel circuit is shown in FIG. 1. The device has a pixel circuit 150, and a column circuit 155.

Incident photons pass through the photogate ("PG") **100** in the pixel circuit **150** and generate electrons which are integrated and stored under PG **100**. A number of the pixel circuits are arranged in each row of the circuit. One of the rows is selected for readout by enabling the row selection transistor **102** ("RS").

In the preferred embodiment, the floating diffusion output node **104** ("FD") is first reset by pulsing reset transistor ("RST") **106**. The resultant voltage on FD **104** is read out from the pixel circuitry onto the column bus **112** using the source follower **110** within the pixel. The voltage on the column bus **112** is sampled onto a first holding capacitor **114** by pulsing transistor SHR **116**. This initial charge is used as the baseline.

The signal charge is then transferred to FD **104** by pulsing PG **100** low. The voltage on FD **104** drops in proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus **112** is sampled onto a second capacitor **118** by pulsing SHR **120**. The difference between the voltages on first capacitor **114** and second capacitor **118** is therefore indicative of the number of photoelectrons that were allowed to enter the floating diffusion.

The capacitors **114, 118** are preferably 1–4 pf capacitors.

All pixels on a selected row are processed simultaneously and sampled onto capacitor at the bottom of their respective columns. The column-parallel sampling process typically takes 1–10 μsec, and preferably occurs during the so-called horizontal blanking interval of a video image.

Each column is successively selected for read-out by turning on column selection p-channel transistors ("CS") **130**. The p-channel source-followers **122, 124** in the column respectively drive the signal (SIG) and horizontal reset (RST) bus lines. These lines are loaded by p-channel load transistors which can be sent directly to a pad for off-chip drive, or can be buffered.

Noise in the sensor is preferably suppressed by the above-described correlated double sampling ("CDS") between the pixel output just after reset, before and after signal charge transfer to FD as described above. The CDS suppresses kTC noise from pixel reset, suppresses 1/f noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage.

The inventors found, however, that kTC noise may be reintroduced by sampling the signal onto the capacitors **114, 118** at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 140–170 μV/e-, corresponding to noise of the order or 13–25 electrons r.m.s. This is similar to noise obtained in most commercial CCDs, through scientific CCDs have been reported with read noise in the 3–5 electrons rms.

Typical biasing for each column's source-follower is 10 μA. This permits charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by cutting the voltage on each load transistor.

The sampling average power dissipation P_s corresponds to:

$$P_s = nIVd$$

where n is number of columns, I is the load transistor bias, V is the supply voltage, and d is the duty cycle. Using n=512, I=μA, V=5V and d=10%, a value for Ps of 2.5 mW is obtained.

A load current of 1 mA or more is needed to drive the horizontal bus lines at the video scan rate. The power dissipated is typically 5 mW.

Quantum efficiency measured in this CMOS APS array is similar to that for interline CCDs. A typical response curve is shown in FIG. 2. The inventors noticed from this that the quantum efficiency reflects significant responsivity in the "dead" part of the pixel; the part containing the readout circuitry rather than the photogate collector. The responsiveness was measured by intra-pixel laser spot scanning.

The inventors postulate the following reason. The transistor gate and channel absorb photons with short absorption lengths (i.e. blue/green). However, longer wavelength photons penetrate through these regions. The subsequently-generated carriers diffuse laterally and are subsequently collected by the photogate.

Thus, despite a fill factor of 25%–30%, the CMOS APS achieves quantum efficiencies that peak between 30%–35% in the red and near infrared. Microlenses are preferably added to refract photoelectrons from the dead cart to a live part and hence improve quantum efficiency.

An important feature of the system described herein is the integration of on-chip timing and control circuits within the same substrate that houses the pixel array and the signal chain electronics. A block diagram of the chip architecture is shown in FIG. **3**.

The analog outputs VS_out (signal) and VR_out (reset) are as described above. The digital outputs include FRAME and READ. Most of the inputs to the chip are asynchronous digital signals, as described herein.

The chip includes a pixel array **300**, which is driven by on-chip electronics. Timing and control circuit **302** drives row electronics **310**, and column electronics **320**.

The control circuits can command read-out of any area of interest within the array. Row decoder **312** controls row drivers **314** which can select a certain row for readout. A specific row is selected by entry of a row value **316** which is output from timing and control **302**. Row value **316** is stored in latch **318** which drives counter **319**. Counter **319** can allow selection of subsequent rows that follow the current row. Similarly, columns can be selected and accessed by latches **322**, counter **324**, decoder **326** and column signal conditioning **328**.

Each of the decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus **330**. Therefore, as described above, selection of a row commands pixels in that row to be transferred to the appropriate row decoding elements, e.g., capacitors. Preferably there is one capacitor associated with each column. This provides for the sequential readout of rows using the column. The capacitors are preferably included within the column signal conditioner **328**. Column decoders **326** also allow selection of only a certain column to be read. There are two parts of each column selection: where to start reading, and where to stop reading. Preferably the operation is carried out using counters and registers. A binary up-counter within the decoder **326** is preset to the start value. A preset number of rows is used by loading the 2's compliment. The up counter then counts up until an overflow.

An alternate loading command is provided using the DEFAULT LOAD input line **332**. Activation of this line forces all counters to a readout window of 128x128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set-by loading a 32-bit latch via the input data bus **330**. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. The counter can hence provide vary large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is tied to one-fourth

the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. The integration time is therefore equal to the delay time and the readout time for a 2.5 MHZ clock. The maximum delay time is 2^{32}/2.5 MHZ, or around 28 minutes. These values therefore easily allow obtaining a 30 Hz frame.

The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in FIGS. 4*a* and 4*b*. FIG. 4*a* shows an operation to operate in the photogate mode and FIG. 4*b* shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is V1, the output is V1 plus the threshold.

The column signal conditioning circuitry contains a double-delta sampling fixed pattern noise ("FPN") suppression stage that reduces FPN to below 0.2% sat with a random distribution. Since the APS is formed of a logic family that is compatible with CMOS, e.g., NMOS, the circuitry can be formed of CMOS. This allows power dissipation in the timing and control digital circuitry to be minimized and to scale with clock rate.

An active pixel sensor includes both a photodetector and the readout amplifier integrated within the same substrate as the light collecting device, e.g., the photodiode. The readout amplifier is preferably within and/or associated with a pixel.

A first embodiment of the present invention is a 128×128 CMOS photodiode type active pixel sensor that includes on chip timing, control and signal train electronics. A more detailed drawing of the chip is shown in FIG. 5. Asynchronous digital signals are converted by this chip to VS and VR analog outputs which are used to run the chip.

Pixel portion **500** includes a photodiode **502** which stores incident photons under photogate **504**. The photons are integrated as electrons within the photogate well. The output is buffered by follower **508**.

The rows are arranged into an array. A particular row is selected by the row transistor **514**. This allows the information from within the selected pixel **500** to be passed to the column decoder circuitry. Reset transistor **530** is connected to a sink **532**. Reset transistor is biased to a low potential level to allow all charge to bleed to sink **532**, and hence hold the stored charge in reset. The system is removed from reset by biasing the gate to a level as shown. This level is less than a highest possible potential to thereby allow charge which accumulates above that level to pass to sink **532**. Hence, the charge cannot overflow in an undesired way. This suppresses the blooming effect.

The depicted photogate system is driven according to the readout sequence shown in FIG **6**. A row is selected by activating row selecting transistor **514**. The cycle begins by sampling the signal present on each column pixel in that row. Sampling is initiated by biasing transistor **526** to place the signal from each column pixel in the row onto the holding capacitor **510**.

After the current pixel value has been transferred to the capacitor **510**, the pixel in the row is reset by biasing reset transistor to a low level, to photodiode **502** to the preset voltage sink **532**.

Correlated double sampling is effected by sampling the reset value, as a reset level, onto the holding capacitor **512**. This is done by activating the reset transistor **516**.

The voltage value of the reset branch of the column circuit is given by

$$Vcol_R=\beta\{\alpha[V_{pdr}-V_{tpix}]-V_{tcolr}\}$$

Where α is the gain of the pixel source follower **508**, β is the gain of the column source follower **526**, and V_{pdr} is the voltage on the photodiode after reset, V_{tpix} is the threshold voltage of the pixel source follower and channel transistor, and V_{tcolr} is the threshold voltage of the column source follower p-channel transistor.

Using similar reasoning, the output voltage of the signal branch of the column circuit is

$$Vcol_S=\beta\{\alpha[V_{pds}-V_{tpix}]-V_{tcols}\}$$

where V_{pds} is the voltage on the photodiode with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor.

The inventors have found experimentally that the peak-to-peak variation $V_{tcolr}-V_{tcols}$ is typically between 10 and 20 millivolts. This, however, is a source of column to column fixed pattern noise. The inventors herein suggest a double delta sampling technique to eliminate this column to column noise. The present approach represents an improved version of the previously-described double delta sampling circuitry. The operation proceeds as follows. A column is first selected. After a settling time equivalent to half of the column selection period, a special double delta sampling technique is performed to remove the column fixed pattern noise. Therefore, the varying thresholds on the different transistors cause varying outputs. According to this aspect, the threshold outputs of these transistors are equalized using a capacitor to equalize the charge. The capacitor is applied with the charge before and after the voltage change. Therefore, the output of the capacitor represents the difference between before and after, and the fixed pattern noise component drops out of the equation.

This system uses a DDS switch **520** and first and second column select switches **522**, **524** to short across the respective capacitors. All three switches are turned on to short across the two sample and hold capacitors **510**. This clamp operation is shown in line 8 of FIG. 6.

Prior to the DDS operation, the reset and signal column components, Vcol_R and Vcol_S include their signal values plus a source follower voltage threshold component from the appropriate source follower. The object of the special following circuit of the present invention is to remove that source follower threshold component. The operation proceeds as follows. Prior to the beginning of some operation, the capacitors are precharged through clamp transistors to a clamp voltage V_{cl}. This is maintained by turning on clamp transistors **550** and **552** to connect the appropriate capacitors to the voltage V_{cl}. The clamp operation is shown on line 8 of FIG. 6. Immediately after the clamp is released, the DDS transistors **520**, **522** and **524** are turned on. This has the effect of shorting across the capacitors **510** and **512**. When the transistors are shorted, the voltage that is applied to the output drivers **554**, **556** includes only the voltage threshold component. The differential amplification of the voltage render the output voltage free of the voltage threshold component. Mathematically, prior to clamp being deactivated, the output signals are:

$$VR_OUT=\gamma(V_{cl}-V_{tr})$$

and

$$VS_OUT=\gamma(V_{cl}-V_{ts})$$

where γ is the gain of the third stage source-follower, V_{cl} is the clamp voltage, and V_{tr} and V_{ts} are the threshold voltages of the third stage source-follower n-channel transistors, reset and signal branch respectively. Deactivation of the clamp circuit and simultaneous activation of the DDS switch causes several changes. The voltages in the two column branch sampling circuits equalize becoming:

$$V_{cs}=V_{cr}=\alpha[V_{pdr}-V_{tplx}+V_{pds}-V_{tplx}]/2$$

This in turn causes a change in Vcol_S and Vcol_R to:

$$Vcol_R'=\beta\{\alpha[V_{pdr}-V_{tplx}+V_{pds}-V_{tplx}]/2-V_{tcolr}\}$$

and

$$Vcol_S'=\beta\{\alpha[V_{pdr}-V_{tplx}+V_{pds}-V_{tplx}]/2-V_{tcolr}\}$$

Consequently, the voltage outputs change to:

$$VR_OUT=\gamma(V_{cl}-Vcol_R'-Vcol_R-V_{tr})$$

and

$$VS_OUT=\gamma(V_{cl}-Vcol_S'-Vcol_S-V_{ts})$$

We note

$$Vcol_S'-Vcol_S=\beta\{\alpha[V_{pds}-V_{pdr}]/2\}$$

and

$$Vcol_R'-Vcol_R=\beta\{\alpha[V_{pdr}-V_{pds}]/2\}$$

When the outputs are differentially amplified off-chip, the common clamp voltage Vcl is removed, leaving only the difference between signal and reset. The net differential output voltage is given by:

$$VP_out=VS_OUT=\alpha\beta\gamma(V_{pdr}-V_{pds}=V_{sensit})$$

FIG. 7 shows the layout of the pixel for 128x128 array size device. This system formed a 19.2 micron pixel size using 1.2 μm n-well CMOS. The maximum clock rate is 10 MHZ, the maximum pixel rate is 2.5 MHZ and maximum integration delay is 1.6×10^9 clock periods.

A second embodiment uses similar design techniques to produce a 256x256 array size. This embodiment also uses a pixel with a photogate imaging element along with four transistors to perform the functions of readout, selection, and reset. Readout is preferably achieved using a column parallel architecture which is multiplexed one row at a time and then one column at a time through an on-chip amplifier/buffer. An important part of this embodiment,like the first embodiment, is the use of a chip common logic elements to control row and address decoders and delay counters.

This embodiment allows use in three modes of operation: Photogate mode, photodiode mode and differencing mode. The photogate mode is the standard mode for this chip. The photodiode mode alters the readout timing to be similar to that for photodiode operation. The differencing mode alters the readout timing in such a way that the value of each pixel output is the difference between the current frame and the previous frame. The chip inputs that are required are a single +5 V power supply, start command, and parallel data load commands for defining integration time and windowing parameters. The output has two differential analog channels.

The second embodiment uses the block diagram of the chip architecture shown in FIG. 8. The analog outputs of VS_OUT (signal) and VR_OUT (reset), and digital outputs of FRAME and READ. The inputs to the chip are asynchronous digital signals. The chip includes addressing circuitry allowing readout of any area of interest within the 256x256 array. The decoder includes counters that are preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 256x256.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. This counter allows forming very large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is tied to one fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 HZ frame rate can be achieved without difficulty.

The chip is idle when the RUN command is deactivated. This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

The 255x256 CMOS APS uses a system having a similar block diagram to those described previously. The pixel unit cell has a photogate (PG), a source-follower input transistor, a row selection transistor and a reset transistor. A load transistor VLN and two cutout branches to store the reset and signal levels are located at the bottom of each column of pixels. Each branch has a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel.

A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) and the reset value is sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate in the row is transferred to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capacitor CS. These signals are then placed on the output data bus by the column select circuitry. In the Photodiode mode this process, is reversed; first the charge under the photogate is read out and then the reset level is sampled. This non-correlated double sampling mode would be primarily used with a photodiode, i.e., non active pixel sensor, pixel.

In the differencing mode, the capacitors CS and CR are used to store the signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: Rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other

sample and hold capacitor. The difference between these two signals is now the frame to frame difference.

A simplified expression for the output of the reset branch of the column circuit is given by:

$$Vcol_R=\beta\{\alpha[Vr-V_{epix}]-V_{tcolr}\}$$

where α is the gain of the pixel source-follower, β is the gain of the column source-follower, Vr is the voltage on the floating diffusion after reset, V_{epix} is the threshold voltage of the pixel source-follower n-channel transistor, and V_{tcolr} is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output voltage of the signal branch of the column circuit is given by:

$$Vcol_S=\beta\{\alpha[V_s-V_{epix}]-V_{tcols}\}$$

where V_s is the voltage on the floating diffusion with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak to peak variation in $V_{tcolr}-V_{tcols}$ is typically 10–20 mV. It is desirable to remove this source of column-to-column fixed pattern noise FPN, JPL has previously developed a double delta sampling (DDS) technique to eliminate the column-to-column FPN. This approach represented an improved version of the DDS circuitry.

Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent to one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal outputs (Vcol_R and VCOL_S) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers (VR_OUT and VS_OUT) that is free of the voltage threshold component.

This chip uses a similar pixel cell to that shown in FIG. 5. FIG. 9 shows the layout of the pixel cell. PG and RESET are routed horizontally in polysilicon while the pixel output is routed vertically in metal. Metal2 was routed within the pixel for row selection. Metal2 was also used as a light shield and covers most of the active area outside of the pixel array. The designed fill factor of the pixel is approximately 21%.

According to another feature, a logo can be formed on the acquired image by using a light blocking metal light shield. The light shield is formed to cover certain pixels in the shape of the logo to be applied. This blocks out those underlying pixels in the array, thereby forming a logo in the shape of the blocked pixels.

The output saturation level of the sensor is 800 mv when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the floating diffusion node (e.g. 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 75,000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47,000 e– per supply volt.

Dark current was measured at less than 500 pA/cm^2.

Conversion gain (μV/e–) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1%-similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer.

The quantum efficiency of the detector was measured using a CVI ¼ m monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards.

What is claimed is:

1. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors to read at least one element of the array by first reading a reset level of said at least one element, and subsequently, after an integration time, second reading a charged level of said at least one photoreceptor, said reading and said second reading producing output signals based on both said charged level and said reset level.

2. A single chip camera device as in claim 1 wherein an output signal is equal to said charged level minus said reset level.

3. A camera device as in claim 1, wherein said signal controlling device includes a column-parallel read out device, which reads out a column of said photoreceptors at substantially the same time.

4. A camera device as in claim 1, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

5. A camera device as in claim 4, wherein said readout amplifier is preferably within and/or associated with one element of the array.

6. A camera device as in claim 4, wherein said photoreceptors are photodiodes.

7. A camera device as in claim 4, wherein said photoreceptors are photogates.

8. A camera device as in claim 1, further comprising a mode selector device, selecting a mode of operation of said chip.

9. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors to read at least one element of the array by first reading a reset level of said at least one element, and subsequently, after an integration time, second reading a charged level of said at least one photoreceptor, said

reading and said second reading producing output signals based on both said charged level and said reset level, further comprising a mode selector device, selecting a mode of operation of said chip wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

10. A camera device as in claim 9, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

11. A camera device as in claim 1, wherein said timing circuit allows changing an integration time for said array of photoreceptors by changing a time interval between said first and second reading.

12. A camera device as in claim 1, further comprising fixed pattern noise reduction circuits, on chip.

13. A camera device as in claim 1, further comprising a noise reduction circuit.

14. A camera device as in claim 13, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

15. A camera device as in claim 13, wherein said noise reduction circuit is a fixed pattern noise reduction circuit.

16. A camera device as in claim 13, wherein said noise reduction circuit is a column to column fixed pattern noise reduction circuit.

17. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors with output nodes, and a signal controlling device, controlling said photoreceptors and a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

resetting said output nodes;

sampling a reset value as a first sample;

allowing said photoreceptors to accumulate charge, after resetting said output nodes;

sampling said output nodes after accumulating said charge, producing output signals indicative of a difference between said reset value and said sampled value after accumulating said charge.

18. A method in claim 17 wherein said reset level is sampled during a blanking interval of the video signal.

* * * * *

EXHIBIT C

US006549235B1

(12) **United States Patent**
Fossum et al.

(10) **Patent No.: US 6,549,235 B1**
(45) **Date of Patent: *Apr. 15, 2003**

(54) **SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE SENSOR**

(75) Inventors: **Eric R. Fossum**, La Crescenta; **Robert Nixon**, Shadow Hills, both of CA (US)

(73) Assignee: **California Institute of Technology**, Pasadena, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/120,856**

(22) Filed: **Jul. 21, 1998**

Related U.S. Application Data

(63) Continuation of application No. 08/188,032, filed on Jan. 28, 1994, now Pat. No. 5,471,515, and a continuation of application No. 08/789,608, filed on Jan. 24, 1997, now Pat. No. 5,841,126.

(60) Provisional application No. 60/010,678, filed on Jan. 26, 1996.

(51) **Int. Cl.**[7] **H04N 5/335**

(52) **U.S. Cl.** **348/308**; 348/294

(58) **Field of Search** 348/301, 307, 348/308, 294, 297, 300, 302; 250/208.1; 257/443, 441, 292, 291, 290; H04N 5/335

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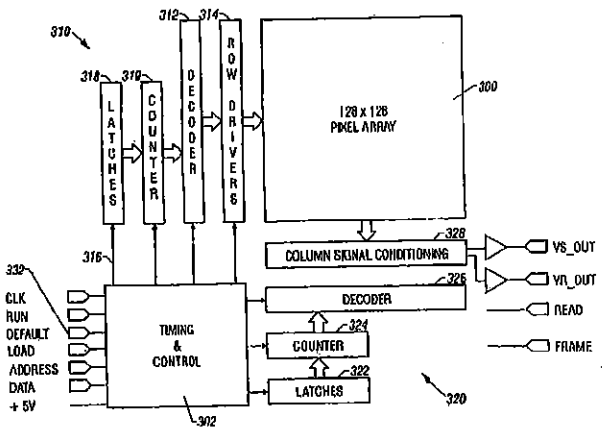
(57) **ABSTRACT**

Single substrate device is formed to have an image acquisition device and a controller. The controller on the substrate controls the system operation.

66 Claims, 10 Drawing Sheets



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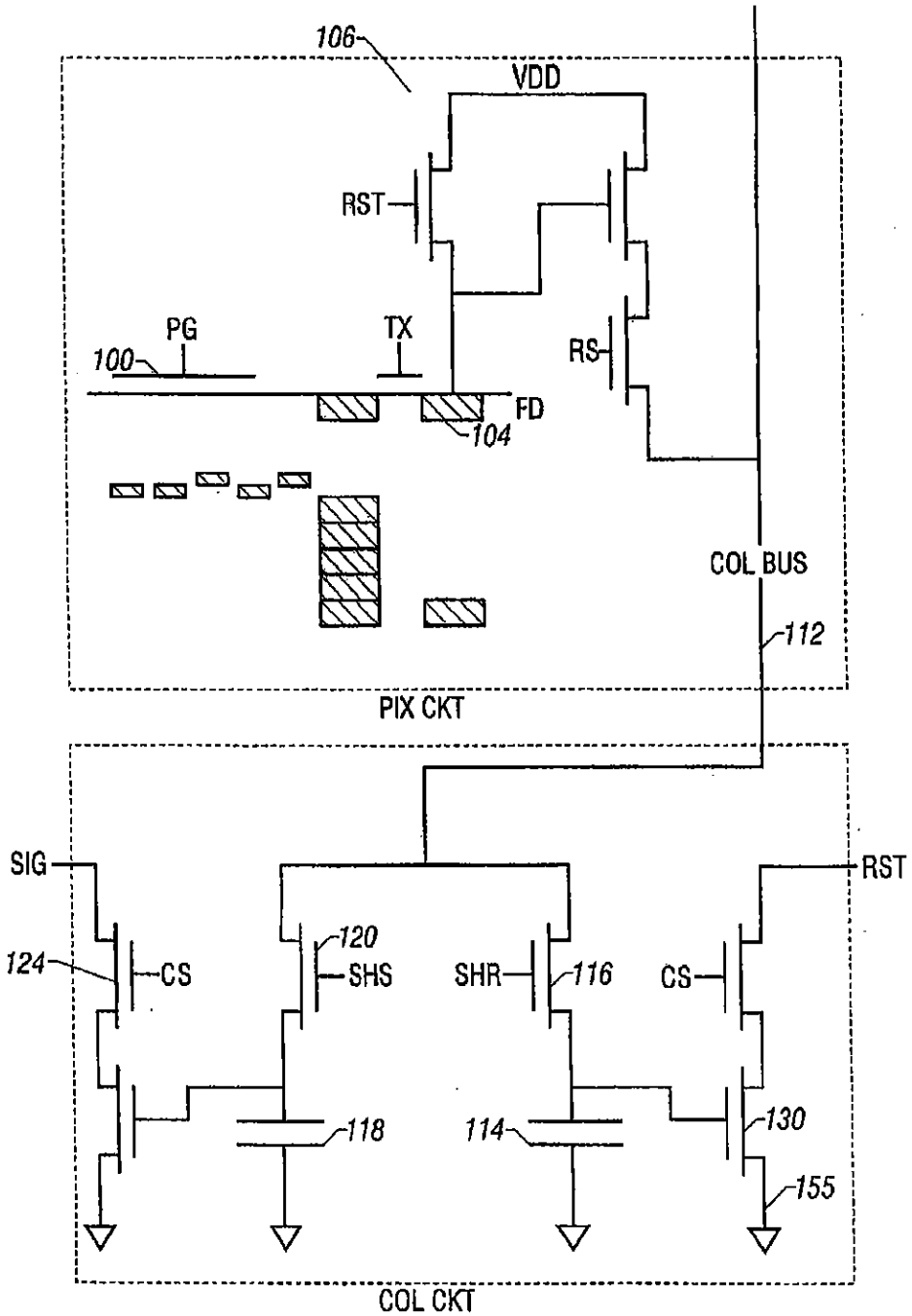

106
VDD
RST
PG
TX
RS
100
FD
104
COL BUS
112
PIX CKT
SIG
RST
124
CS
120
SHS
SHR
116
CS
118
114
130
155
COL CKT

FIG. 1

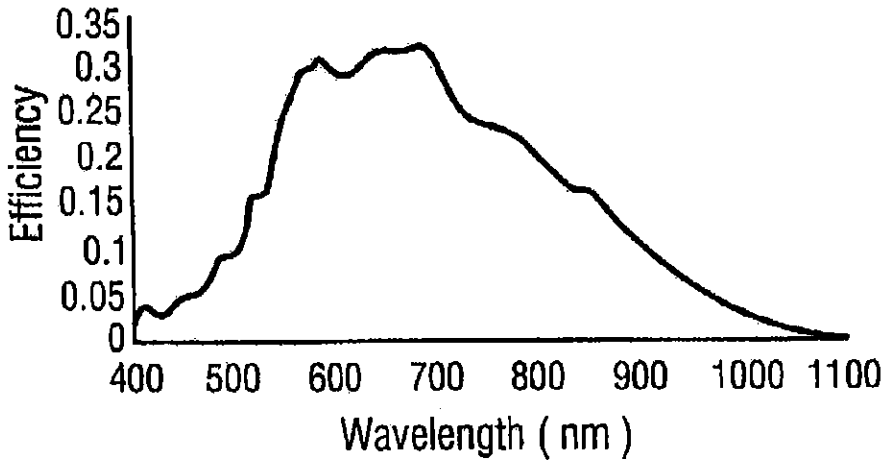

Efficiency
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
400
500
600
700
800
900
1000
1100
Wavelength (nm)

FIG. 2

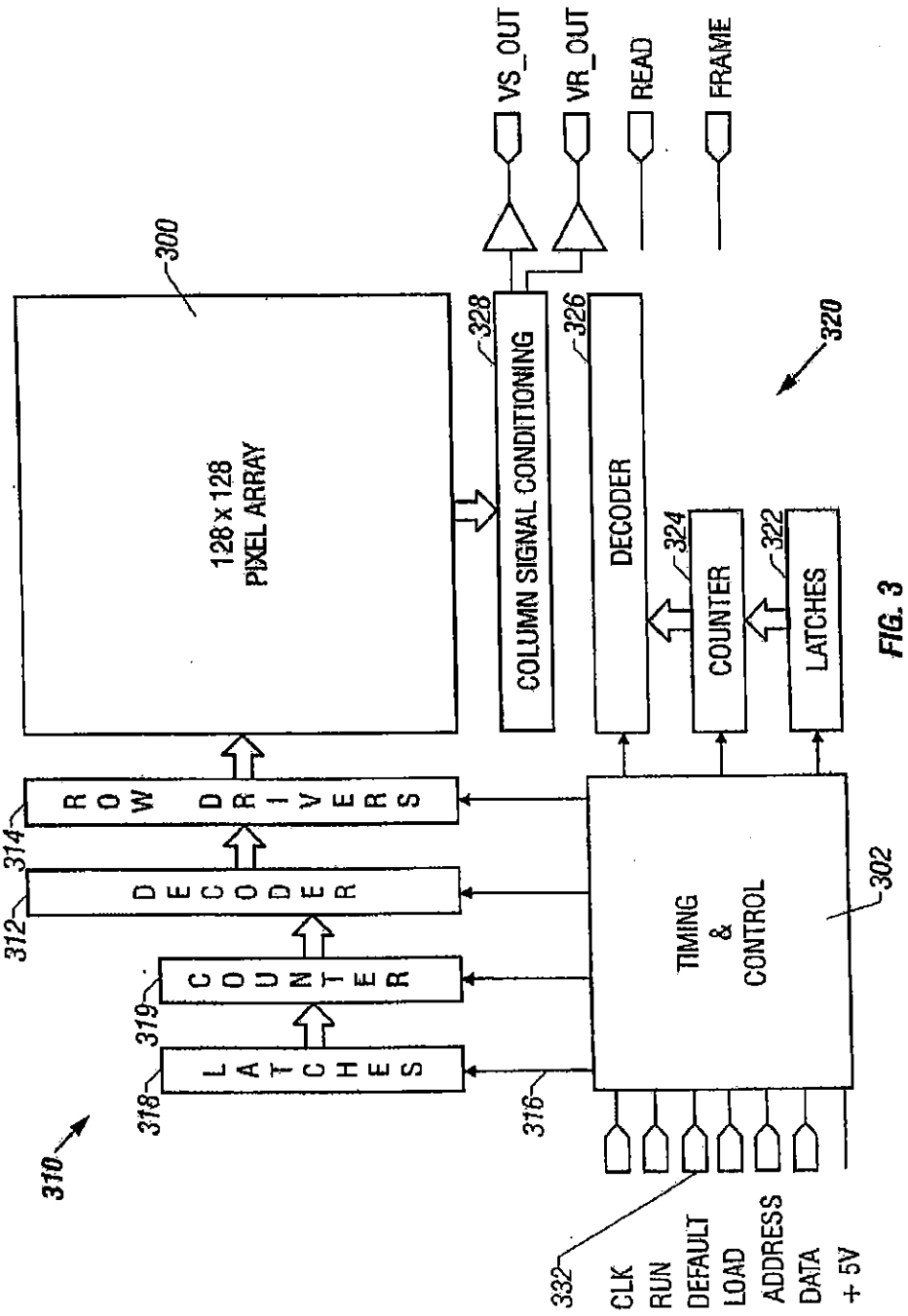

VS_OUT
VR_OUT
READ
FRAME
300
128 x 128 PIXEL ARRAY
328
COLUMN SIGNAL CONDITIONING
326
DECODER
320
324
COUNTER
322
LATCHES
ROW DRIVERS
314
DECODER
312
COUNTER
319
LATCHES
318
310
316
TIMING & CONTROL
302
332
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
+ 5V

FIG. 3

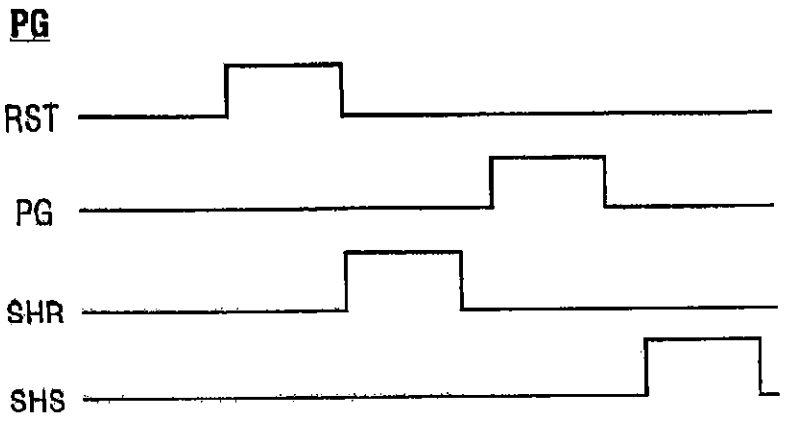


FIG. 4A

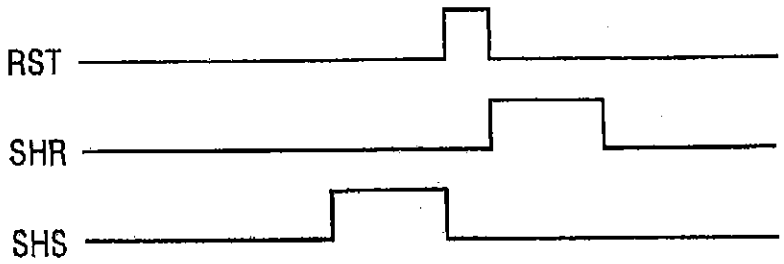


FIG. 4B

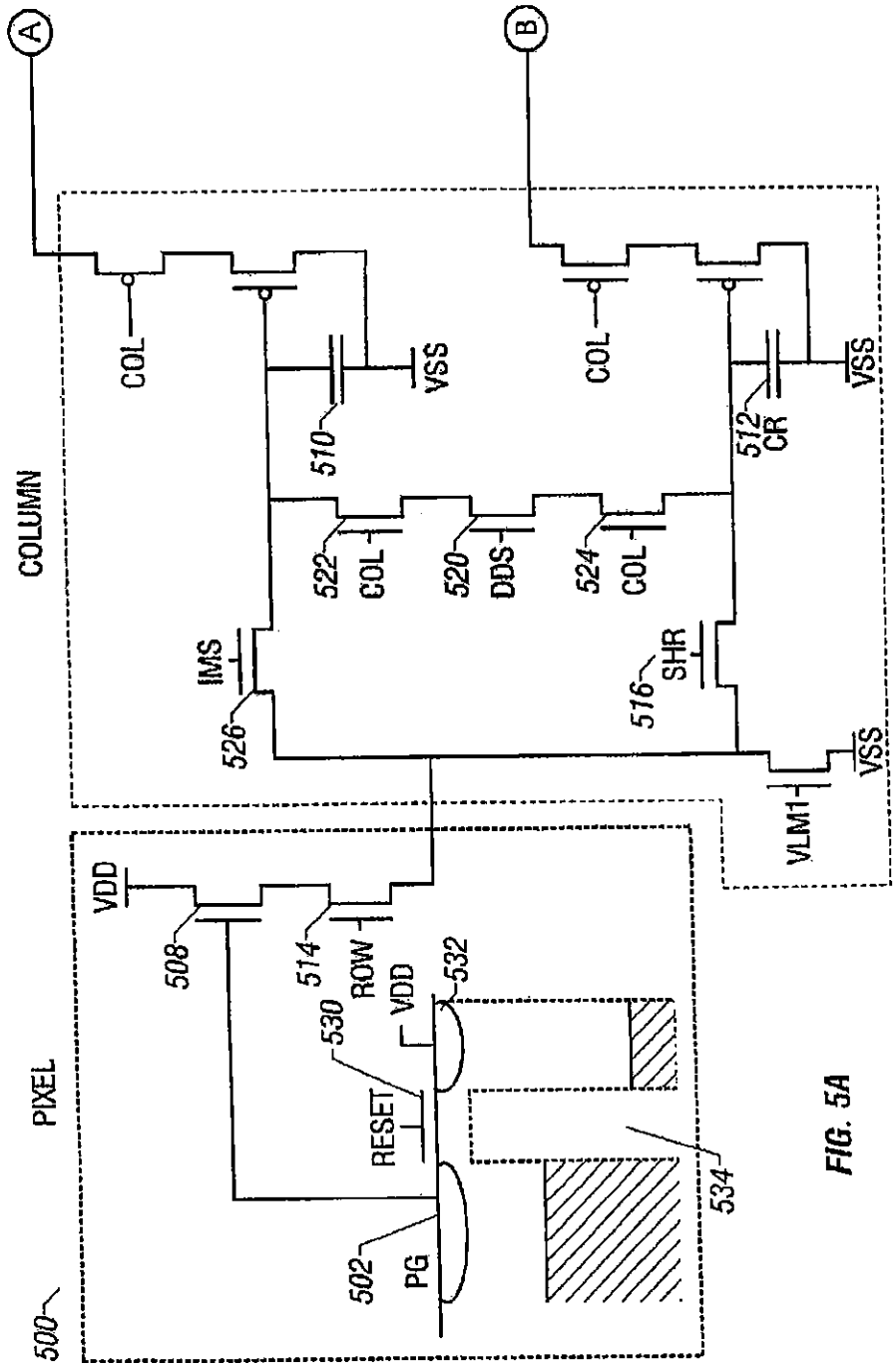

A
B
COL
VSS
510
COL
VSS
512
CR
COLUMN
522
COL
520
DDS
524
COL
IMS
526
SHR
516
VSS
VLM1
VDD
508
514
ROW
VDD
532
530
RESET
534
PG
502
PIXEL
500

FIG. 5A

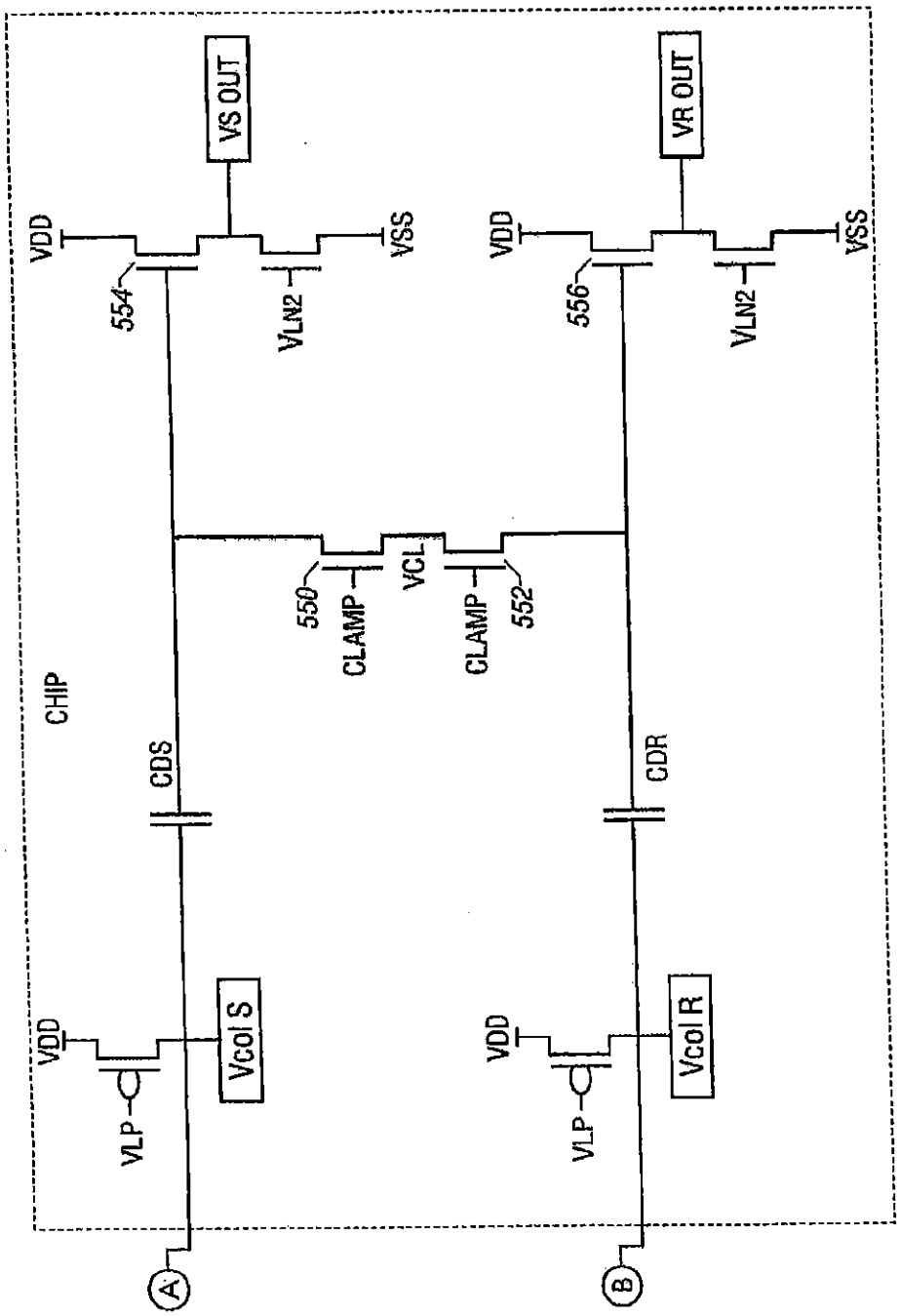

VS OUT
VR OUT
VDD
VSS
554
556
VLN2
550
CLAMP
VCL
552
CHIP
CDS
CDR
VCol S
VCol R
VLP
A
B

FIG. 5B

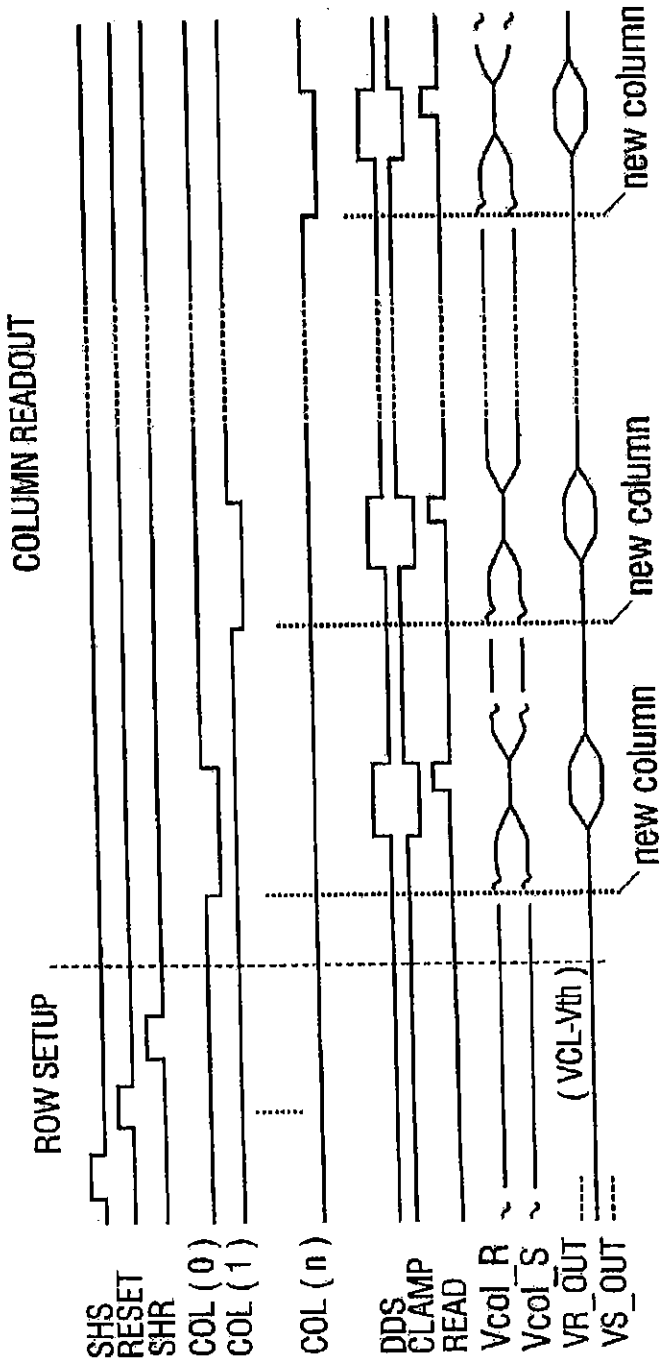

COLUMN READOUT
ROW SETUP
SHS
RESET
SHR
COL (0)
COL (1)
COL (n)
DDS
CLAMP
READ
Vcol_R
Vcol_S
VR_OUT
VS_OUT
(VCL-Vth)
new column
new column
new column

FIG. 6

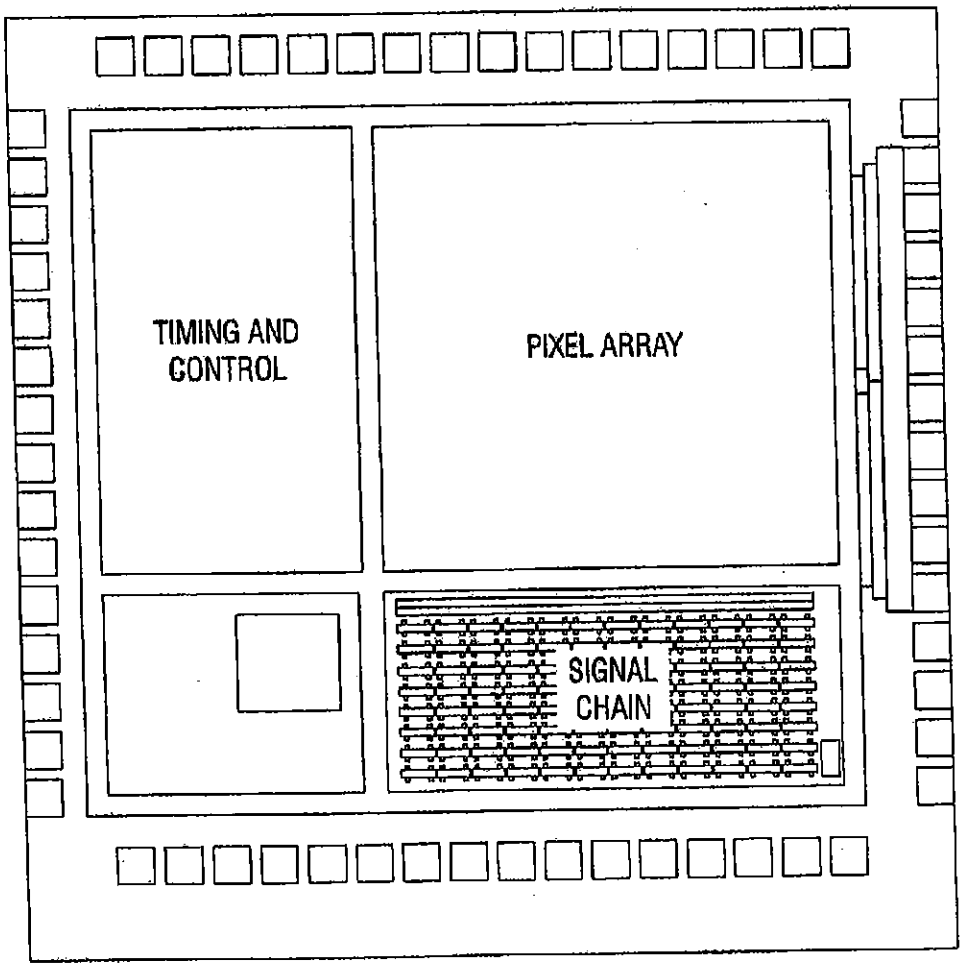


FIG. 7

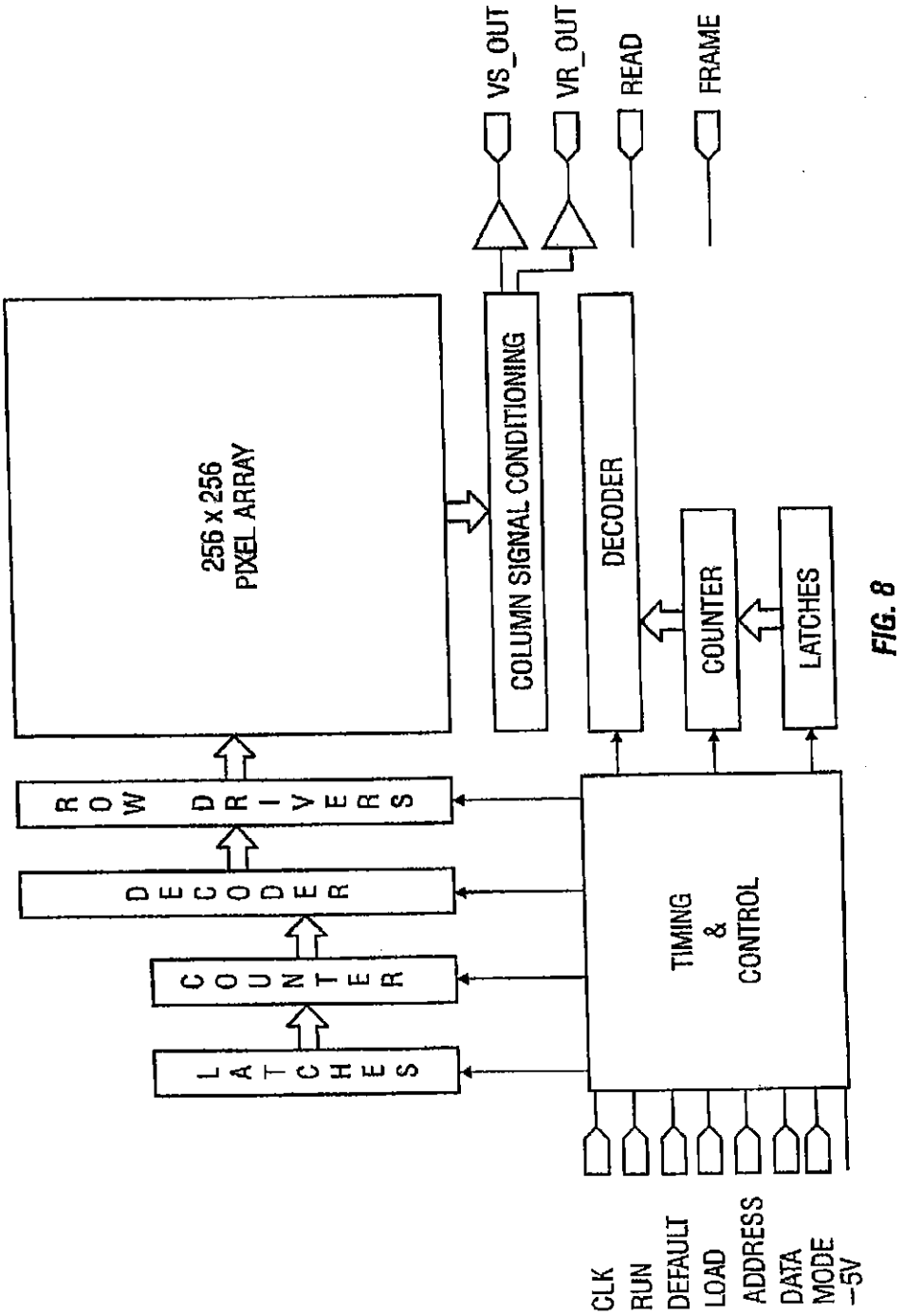
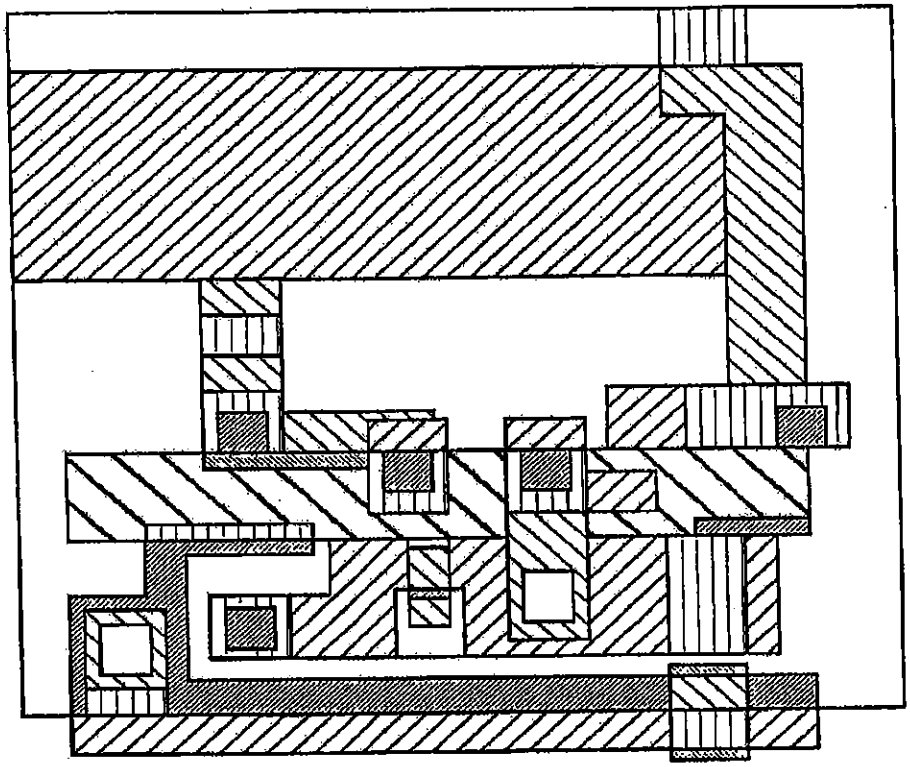

VS_OUT
VR_OUT
READ
FRAME
256 x 256
PIXEL ARRAY
COLUMN SIGNAL CONDITIONING
DECODER
COUNTER
LATCHES
ROW DRIVERS
DECODER
COUNTER
LATCHES
TIMING
&
CONTROL
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
MODE
-5V

FIG. 8



Array Size	256 x 256
Pixel Size	20.4 μm
Technology	1.2 μm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16 x 10^9 clock periods or 1600 secs at 10 MHz

FIG. 9

SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE SENSOR

This is a continuation of U.S. application Ser. No. 08/188,132, filed Jan. 28, 1994 U.S. Pat. No. 5,471,515; provisional application Ser. No. 60/010,678, filed Jan. 26, 1996; and, Ser. No. 08/789,608, filed Jan. 24, 1997 U.S. Pat. No. 5,841,126.

ORIGIN

The invention described herein was made in performance of work under NASA contract and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the contractor has elected to retain title.

FIELD OF THE INVENTION

The present invention relates to a single chip imaging sensor.

BACKGROUND AND SUMMARY OF THE INVENTION

Imaging technology is the science of converting an image to a signal indicative thereof. Imaging systems have broad applications in many fields, including commercial, consumer, industrial, medical, defense and scientific markets.

The original image sensors included an array of photosensitive elements in series with switching elements. Each photosensitive element received an image of a portion of the scene being imaged. That portion is called a picture element or pixel. The image obtaining elements produce an electrical signal indicative of the image plus a noise component. Various techniques have been used in the art to minimize the noise, to thereby produce an output signal that closely follows the image.

Size minimization is also important. The development of the solid state charge coupled device ("CCD") in the early 1970's led to more compact image systems. CCDs use a process of repeated lateral transfer of charge in an MOS electrode-based analog shift register. Photo-generated signal electrons are read after they are shifted into appropriate positions. However, the shifting process requires high fidelity and low loss. A specialized semiconductor fabrication process was used to obtain these characteristics.

CCDs are mostly capacitive devices and hence dissipate very little power. The major power dissipation in a CCD system is from the support electronics. One reason for this problem is because of the realities of forming a CCD system.

The specialized semiconductor fabrication process alluded to above is not generally CMOS compatible. Hence, the support circuitry for such a CCD has been formed using control electronics which were not generally CMOS compatible. The control electronics have dissipated an inordinate percentage of the power in such imaging devices. For example, CCD-based camcorder imaging systems typically operate for an hour on an 1800 mA-hr 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Approximately 8 watts of this is dissipated in the imaging system. The rest is used by the tape recording system, display, and autofocus servos.

Space-based imaging systems often have similar problems. The space based systems operate at lower pixel rates, but with a lower degree of integration, and typically dissipate 20 watts or more.

The CCD has many characteristics which cause it to act like a chip-sized MOS capacitor. The large capacitance of the MOS device, for example, requires large clock swings, ΔV, of the order of 5–15 V to achieve high charge transfer efficiency. The clock drive electronics dissipation is proportional to $C\Delta V^2 f$, and hence becomes large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with their attendant inefficiencies in conversion.

Signal chain electronics that perform correlated double sampling ("CDS") for noise reduction and amplification, and especially analog to digital converters (ADC), also dissipate significant power.

The inventors also noted other inefficiencies in imaging systems. These inefficiencies included fill factor inefficiencies, fixed pattern noise, clock pick up, temporal noise and large pixel size.

Active pixel sensors, such as described in U.S. Pat. No. 5,471,515, the disclosure of which is incorporated by reference herein, use special techniques to integrate both the photodetector and the readout amplifier into the pixel area or adjacent the pixel area. This allows the signal indicative of the pixel to be read out directly. These techniques have enabled use of a logic family whose fabrication processes are compatible with CMOS. This has enabled the controlling circuitry to be made from CMOS or some other low power-dissipating logic family.

The inventors of the present invention have recognized techniques and special efficiencies that are obtained by specialized support electronics that are integrated onto the same substrate as the photosensitive element. Aspects of the present invention include integration, timing, control electronics, signal chain electronics, A/D conversion, and other important control systems integrated on the same substrate as the photosensitive element.

It is hence an object of the present invention to provide for the integration of an entire imaging system on a chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a basic block diagram of a CMOS active pixel circuit;

FIG. 2 shows a graph of typical APS quantum efficiency;

FIG. 3 shows the block diagram of the overall chip including drivers and controlling structures;

FIGS. 4A and 4B show the timing diagrams for photogate operation and photodiode operation, respectively;

FIG. 5 shows a schematic of the active pixel sensor unit cell and readout circuitry;

FIG. 6 shows a timing diagram for setup and readout;

FIG. 7 shows a drawing of an actual layout of the pixel and control circuitry;

FIG. 8 shows a block diagram of a CMOS APS chip; and

FIG. 9 shows an exemplary pixel layout.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An active pixel sensor is herewith described with reference to FIGS. 1–4.

A block diagram of a CMOS active pixel circuit is shown in FIG. 1. The device has a pixel circuit 150, and a column circuit 155.

Incident photons pass through the photogate ("PG") 100 in the pixel circuit 150 and generate electrons which are integrated and stored under PG 100. A number of the pixel circuits are arranged in each row of the circuit. One of the

rows is selected for readout by enabling the row selection transistor **102** ("RS").

In the preferred embodiment, the floating diffusion output node **104** ("FD") is first reset by pulsing reset transistor ("RST") **106**. The resultant voltage on FD **104** is read out from the pixel circuitry onto the column bus **112** using the source follower **110** within the pixel. The voltage on the column bus **112** is sampled onto a first holding capacitor **114** by pulsing transistor SHR **116**. This initial charge is used as the baseline.

The signal charge is then transferred to FD **104** by pulsing PG **100** low. The voltage on FD **104** drops in proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus **112** is sampled onto a second capacitor **118** by pulsing SHR **120**. The difference between the voltages on first capacitor **114** and second capacitor **118** is therefore indicative of the number of photoelectrons that were allowed to enter the floating diffusion.

The capacitors **114, 118** are preferably 1–4 pf capacitors.

All pixels on a selected row are processed simultaneously and sampled onto capacitor at the bottom of their respective columns. The column-parallel sampling process typically takes 1–10 μsec, and preferably occurs during the so-called horizontal blanking interval of a video image.

Each column is successively selected for read-out by turning on column selection p-channel transistors ("CS") **130**. The p-channel source-followers **122, 124** in the column respectively drive the signal (SIG) and horizontal reset (RST) bus lines. These lines are loaded by p-channel load transistors which can be sent directly to a pad for off-chip drive, or can be buffered.

Noise in the sensor is preferably suppressed by the above-described correlated double sampling ("CDS") between the pixel output just after reset, before and after signal charge transfer to FD as described above. The CDS suppresses kTC noise from pixel reset, suppresses 1/f noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage.

The inventors found, however, that kTC noise may be reintroduced by sampling the signal onto the capacitors **114, 118** at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 140–170 μV/e–, corresponding to noise of the order of 13–25 electrons r.m.s. This is similar to noise obtained in most commercial CCDs, through scientific CCDs have been reported with read noise in the 3–5 electrons rms.

Typical biasing for each column's source-follower is 10 μA. This permits charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by cutting the voltage on each load transistor.

The sampling average power dissipation P_s corresponds to:

$$P_s = nIVd$$

where n is number of columns, I is the load transistor bias, V is the supply voltage, and d is the duty cycle. Using n=512, I=μA, V=5V and d=10%, a value for Ps of 2.5 mW is obtained.

A load current of 1 mA or more is needed to drive the horizontal bus lines at the video scan rate. The power dissipated is typically 5 mW.

Quantum efficiency measured in this CMOS APS array is similar to that for interline CCDs. A typical response curve is shown in FIG. 2. The inventors noticed from this that the quantum efficiency reflects significant responsivity in the "dead" part of the pixel; the part containing the readout circuitry rather than the photogate collector. The responsiveness was measured by intra-pixel laser spot scanning.

The inventors postulate the following reason. The transistor gate and channel absorb photons with short absorption lengths (i.e. blue/green). However, longer wavelength photons penetrate through these regions. The subsequently-generated carriers diffuse laterally and are subsequently collected by the photogate.

Thus, despite a fill factor of 25%–30%, the CMOS APS achieves quantum efficiencies that peak between 30%–35% in the red and near infrared. Microlenses are preferably added to refract photoelectrons from the dead part to a live part and hence improve quantum efficiency.

An important feature of the system described herein is the integration of on-chip timing and control circuits within the same substrate that houses the pixel array and the signal chain electronics. A block diagram of the chip architecture is shown in FIG. **3**.

The analog outputs VS_out (signal) and VR_out (reset) are as described above. The digital outputs include FRAME and READ. Most of the inputs to the chip are asynchronous digital signals, as described herein.

The chip includes a pixel array **300**, which is driven by on-chip electronics. Timing and control circuit **302** drives row electronics **310**, and column electronics **320**.

The control circuits can command read-out of any area of interest within the array. Row decoder **312** controls row drivers **314** which can select a certain row for readout. A specific row is selected by entry of a row value **316** which is output from timing and control **302**. Row value **316** is stored in latch **318** which drives counter **319**. Counter **319** can allow selection of subsequent rows that follow the current row. Similarly, columns can be selected and accessed by latches **322**, counter **324**, decoder **326** and column signal conditioning **328**.

Each of the decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus **330**. Therefore, as described above, selection of a row commands pixels in that row to be transferred to the appropriate row decoding elements, e.g., capacitors. Preferably there is one capacitor associated with each column. This provides for the sequential readout of rows using the column. The capacitors are preferably included within the column signal conditioner **328**. Column decoders **326** also allow selection of only a certain column to be read. There are two parts of each column selection: where to start reading, and where to stop reading. Preferably the operation is carried out using counters and registers. A binary up-counter within the decoder **326** is preset to the start value. A preset number of rows is used by loading the 2's compliment. The up counter then counts up until an overflow.

An alternate loading command is provided using the DEFAULT LOAD input line **332**. Activation of this line forces all counters to a readout window of 128x128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus **330**. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. The counter can hence provide vary large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration

time. The integration time is therefore equal to the delay time and the readout time for a 2.5 MHZ clock. The maximum delay time is $2^{32}/2.5$ MHZ, or around 28 minutes. These values therefore easily allow obtaining a 30 Hz frame.

The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in FIGS. 4*a* and 4*b*. FIG. 4*a* shows an operation to operate in the photogate mode and FIG. 4*b* shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is V1, the output is V1 plus the threshold.

The column signal conditioning circuitry contains a double-delta sampling fixed pattern noise ("FPN") suppression stage that reduces FPN to below 0.2% sat with a random distribution. Since the APS is formed of a logic family that is compatible with CMOS, e.g., NMOS, the circuitry can be formed of CMOS. This allows power dissipation in the timing and control digital circuitry to be minimized and to scale with clock rate.

An active pixel sensor includes both a photodetector and the readout amplifier integrated within the same substrate as the light collecting device, e.g., the photodiode. The readout amplifier is preferably within and/or associated with a pixel.

A first embodiment of the present invention is a 128×128 CMOS photodiode type active pixel sensor that includes on chip timing, control and signal train electronics. A more detailed drawing of the chip is shown in FIG. 5. Asynchronous digital signals are converted by this chip to VS and VR analog outputs which are used to run the chip.

Pixel portion **500** includes a photodiode **502** which stores incident photons under photogate **504**. The photons are integrated as electrons within the photogate well. The output is buffered by follower **508**.

The rows are arranged into an array. A particular row is selected by the row transistor **514**. This allows the information from within the selected pixel **500** to be passed to the column decoder circuitry. Reset transistor **530** is connected to a sink **532**. Reset transistor is biased to a low potential level to allow all charge to bleed to sink **532**, and hence hold the stored charge in reset. The system is removed from reset by biasing the gate to a level as shown. This level is less than a highest possible potential to thereby allow charge which accumulates above that level to pass to sink **532**. Hence, the charge cannot overflow in an undesired way. This suppresses the blooming effect.

The depicted photogate system is driven according to the readout sequence shown in FIG. 6. A row is selected by activating row selecting transistor **514**. The cycle begins by sampling the signal present on each column pixel in that row. Sampling is initiated by biasing transistor **526** to place the signal from each column pixel in the row onto the holding capacitor **510**.

After the current pixel value has been transferred to the capacitor **510**, the pixel in the row is reset by biasing reset transistor to a low level, to photodiode **502** to the preset voltage sink **532**.

Correlated double sampling is effected by sampling the reset value, as a reset level, onto the holding capacitor **512**. This is done by activating the reset transistor **516**.

The voltage value of the reset branch of the column circuit is given by

$$Vcol_R=\beta\{\alpha[V_{pdr}-V_{tpix}]-V_{tcolr}\}$$

Where α is the gain of the pixel source follower **508**, β is the gain of the column source follower **526**, and V_{pdr} is the voltage on the photodiode after reset, V_{tpix} is the threshold voltage of the pixel source follower and channel transistor, and V_{tcolr} is the threshold voltage of the column source follower p-channel transistor.

Using similar reasoning, the output voltage of the signal branch of the column circuit is

$$Vcol_S=\beta\{\alpha[V_{pds}-V_{tpix}]-V_{tcols}\}$$

where V_{pds} is the voltage on the photodiode with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor.

The inventors have found experimentally that the peak-to-peak variation $V_{tcolr}-V_{tcols}$ is typically between 10 and 20 millivolts. This, however, is a source of column to column fixed pattern noise. The inventors herein suggest a double delta sampling technique to eliminate this column to column noise. The present approach represents an improved version of the previously-described double delta sampling circuitry. The operation proceeds as follows. A column is first selected. After a settling time equivalent to half of the column selection period, a special double delta sampling technique is performed to remove the column fixed pattern noise. Therefore, the varying thresholds on the different transistors cause varying outputs. According to this aspect, the threshold outputs of these transistors are equalized using a capacitor to equalize the charge. The capacitor is applied with the charge before and after the voltage change. Therefore, the output of the capacitor represents the difference between before and after, and the fixed pattern noise component drops out of the equation.

This system uses a DDS switch **520** and first and second column select switches **522**, **524** to short across the respective capacitors. All three switches are turned on to short across the two sample and hold capacitors **510**. This clamp operation is shown in line 8 of FIG. 6.

Prior to the DDS operation, the reset and signal column components, Vcol_R and Vcol_S include their signal values plus a source follower voltage threshold component from the appropriate source follower. The object of the special following circuit of the present invention is to remove that source follower threshold component. The operation proceeds as follows. Prior to the beginning of some operation, the capacitors are precharged through clamp transistors to a clamp voltage V_{cl}. This is maintained by turning on clamp transistors **550** and **552** to connect the appropriate capacitors to the voltage V_{cl}. The clamp operation is shown on line 8 of FIG. 6. Immediately after the clamp is released, the DDS transistors **520**, **522** and **524** are turned on. This has the effect of shorting across the capacitors **510** and **512**. When the transistors are shorted, the voltage that is applied to the output drivers **554**, **556** includes only the voltage threshold component. The differential amplification of the voltage render the output voltage free of the voltage threshold component. Mathematically, prior to clamp being deactivated, the output signals are:

$$VR_OUT=\gamma(V_{cl}-V_{tr})$$

and

$$VS_OUT=\beta(V_{cl}-V_{ts})$$

where γ is the gain of the third stage source-follower, V_{cf} is the clamp voltage, and V_{tr} and V_{ts} are the threshold voltages of the third stage source-follower n-channel transistors, reset and signal branch respectively. Deactivation of the clamp circuit and simultaneous activation of the DDS switch causes several changes. The voltages in the two column branch sampling circuits equalize becoming:

$$V_{co}=V_{cr}=\alpha[V_{pdr}-V_{tptx}+V_{pds}-V_{tpix}]/2$$

This in turn causes a change in Vcol_S and Vcol_R to:

$$Vcol_R'=\beta\{\alpha[V_{pdr}-V_{tptx}+V_{pds}-V_{tpix}]/2-V_{tcolr}\}$$

and

$$Vcol_S'=\beta\{\alpha[V_{pdr}-V_{tptx}+V_{pds}-V_{tpix}]/2-V_{tcolr}\}$$

Consequently, the voltage outputs change to:

$$VR_OUT=\gamma(V_{cf}-Vcol_R'-Vcol_R-V_{tr})$$

and

$$VS_OUT=\gamma(V_{cf}-Vcol_S'-Vcol_S-V_{ts})$$

We note

$$Vcol_S'-Vcol_S=\beta\{\alpha[V_{pdr}-V_{pds}]/2\}$$

and

$$Vcol_R'-Vcol_R=\beta\{\alpha[V_{pdr}-V_{pds}]/2\}$$

When the outputs are differentially amplified off-chip, the common clamp voltage Vcl is removed, leaving only the difference between signal and reset. The net differential output voltage is given by:

$$VR_OUT-VS_OUT=\alpha\beta\gamma(V_{pdr}-V_{pds}=V_{const})$$

FIG. 7 shows the layout of the pixel for 128×128 array size device. This system formed a 19.2 micron pixel size using 1.2 μm n-well CMOS. The maximum clock rate is 10 MHZ, the maximum pixel rate is 2.5 MHZ and maximum integration delay is 1.6×10^9 clock periods.

A second embodiment uses similar design techniques to produce a 256×256 array size. This embodiment also uses a pixel with a photogate imaging element along with four transistors to perform the functions of readout, selection, and reset. Readout is preferably achieved using a column parallel architecture which is multiplexed one row at a time and then one column at a time through an on-chip amplifier/buffer. An important part of this embodiment, like the first embodiment, is the use of a chip common logic elements to control row and address decoders and delay counters.

This embodiment allows use in three modes of operation: Photogate mode, photodiode mode and differencing mode. The photogate mode is the standard mode for this chip. The photodiode mode alters the readout timing to be similar to that for photodiode operation. The differencing mode alters the readout timing in such a way that the value of each pixel output is the difference between the current frame and the previous frame. The chip inputs that are required are a single +5 V power supply, start command, and parallel data load commands for defining integration time and windowing parameters. The output has two differential analog channels.

The second embodiment uses the block diagram of the chip architecture shown in FIG. 8. The analog outputs of VS_OUT (signal) and VR_OUT (reset), and digital outputs of FRAME and READ. The inputs to the chip are asynchronous digital signals. The chip includes addressing circuitry allowing readout of any area of interest within the 256×256 array. The decoder includes counters that are preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 256×256.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. This counter allows forming very large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is tied to one fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 HZ frame rate can be achieved without difficulty.

The chip is idle when the RUN command is deactivated. This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

The 256×256 CMOS APS uses a system having a similar block diagram to those described previously. The pixel unit cell has a photogate (PG), a source-follower input transistor, a row selection transistor and a reset transistor. A load transistor VLN and two output branches to store the reset and signal levels are located at the bottom of each column of pixels. Each branch has a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel.

A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) and the reset value is sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate in the row is transferred to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capacitor CS. These signals are then placed on the output data bus by the column select circuitry. In the Photodiode mode this process, is reversed; first the charge under the photogate is read out and then the reset level is sampled. This non-correlated double sampling mode would be primarily used with a photodiode, i.e., non active pixel sensor, pixel.

In the differencing mode, the capacitors CS and CR are used to store the signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: Rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other sample and hold capacitor. The difference between these two signals is now the frame to frame difference.

A simplified expression for the output of the reset branch of the column circuit is given by:

$$Vcol_R = \beta\{\alpha[Vr - V_{tpix}] - V_{tcolr}\}$$

where α is the gain of the pixel source-follower, β is the gain of the column source-follower, Vr is the voltage on the floating diffusion after reset, V_{tpix} is the threshold voltage of the pixel source-follower n-channel transistor, and V_{tcolr} is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output voltage of the signal branch of the column circuit is given by:

$$Vcol_S = \beta\{\alpha[V_S V_{tpix}] - V_{tcols}\}$$

where V_S is the voltage on the floating diffusion with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak to peak variation in V_{tcolr}–V_{tcol} is typically 10–20 mV. It is desirable to remove this source of column-to-column fixed pattern noise FPN. JPL has previously developed a double delta sampling (DDS) technique to eliminate the column-to-column FPN. This approach represented an improved version of the DDS circuitry.

Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent to one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal outputs (Vcol_R and VCOL_S) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers (VR_OUT and VS_OUT) that is free of the voltage threshold component.

This chip uses a similar pixel cell to that shown in FIG. 5. FIG. 9 shows the layout of the pixel cell. PG and RESET are routed horizontally in polysilicon while the pixel output is routed vertically in metal1. Metal2 was routed within the pixel for row selection. Metal2 was also used as a light shield and covers most of the active area outside of the pixel array. The designed fill factor of the pixel is approximately 21%.

According to another feature, a logo can be formed on the acquired image by using a light blocking metal light shield. The light shield is formed to cover certain pixels in the shape of the logo to be applied. This blocks out those underlying pixels in the array, thereby forming a logo in the shape of the blocked pixels.

The output saturation level of the sensor is 800 mv when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the floating diffusion node (e.g. 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 75,000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47,000 e– per supply volt.

Dark current was measured at less than 500 pA/cm^2.

Conversion gain (μV/e–) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1%—similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer.

The quantum efficiency of the detector was measured using a CVI ¼ m monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards.

What is claimed is:

1. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and further comprising double sampling charge storage elements on said substrate.

2. A camera device as in claim 1, wherein said timing circuit includes a timer for first sampling a reset level on a first of said charge storage elements, and then for second sampling a signal level on a second of said charge storage elements.

3. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said array of photoreceptors are controlled to output an entire row of said photoreceptors substantially simultaneously; and

a plurality of double sampling charge storage elements integrated on said substrate; one for each of said columns.

4. A camera device as in claim 3, wherein said timing circuit includes a timer for first sampling all reset levels in a specific column on first charge storage elements, and then for second sampling all signal levels on second charge storage elements.

5. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a pho-

toreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said signal controlling device includes a column selector allowing selection of a desired colum for read out, and a tow selector which allows selection of a desired row fro readout.

6. A camera device as in claim 5, wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated in said substrate.

7. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

8. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout, wherein said colum selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

9. A camera device as in claim 8, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

10. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, further comprising a mode selector device, selecting a mode of operation of said chip,

wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with phologates, and second mode of operation, different that said first mode of operation, for operation with photodiodes.

11. A camera device as in claim 10, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

12. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and

further comprising a correlated double sampling circuit.

13. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same

substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

14. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

wherein said timing circuit allows changing an integration time for said array of photoreceptors.

15. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and

further comprising fixed pattern noise reduction circuits, on said substrate.

16. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, further comprising a noise reduction circuit,

wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

17. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

18. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, further comprising a mode selector device, selecting a mode of operation of said chip,

wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and second mode of operation, different that said first mode of operation, for operation with photodiodes.

19. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing present of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

20. A camera device as in claim 19, wherein said signal controlling device includes a column-parallel read. out device, which reads out a row of said photoreceptors at substantially the same time.

21. A camera device as in claim 20, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

22. A camera device as in claim 19, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop values.

23. A camera device as in claim 19, wherein said photoreceptors are photodiodes.

24. A camera device as in claim 19, wherein said photoreceptors are photogates.

25. A camera device as in claim 19, wherein said photoreceptors are either photogates or photodiodes, further comprising a mode selector device which selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

26. A camera device as in claim 25, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

27. A camera device as in claim 19, further comprising a correlated double sampling circuit integrated on the chip.

28. A camera device as in claim 19, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

29. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

30. A camera device as in claim 29, wherein said readout amplifier is preferably within and/or associated with one element of the array.

31. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

32. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

33. A camera device as in claim 32, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

34. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors in a first mode or in a second mode, depending on a type of photoreceptor being used.

35. A camera device as in claim 34, wherein said photoreceptor is one of a photodiode or a photogate, and said array is controlled into said first mode for said photogate and in said second mode for said photodiode.

36. A camera device as in claim 35, further comprising a correlated double sampling circuit.

37. A camera device as in claim 35, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

38. A camera device as in claim 35, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

39. A camera device as in claim 38, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

40. A camera device as in claim 34, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

41. A camera device as in claim 40, wherein said readout amplifier is preferably within and/or associated with one element of the array.

42. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors in a first mode or in a second mode, depending on a type of photoreceptor being used, further comprising a noise reduction circuit.

43. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

said control portion including common logic elements to control row and address decoders and delay counters.

44. A camera device as in claim 43, wherein said signal controlling device includes a column-parallel read out device, which reads out a column of said photoreceptors at substantially the same time.

45. A camera device as in claim 44, further comprising a noise reduction circuits, on chip.

46. A camera device as in claim 45, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

47. A camera device as in claim 45, wherein said noise reduction circuit is a fixed pattern noise reduction circuit.

48. A camera device as in claim 45, wherein said noise reduction circuit is a column to column fixed pattern noise reduction circuit.

49. A camera device as in claim 43, wherein said signal controlling device includes a column selector allowing selection of a desired row for read out, and a row selector which allows selection of a desired row for readout.

50. A camera device as in claim 49 wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

51. A camera device as in claim 49, wherein said column selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

52. A camera device as in claim 51, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

53. A camera device as in claim 43, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

54. A camera device as in claim 53, wherein said readout amplifier is preferably within and/or associated with one element of the array.

55. A camera device as in claim 53, wherein said photoreceptors are photodiodes.

56. A camera device as in claim 53 wherein said photoreceptors are photogates.

57. A camera device as in claim 43, further comprising a correlated double sampling circuit.

58. A camera device as in claim 43, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

59. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

said control portion including common logic elements to control row and address decoders and delay counters, further comprising a mode selector device, selecting a mode of operation of said chip.

60. A camera device as in claim 59, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

61. A camera device as in claim 60, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

62. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

63. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors arranged in row and columns;

a charge storage element, associated with each said columns;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously, further comprising a mode selector device, selecting a mode of operation of said chip.

64. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said colum;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously,

wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

65. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

66. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors, and a signal controlling device, controlling said photoreceptors and a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

determining a first mode of operation for said photoreceptors being photogates, and a second mode of operation for said photoreceptors being photodiodes;

using said on-chip timing and control circuit to control sequences for accessing rows in a specified order depending on said mode of operation, using a first sequence for said first mode of operation for photogates, and a second mode of operation for said second mode for photodiodes, a timing for said first mode being different than a timing for said second mode.

* * * * *

EXHIBIT D

US006606122B1

(12) **United States Patent**
Shaw et al.

(10) **Patent No.: US 6,606,122 B1**
(45) **Date of Patent: Aug. 12, 2003**

(54) **SINGLE CHIP CAMERA ACTIVE PIXEL SENSOR**

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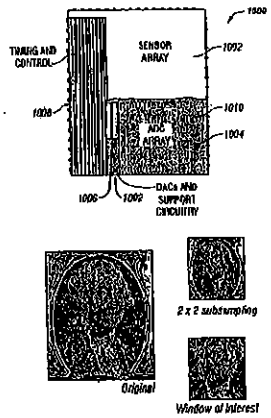
Primary Examiner—Wendy R. Garber
Assistant Examiner—John M. Villecco
(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(57) **ABSTRACT**

A totally digital single chip camera includes communications to operate most of its structure in serial communication mode. The digital single chip camera include a D/A converter for converting an input digital word into an analog reference signal. The chip includes all of the necessary circuitry for operating the chip using a single pin.

6 Claims, 13 Drawing Sheets



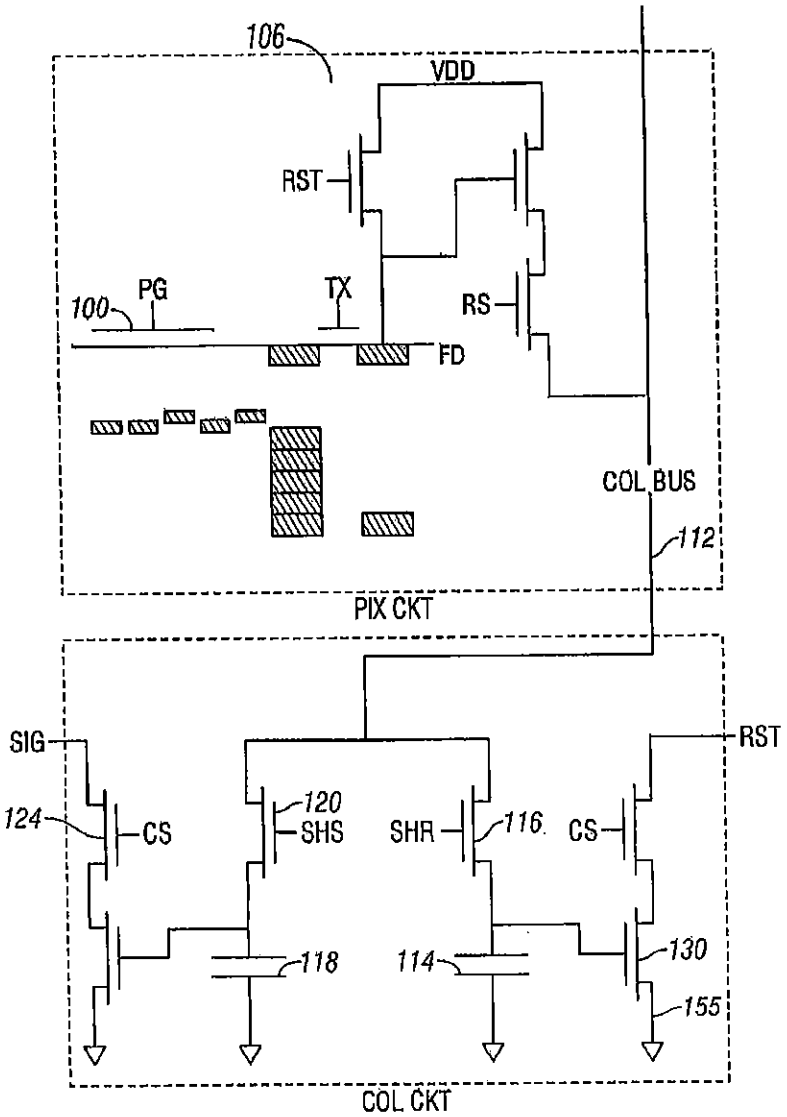

106
VDD
RST
100
PG
TX
RS
FD
COL BUS
112
PIX CKT
SIG
124
CS
120
SHS
SHR
116
CS
RST
118
114
130
155
COL CKT

FIG. 1

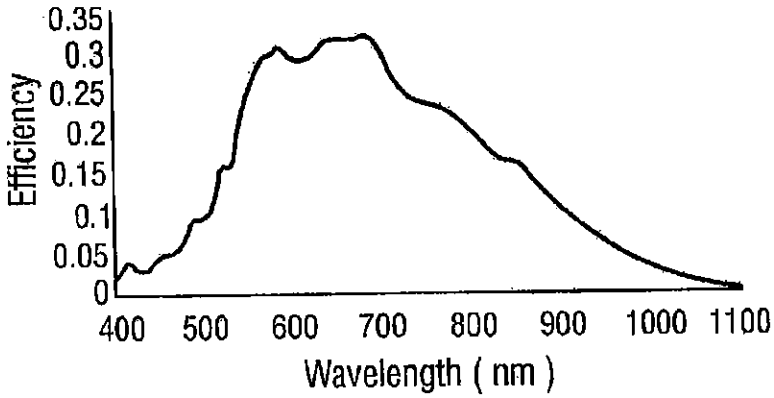
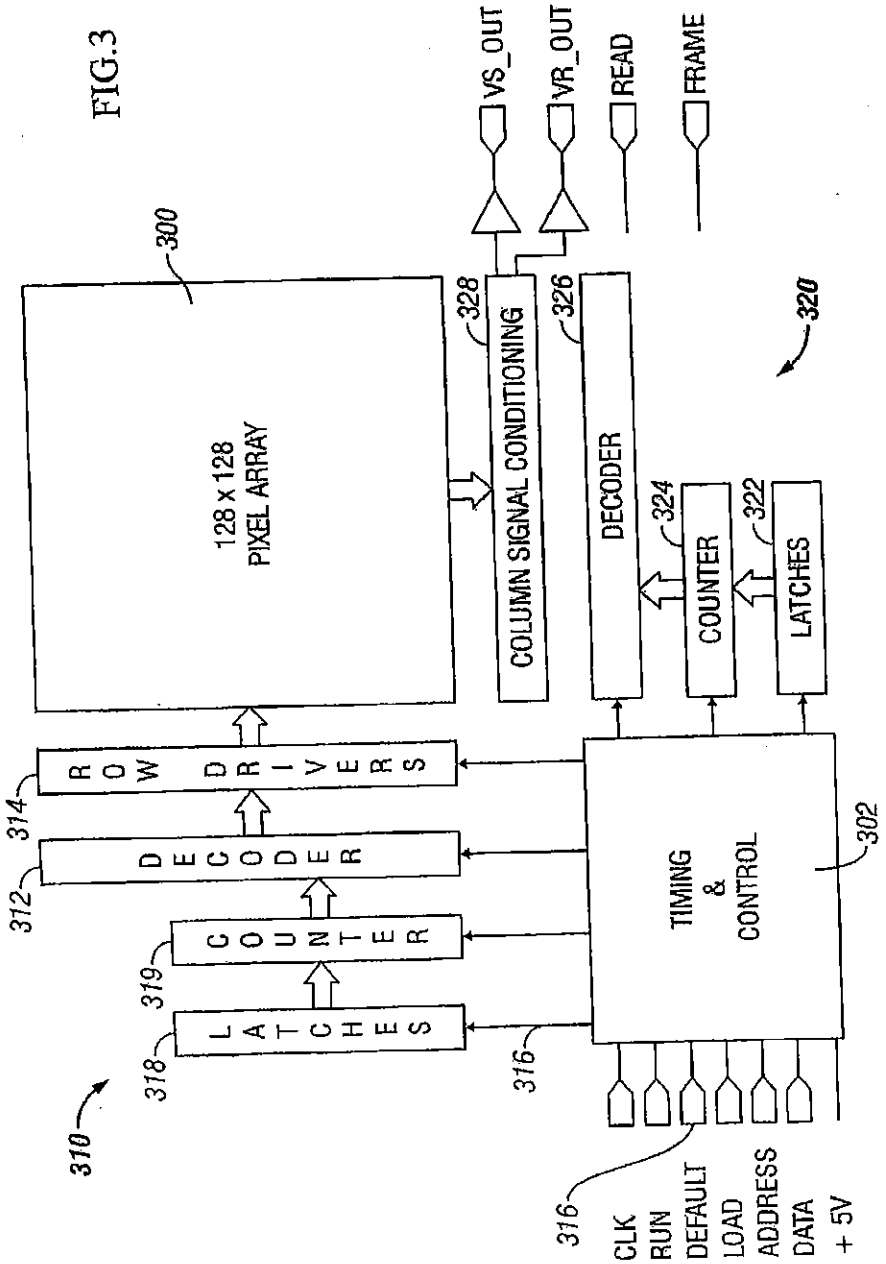

Efficiency
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
400
500
600
700
800
900
1000
1100
Wavelength (nm)

FIG. 2

FIG.3


VS_OUT
VR_OUT
READ
FRAME
300
128 x 128 PIXEL ARRAY
328
COLUMN SIGNAL CONDITIONING
326
DECODER
320
324
COUNTER
322
LATCHES
ROW DRIVERS
314
DECODER
312
COUNTER
319
LATCHES
318
310
316
TIMING & CONTROL
302
316
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
+ 5V

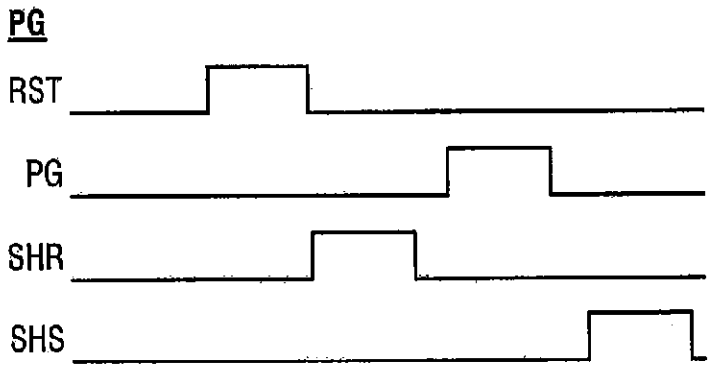


FIG. 4A

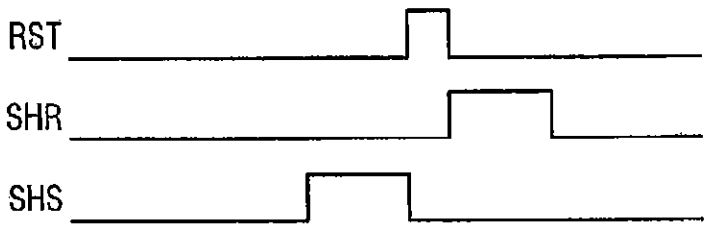


FIG. 4B

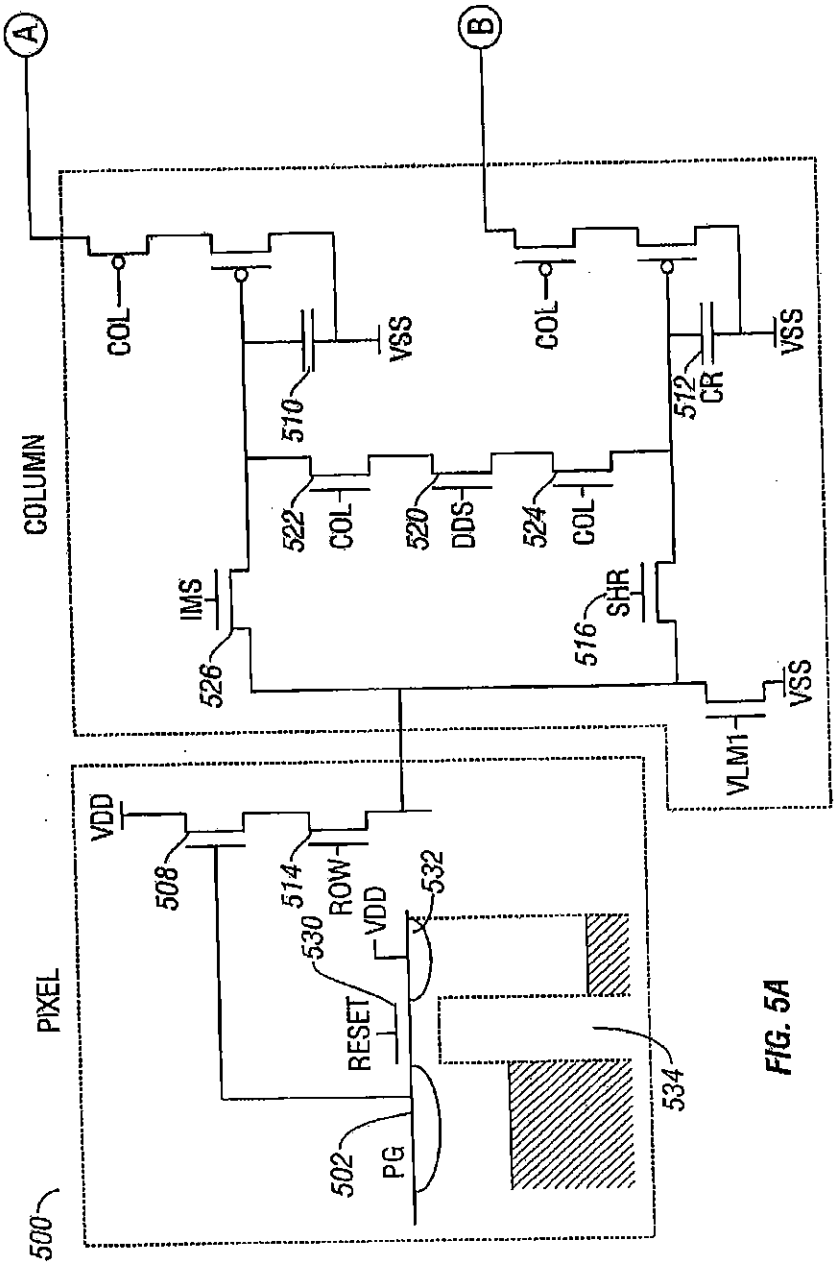

A
B
COLUMN
COL
VSS
510
512
CR
522
520
DDS
524
IMS
526
SHR
516
VLM1
PIXEL
VDD
508
514
ROW
530
532
RESET
502
PG
534
500

FIG. 5A

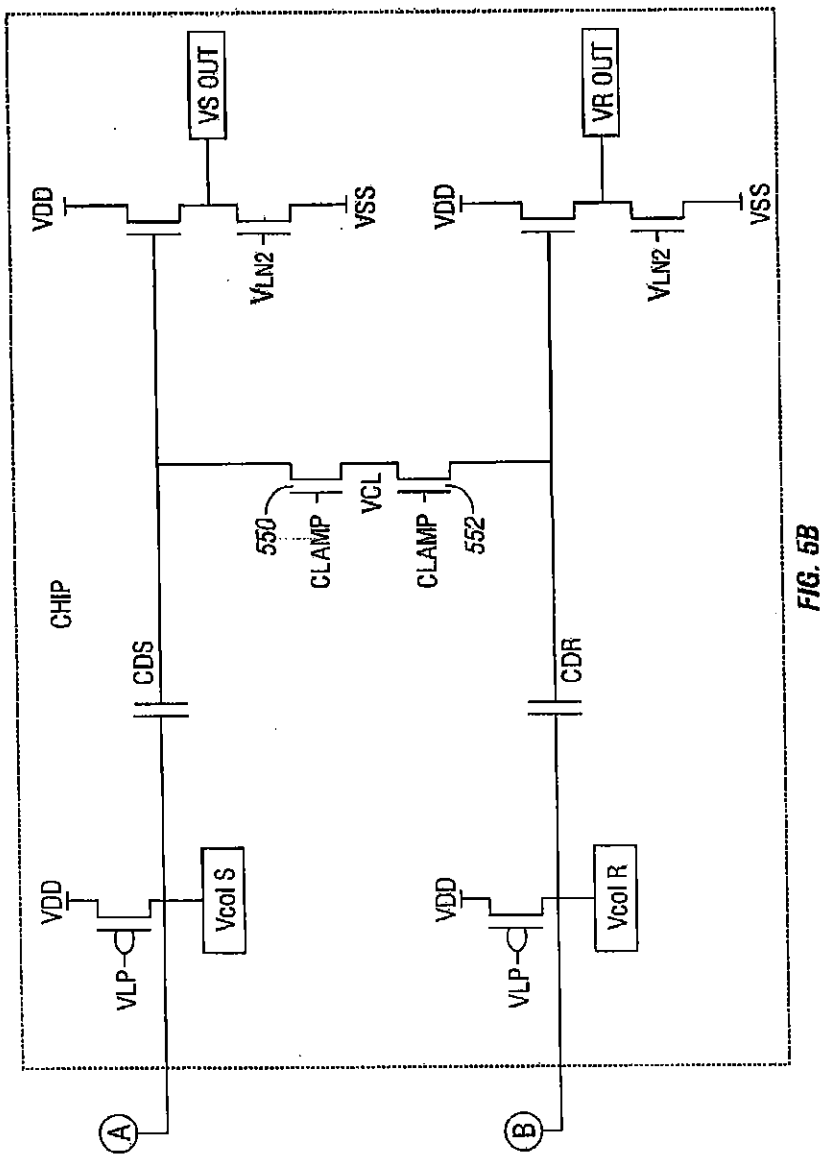

VS OUT
VR OUT
VDD
VSS
VLN2
VCL
CLAMP
550
552
CHIP
CDS
CDR
VLP
Vcol S
Vcol R
A
B

FIG. 5B

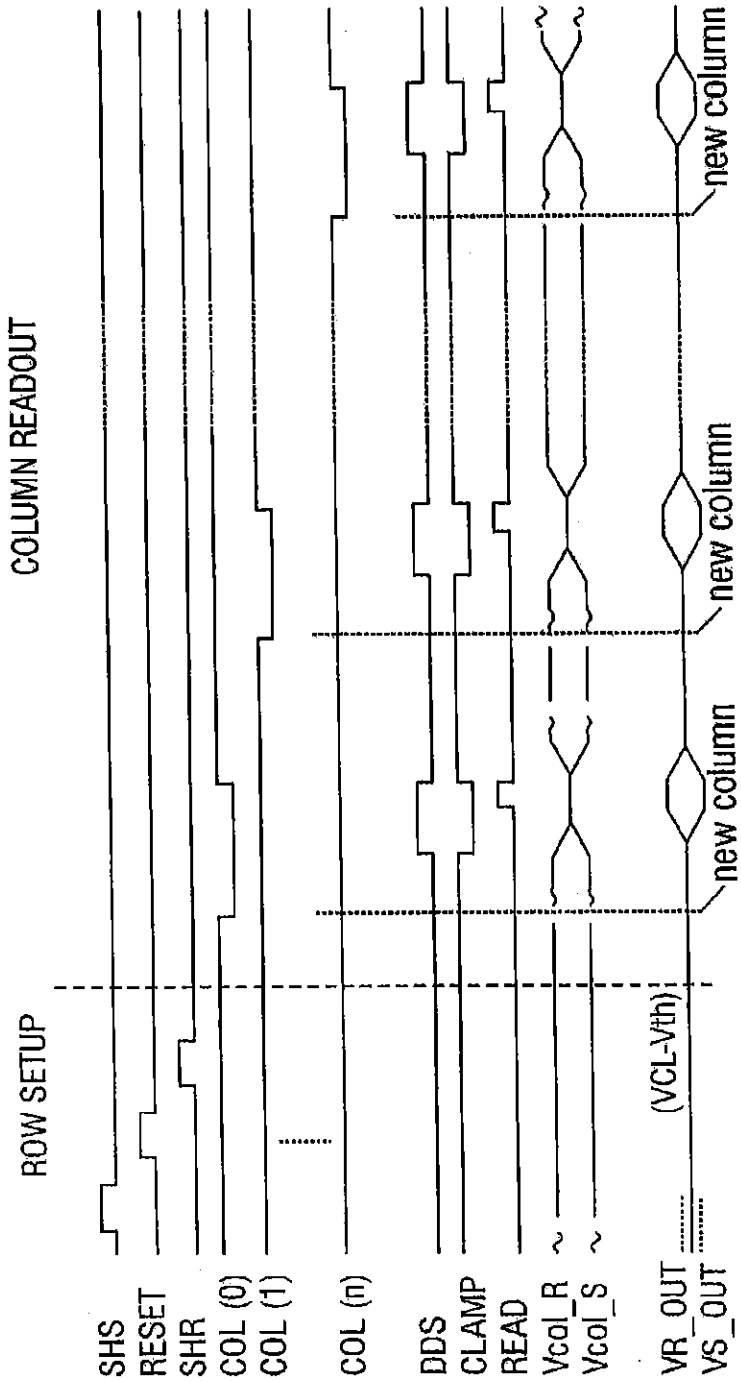

COLUMN READOUT
ROW SETUP
SHS
RESET
SHR
COL (0)
COL (1)
COL (n)
DDS
CLAMP
READ
Vcol_R
Vcol_S
VR_OUT
VS_OUT
(VCL-Vth)
new column
new column
new column

FIG. 6

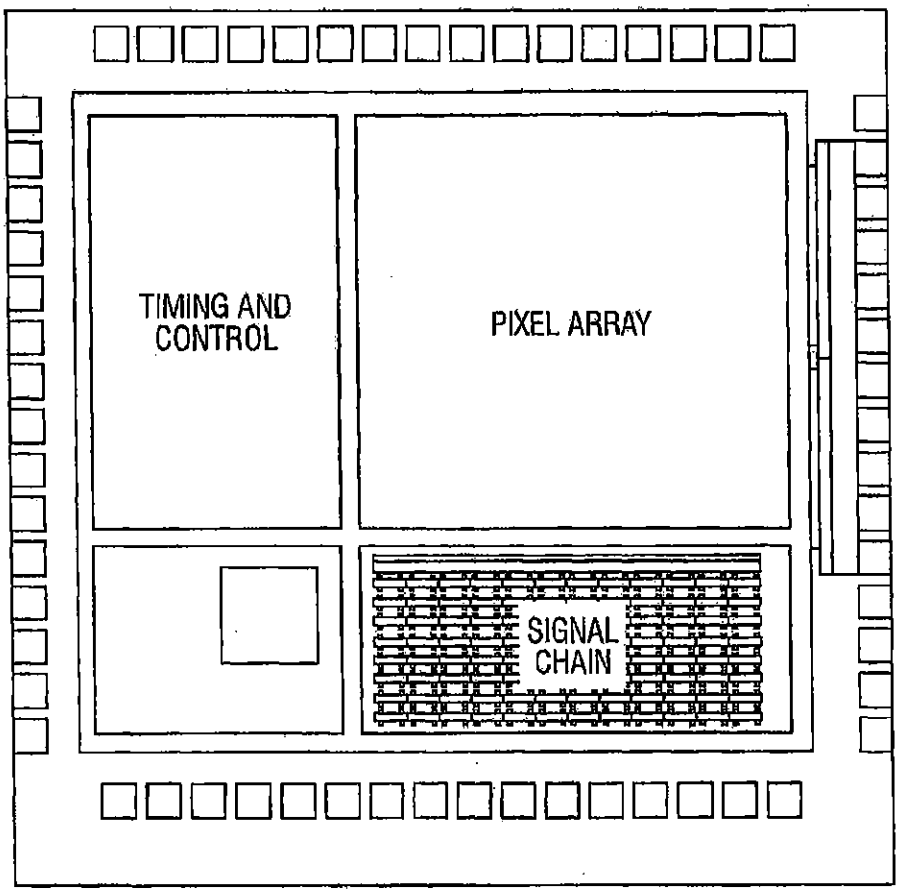


FIG. 7

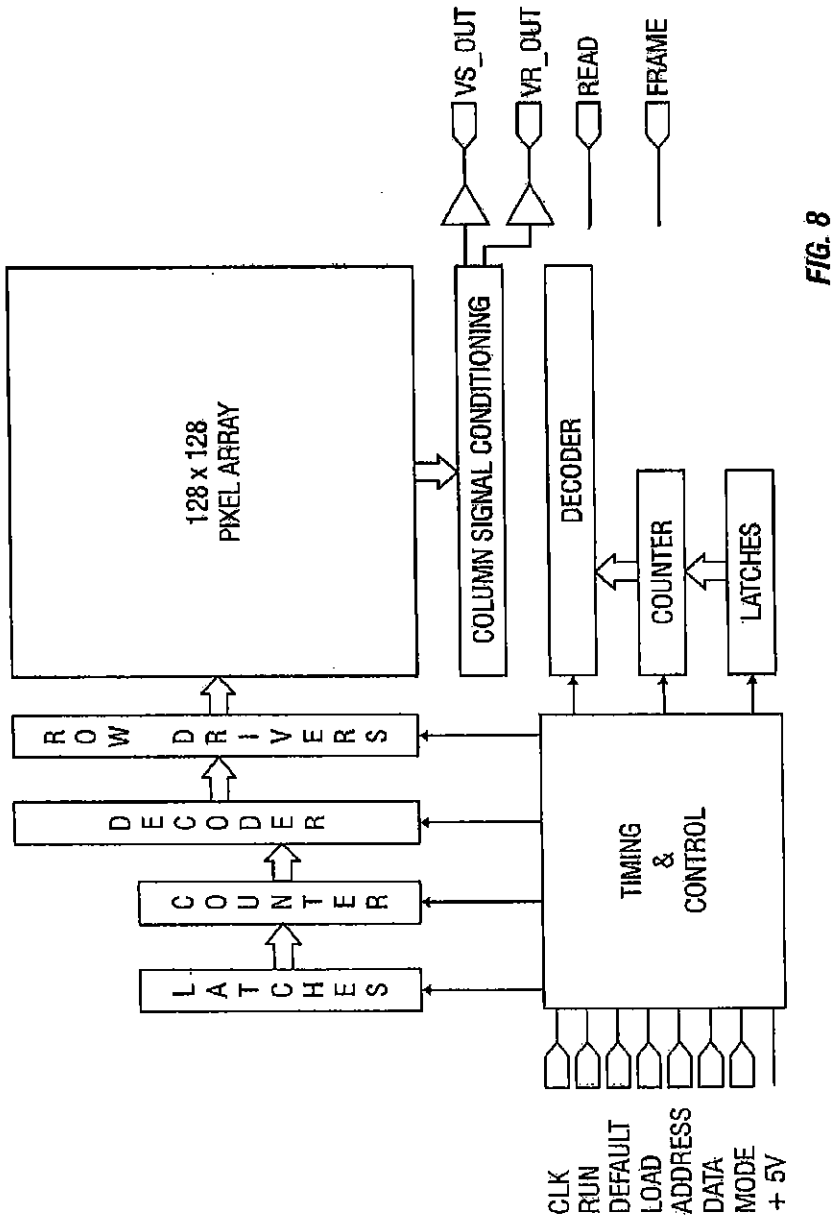
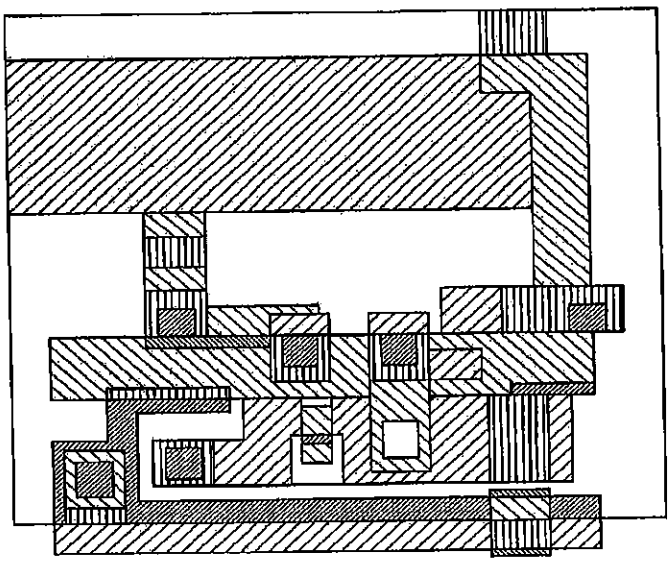
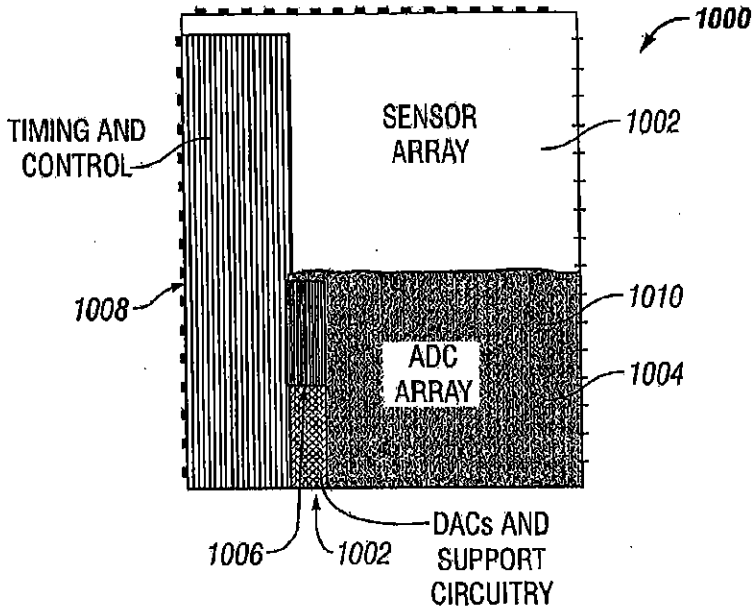

VS_OUT
VR_OUT
READ
FRAME
128 x 128
PIXEL ARRAY
COLUMN SIGNAL CONDITIONING
DECODER
COUNTER
LATCHES
ROW DRIVERS
DECODER
COUNTER
LATCHES
TIMING
&
CONTROL
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
MODE
+ 5V

FIG. 8



Array Size	256 x 256
Pixel Size	20.4 μm
Technology	1.2μm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16×10^9 clock periods or 1600 secs at 10 MHz

FIG. 9


1000
TIMING AND CONTROL
SENSOR ARRAY
1002
1008
1010
ADC ARRAY
1004
1006
1002
DACs AND SUPPORT CIRCUITRY

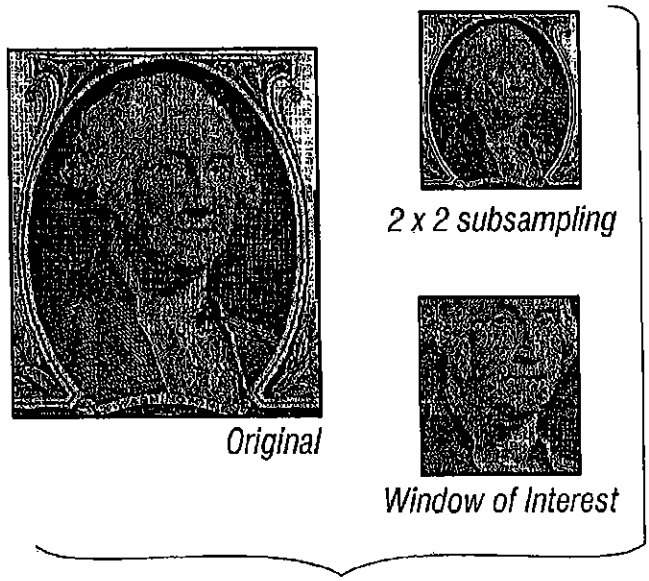

2 x 2 subsampling
Original
Window of Interest

FIG. 10

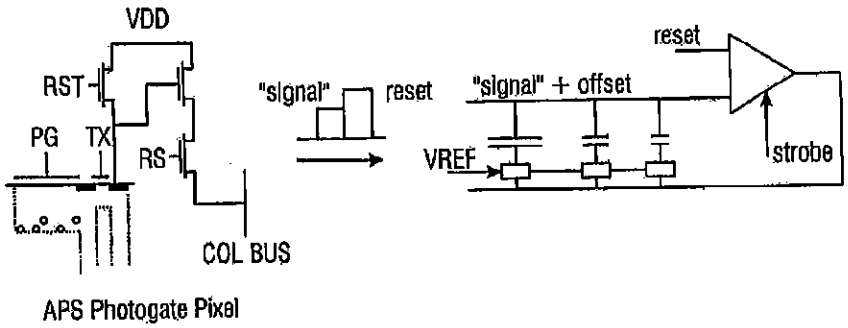


FIG. 11A

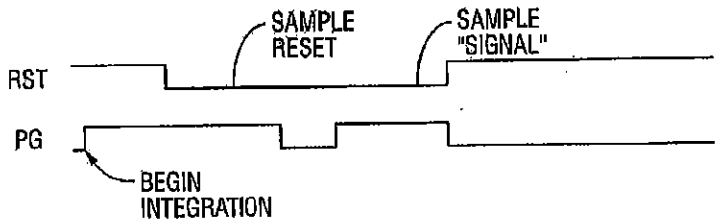


FIG. 11B

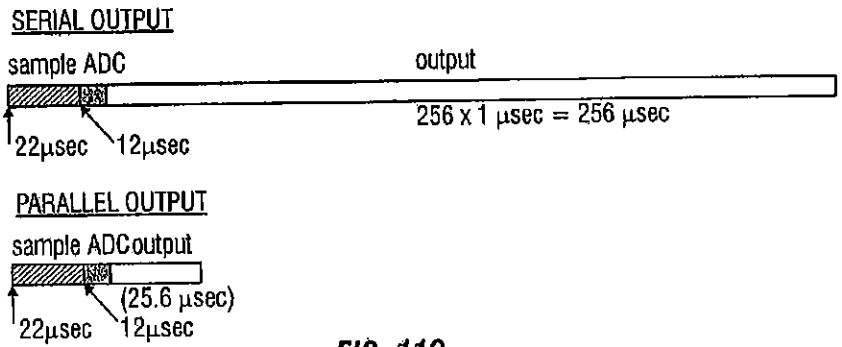


FIG. 11C

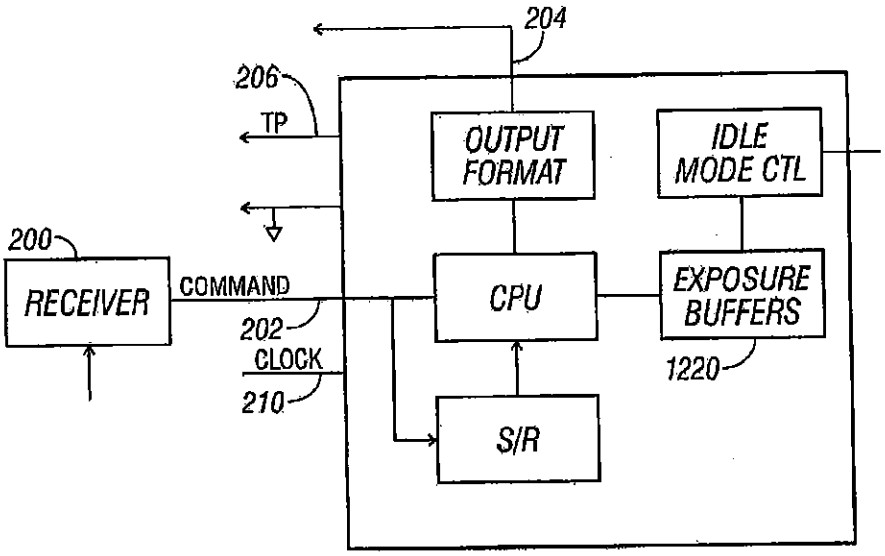


FIG. 12

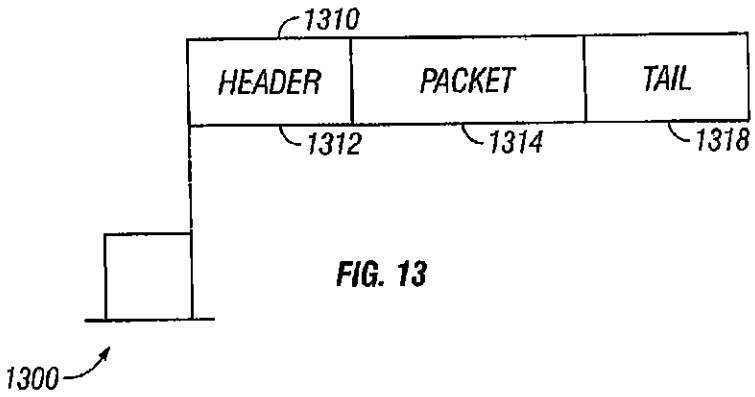


FIG. 13

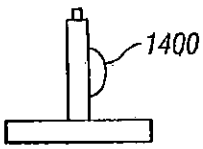


FIG. 14

SINGLE CHIP CAMERA ACTIVE PIXEL SENSOR

This claims priority from Provisional Application No. 60/060,236 having a filing date of Sep. 29, 1997.

Origin

The invention described herein was made in performance of work under NASA contract and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the contractor has elected to retain title.

FIELD OF THE INVENTION

The present invention relates to a single chip imaging sensor.

BACKGROUND AND SUMMARY

Imaging technology is the science of converting an image to a signal indicative thereof. Imaging systems have broad applications in many fields, including commercial, consumer, industrial, medical, defense and scientific markets.

The original image sensors included an array of photosensitive elements in series with switching elements. Each photosensitive element received an image of a portion of the scene being imaged. That portion is called a picture element or pixel. The image obtaining elements produce an electrical signal indicative of the image plus a noise component. Various techniques have been used in the art to minimize the noise, to thereby produce an output signal that closely follows the image.

Size minimization is also important. The development of the solid state charge coupled device ("CCD") in the early 1970's led to more compact image systems. CCDs use a process of repeated lateral transfer of charge in an MOS electrode-based analog shift register. Photo-generated signal electrons are read after they are shifted into appropriate positions. However, the shifting process requires high fidelity and low loss. A specialized semiconductor fabrication process was used to obtain these characteristics.

CCDs are mostly capacitive devices and hence dissipate very little power. The major power dissipation in a CCD system is from the support electronics. One reason for this problem is because of the realities of forming a CCD system.

The specialized semiconductor fabrication process alluded to above is not generally CMOS compatible. Hence, the support circuitry for such a CCD has been formed using control electronics which were not generally CMOS compatible. The control electronics have dissipated an inordinate percentage of the power in such imaging devices. For example, CCD-based camcorder imaging systems typically operate for an hour on an 1800 mA-hr 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Approximately 8 watts of this is dissipated in the imaging system. The rest is used by the tape recording system, display, and autofocus servos.

Space-based imaging systems often have similar problems. The space based systems operate at lower pixel rates, but with a lower degree of integration, and typically dissipate 20 watts or more.

The CCD has many characteristics which cause it to act like a chip-sized MOS capacitor. The large capacitance of the MOS device, for example, requires large clock swings, ΔV, of the order of 5–15 V to achieve high charge transfer efficiency. The clock drive electronics dissipation is proportional to CAV^2f, and hence becomes large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with their attendant inefficiencies in conversion.

Signal chain electronics that perform correlated double sampling ("CDS") for noise reduction and amplification, and especially analog to digital converters (ADC), also dissipate significant power.

The inventors also noted other inefficiencies in imaging systems. These inefficiencies included fill factor inefficiencies, fixed pattern noise, clock pick up, temporal noise and large pixel size.

Active pixel sensors, such as described in U.S. Pat. No. 5,471,515, the disclosure of which is incorporated by reference herein, use special techniques to integrate both the photodetector and the readout amplifier into the pixel area or adjacent the pixel area. This allows the signal indicative of the pixel to be read out directly. These techniques have enabled use of a logic family whose fabrication processes are compatible with CMOS. This has enabled the controlling circuitry to be made from CMOS or some other low power-dissipating logic family.

The inventors of the present invention have recognized techniques and special efficiencies that are obtained by specialized support electronics that are integrated onto the same substrate as the photosensitive element. Aspects of the present invention include integration, timing, control electronics, signal chain electronics, A/D conversion, and other important control systems integrated on the same substrate as the photosensitive element.

The disclosure also describes various improvements in such a system.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a basic block diagram of a CMOS active pixel circuit;

FIG. 2 shows a graph of typical APS quantum efficiency;

FIG. 3 shows the block diagram of the overall chip including drivers and controlling structures;

FIGS. 4A and 4B show the timing diagrams for photogate operation and photodiode operation, respectively;

FIG. 5 shows a schematic of the active pixel sensor unit cell and readout circuitry;

FIG. 6 shows a timing diagram for setup and readout;

FIG. 7 shows a drawing of an actual layout of the pixel and control circuitry;

FIG. 8 shows a block diagram of a CMOS APS chip; and

FIG. 9 shows an exemplary pixel layout.

FIG. 10 shows the basic array of the improved noise reduction circuit embodiment.

FIGS. 11A and 11B show the noise reduction circuit embodiment.

FIG. 11C shows serial and parallel output from the A/D converter.

FIG. 12 shows a functional block diagram of the improved embodiment.

FIG. 13 shows a timing diagram of the serial communication.

FIG. 14 shows an alternate mounting configuration for the chip with the devicemounted on its side.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An active pixel sensor is herewith described with reference to FIGS. 1–4.

A block diagram of a CMOS active pixel circuit is shown in FIG. 1. The device has a pixel circuit **150**, and a column circuit **155**.

Incident photons pass through the photogate ("PG") **100** in the pixel circuit **150** and generate electrons which are integrated and stored under PG **100**. A number of the pixel circuits are arranged in each row of the circuit. One of the rows is selected for readout by enabling the row selection transistor **102** ("RS").

In the preferred embodiment, the floating diffusion output node **104** ("FD") is first reset by pulsing reset transistor ("RST") **106**. The resultant voltage on FD **104** is read out from the pixel circuitry onto the column bus **112** using the source follower **110** within the pixel. The voltage on the column bus **112** is sampled onto a first holding capacitor **114** by pulsing transistor SHR **116**. This initial charge is used as the baseline.

The signal charge is then transferred to FD **104** by pulsing PG **100** low. The voltage on FD **104** drops in proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus **112** is sampled onto a second capacitor **118** by pulsing SHR **120**. The difference between the voltages on first capacitor **114** and second capacitor **118** is therefore indicative of the number of photoelectrons that were allowed to enter the floating diffusion.

The capacitors **114**, **118** are preferably 1–4 pf capacitors.

All pixels on a selected row are processed simultaneously and sampled onto capacitor at the bottom of their respective columns. The column-parallel sampling process typically takes 1–10 μsec, and preferably occurs during the so-called horizontal blanking interval of a video image.

Each column is successively selected for read-out by turning on column selection p-channel transistors ("CS") **130**. The p-channel source-followers **122**, **124** in the column respectively drive the signal (SIG) and horizontal reset (RST) bus lines. These lines are loaded by p-channel load transistors which can be sent directly to a pad for off-chip drive, or can be buffered.

Noise in the sensor is preferably suppressed by the above-described correlated double sampling ("CDS") between the pixel output just after reset, before and after signal charge transfer to FD as described above. The CDS suppresses kTC noise from pixel reset, suppresses 1/f noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage.

The inventors found, however, that kTC noise may be reintroduced by sampling the signal onto the capacitors **114**, **118** at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 140–170 μV/e–, corresponding to noise of the order of 13–25 electrons rms. This is similar to noise obtained in most commercial CCDs, through scientific CCDs have been reported with read noise in the 3–5 electrons rms.

Typical biasing for each column's source-follower is 10 μA. This permits charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by cutting the voltage on each load transistor.

The sampling average power dissipation P_s corresponds to:

$$P_s = n\,I\,V\,d$$

where n is number of columns, I is the load transistor bias, V is the supply voltage, and d is the duty cycle. Using n=512, I=μA, V=5V and d=10%, a value for Ps of 2.5 mW is obtained.

A load current of 1 mA or more is needed to drive the horizontal bus lines at the video scan rate. The power dissipated is typically 5 mW.

Quantum efficiency measured in this CMOS APS array is similar to that for interline CCDs. A typical response curve is shown in FIG. 2. The inventors noticed from this that the quantum efficiency reflects significant responsivity in the "dead" part of the pixel; the part containing the readout circuitry rather than the photogate collector. The responsiveness was measured by intra-pixel laser spot scanning.

The inventors postulate the following reason. The transistor gate and channel absorb photons with short absorption lengths (i.e. blue/green). However, longer wavelength photons penetrate through these regions. The subsequently-generated carriers diffuse laterally and are subsequently collected by the photogate.

Thus, despite a fill factor of 25%–30%, the CMOS APS achieves quantum efficiencies that peak between 30%–35% in the red and near infrared. Microlenses are preferably added to refract photoelectrons from the dead part to a live part and hence improve quantum efficiency.

An important feature of the system described herein is the integration of on-chip timing and control circuits within the same substrate that houses the pixel array and the signal chain electronics. A block diagram of the chip architecture is shown in FIG. 3.

The analog outputs VS_out (signal) and VR_out (reset) are as described above. The digital outputs include FRAME and READ. Most of the inputs to the chip are asynchronous digital signals, as described herein.

The chip includes a pixel array **300**, which is driven by on-chip electronics. Timing and control circuit **302** drives row electronics **310**, and column electronics **320**.

The control circuits can command read-out of any area of interest within the array. Row decoder **312** controls row drivers **314** which can select a certain row for readout. A specific row is selected by entry of a row value **316** which is output from timing and control **302**. Row value **316** is stored in latch **318** which drives counter **319**. Counter **319** can allow selection of subsequent rows that follow the current row. Similarly, columns can be selected and accessed by latches **322**, counter **324**, decoder **326** and column signal conditioning **328**.

Each of the decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus **330**. Therefore, as described above, selection of a row commands pixels in that row to be transferred to the appropriate row decoding elements, e.g., capacitors. Preferably there is one capacitor associated with each column. This provides for the sequential readout of rows using the column. The capacitors are preferably included within the column signal conditioner **328**. Column decoders **326** also allow selection of only a certain column to be read. There are two parts of each column selection: where to start reading, and where to stop reading. Preferably the operation is carried out using counters and registers. A binary up-counter within the decoder **326** is preset to the start value. A preset number of rows is used by loading the 2's compliment. The up counter then counts up until an overflow.

An alternate loading command is provided using the DEFAULT LOAD input line **332**. Activation of this line forces all counters to a readout window of 128×128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus **330**. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. The counter can hence provide vary large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. The integration time is therefore equal to the delay time and the readout time for a 2.5 MHZ clock. The maximum delay time is 2^{32}/2.5 MHZ, or around 28 minutes. These values therefore easily allow obtaining a 30 Hz frame.

The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in FIGS. 4A and 4B. FIG. 4A shows an operation to operate in the photogate mode and FIG. 4B shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is V1, the output is V1 plus the threshold.

The column signal conditioning circuitry contains a double-delta sampling fixed pattern noise ("FPN") suppression stage that reduces FPN to below 0.2% sat with a random distribution. Since the APS is formed of a logic family that is compatible with CMOS, e.g., NMOS, the circuitry can be formed of CMOS. This allows power dissipation in the timing and control digital circuitry to be minimized and to scale with clock rate.

An active pixel sensor includes both a photodetector and the readout amplifier integrated within the same substrate as the light collecting device, e.g., the photodiode. The readout amplifier is preferably within and/or associated with a pixel.

A first embodiment of the present invention is a 128×128 CMOS photodiode type active pixel sensor that includes on chip timing, control and signal train electronics. A more detailed drawing of the chip is shown in FIG. **5**. Asynchronous digital signals are converted by this chip to VS and VR analog outputs which are used to run the chip.

Pixel portion **500** includes a photodiode **502** which stores incident photons under photogate **504**. The photons are integrated as electrons within the photogate well. The output is buffered by follower **508**.

The rows are arranged into an array. A particular row is selected by the row transistor **514**. This allows the information from within the selected pixel **500** to be passed to the column decoder circuitry. Reset transistor **530** is connected to a sink **532**. Reset transistor is biased to a low potential level to allow all charge to bleed to sink **532**, and hence hold the stored charge in reset. The system is removed from reset by biasing the gate to a level as shown. This level is less than a highest possible potential to thereby allow charge which accumulates above that level to pass to sink **532**. Hence, the charge cannot overflow in an undesired way. This suppresses the blooming effect.

The depicted photogate system is driven according to the readout sequence shown in FIG. 6. A row is selected by activating row selecting transistor **514**. The cycle begins by sampling the signal present on each column pixel in that row. Sampling is initiated by biasing transistor **526** to place the signal from each column pixel in the row onto the holding capacitor **510**.

After the current pixel value has been transferred to the capacitor **510**, the pixel in the row is reset by biasing reset transistor to a low level, to photodiode **502** to the preset voltage sink **532**.

Correlated double sampling is effected by sampling the reset value, as a reset level, onto the holding capacitor **512**. This is done by activating the reset transistor **516**.

The voltage value of the reset branch of the column circuit is given by

$$Vcol_R=\beta\{\alpha[V_{pdr}-V_{tpix}]-V_{tcolr}\}$$

Where α is the gain of the pixel source follower **508**, β is the gain of the column source follower **526**, and V_{pdr} is the voltage on the photodiode after reset, V_{tpix} is the threshold voltage of the pixel source follower and channel transistor, and V_{tcolr} is the threshold voltage of the column source follower p-channel transistor.

Using similar reasoning, the output voltage of the signal branch of the column circuit is

$$Vcol_S=\beta\{\alpha[V_{pds}-V_{tpix}]-V_{tcols}\}$$

where V_{pds} is the voltage on the photodiode with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor.

The inventors have found experimentally that the peak-to-peak variation $V_{tcolr}-V_{tcols}$ is typically between 10 and 20 millivolts. This, however, is a source of column to column fixed pattern noise. The inventors herein suggest a double delta sampling technique to eliminate this column to column noise. The present approach represents an improved version of the previously-described double delta sampling circuitry. The operation proceeds as follows. A column is first selected. After a settling time equivalent to half of the column selection period, a special double delta sampling technique is performed to remove the column fixed pattern noise. Therefore, the varying thresholds on the different transistors cause varying outputs. According to this aspect, the threshold outputs of these transistors are equalized using a capacitor to equalize the charge. The capacitor is applied with the charge before and after the voltage change. Therefore, the output of the capacitor represents the difference between before and after, and the fixed pattern noise component drops out of the equation.

This system uses a DDS switch **520** and first and second column select switches **522**, **524** to short across the respective capacitors. All three switches are turned on to short across the two sample and hold capacitors **510**. This clamp operation is shown in line **8** of FIG. **6**.

Prior to the DDS operation, the reset and signal column components, Vcol_R and Vcol_S include their signal values plus a source follower voltage threshold component from the appropriate source follower. The object of the special following circuit of the present invention is to remove that source follower threshold component. The operation proceeds as follows. Prior to the beginning of some operation, the capacitors are precharged through clamp transistors to a clamp voltage V_{cl}. This is maintained by turning on clamp transistors **550** and **552** to connect the appropriate capacitors to the voltage V_{cl}. The clamp operation is shown on line **8** of FIG. **6**. Immediately after the clamp is released, the DDS transistors **520**, **522** and **524** are

turned on. This has the effect of shorting across the capacitors 510 and 512. When the transistors are shorted, the voltage that is applied to the output drivers 554, 556 includes only the voltage threshold component. The differential amplification of the voltage render the output voltage free of the voltage threshold component. Mathematically, prior to clamp being deactivated, the output signals are:

$$VR_OUT=\gamma(V_{cl}-V_{tr})$$

$$\text{and } VS_OUT=\gamma(V_{cl}-V_{ts})$$

where γ is the gain of the third stage source-follower, V_{cl} is the clamp voltage, and V_{tr} and V_{ts} are the threshold voltages of the third stage source-follower n-channel transistors, reset and signal branch respectively. Deactivation of the clamp circuit and simultaneous activation of the DDS switch causes several changes. The voltages in the two column branch sampling circuits equalize becoming:

$$V_{cs}=V_{cr}=\alpha[V_{pdr}-V_{tpfr}+V_{pds}-V_{tpfs}]/2$$

This in turn causes a change in Vcol_S and Vcol_R to:

$$Vcol_R'=\beta\{\alpha[V_{pdr}-V_{tpfr}+V_{pds}-V_{tpfs}]/2-V_{rcolr}\}$$

$$\text{and } Vcol_S'=\beta\{\alpha[V_{pdr}-V_{tpfr}+V_{pds}-V_{tpfs}]/2-V_{rcols}\}$$

Consequently, the voltage outputs change to:

$$VR_OUT=\gamma(V_{cl}-V_{col}_R'-Vcol_R-V_{tr})$$

$$\text{and } VS_OUT=\gamma(V_{cl}-Vcol_S'-Vcol_S-V_{ts})$$

We note

$$Vcol_S'-Vcol_S=\beta\{\alpha[V_{pds}-V_{pdr}]/2\}$$

$$\text{and } Vcol_R'-Vcol_R=\beta\{\alpha[V_{pds}-V_{pdr}]/2\}$$

When the outputs are differentially amplified off-chip, the common clamp voltage Vcl is removed, leaving only the difference between signal and reset. The net differential output voltage is given by:

$$VR_OUT-VS_OUT=\alpha\gamma(V_{pdr}-V_{pds}-V_{const})$$

FIG. 7 shows the layout of the pixel for 128×128 array size device. This system formed a 19.2 micron pixel size using 1.2 μm n-well CMOS. The maximum clock rate is 10 MHZ, the maximum pixel rate is 2.5 MHZ and maximum integration delay is 1.6×10^9 clock periods.

A second embodiment uses similar design techniques to produce a 256×256 array size. This embodiment also uses a pixel with a photogate imaging element along with four transistors to perform the functions of readout, selection, and reset. Readout is preferably achieved using a column parallel architecture which is multiplexed one row at a time and then one column at a time through an on-chip amplifier/buffer. An important part of this embodiment, like the first embodiment, is the use of a chip common logic elements to control row and address decoders and delay counters.

This embodiment allows use in three modes of operation: Photogate mode, photodiode mode and differencing mode. The photogate mode is the standard mode for this chip. The photodiode mode alters the readout timing to be similar to that for photodiode operation. The differencing mode alters the readout timing in such a way that the value of each pixel output is the difference between the current frame and the previous frame. The chip inputs that are required are a single +5 V power supply, start command, and parallel data load commands for defining integration time and windowing parameters. The output has two differential analog channels.

The second embodiment uses the block diagram of the chip architecture shown in FIG. 8. The analog outputs of VS_OUT (signal) and VR_OUT (reset), and digital outputs of FRAME and READ. The inputs to the chip are asynchronous digital signals. The chip includes addressing circuitry allowing readout of any area of interest within the 256×256 array. The decoder includes counters that are preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 256×256.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. This counter allows forming very large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is tied to one fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 HZ frame rate can be achieved without difficulty.

The chip is idle when the RUN command is deactivated. This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

The 256×256 CMOS APS uses a system having a similar block diagram to those described previously. The pixel unit cell has a photogate (PG), a source-follower input transistor, a row selection transistor and a reset transistor. A load transistor VLN and two output branches to store the reset and signal levels are located at the bottom of each column of pixels. Each branch has a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel.

A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) and the reset value is sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate in the row is transferred to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capacitor CS. These signals are then placed on the output data bus by the column select circuitry. In the Photodiode mode this process, is reversed; first the charge under the photogate is read out and then the reset level is sampled. This non-correlated double sampling mode would be primarily used with a photodiode, i.e., non active pixel sensor, pixel.

In the differenciug mode, the capacitors CS and CR are used to store the signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: Rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous

pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other sample and hold capacitor. The difference between these two signals is now the frame to frame difference.

A simplified expression for the output of the reset branch of the column circuit is given by:

$$Vcol_R = \beta\{\alpha[Vr - V_{tpix}] - V_{tcolr}\}$$

where α is the gain of the pixel source-follower, β is the gain of the column source-follower, Vr is the voltage on the floating diffusion after reset, V_{tpix} is the threshold voltage of the pixel source-follower n-channel transistor, and V_{tcolr} is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output voltage of the signal branch of the column circuit is given by:

$$Vcol_S = \beta\{\alpha[V_s - V_{tpix}] - V_{tcols}\}$$

where V_s is the voltage on the floating diffusion with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak to peak variation in V_{tcolr}–V_{tcols} is typically 10–20 mV. It is desirable to remove this source of column-to-column fixed pattern noise FPN. JPL has previously developed a double delta sampling (DDS) technique to eliminate the column-to-column FPN. This approach represented an improved version of the DDS circuitry.

Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent to one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal outputs (Vcol_R and VCOL_S) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers (VR_OUT and VS_OUT) that is free of the voltage threshold component.

This chip uses a similar pixel cell to that shown in FIG. 5. FIG. 9 shows the layout of the pixel cell. PG and RESET are routed horizontally in polysilicon while the pixel output is routed vertically in metal 1. Metal 2 was routed within the pixel for row selection. Metal 2 was also used as a light shield and covers most of the active area outside of the pixel array. The designed fill factor of the pixel is approximately 21%.

According to another feature, a logo can be formed on the acquired image by using a light blocking metal light shield. The light shield is formed to cover certain pixels in the shape of

the logo to be applied. This blocks out those underlying pixels in the array, thereby forming a logo in the shape of the blocked pixels.

The output saturation level of the sensor is 800 mv when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the floating diffusion node (e.g. 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 75,000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47,000 e– per supply volt.

Dark current was measured at less than 500 pA/cm^2.

Conversion gain (μV/e–) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1%—similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer.

The quantum efficiency of the detector was measured using a CVI 1/4 m monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards.

FIG. 10 shows a block diagram of an improved embodiment with new developments in the single chip camera active pixel sensor.

A block diagram of the embodiment is shown in FIG. 10, which shows the architectural layout of the sensor 1000. The sensor array 100 is surrounded by electrical connection pins 1002, each of which can have a predefined function. The sensor is arranged as a number of logical portions, including the sensor array 1002, the A to D converter array 1004, the D/A converters and support circuitry 1006. One side of the chip, here the left-most portion of the chip, forms timing and control circuit 1008. The other side, here the right most portion, includes the image acquisition structure—the photosensitive array and the analog to digital converters.

In this embodiment, the A/D converter array is formed of a plurality of columnar-shaped A/D converter devices 1010, preferably one of the devices for each row of the array. When each of the columnar A/D converter devices 1010 is associated with one of the columns of the sensor, the system operates in a so-called column-parallel mode where the information is output one column at a time. There are preferably 256 of the column-parallel 10 bit successive approximation A to D converters, one arranged under each column which it is associated. Each includes internal correlated double sampling ("CDS") and offset correction.

There are two inputs to the A to D converter. One is for the pixel reference (reset value) and the other is for the pixel "signal" value. CDS involves subtracting the pixel "signal" value from the pixel reset level for any given cycle. In operation, the pixel reset level, which is higher than the pixel "signal" value, is sampled and stored on a single fixed capacitor at one of the inputs. The pixel "signal" is sampled and stored at the other input on a bank of id logarithmically scaled capacitors, with values C/2"--, C/2, C/4, C/8, etc. The bottom plates of these capacitors are initially set to ground. There are 10 capacitors defining a 10-bit A to D converter. The voltage level "VREF", indicated in the figure, defines the dynamic range of the A to D converter. After the two inputs have been introduced, the A to D converter operation proceeds. First, the bottom plate of the largest capacitor (C/2) is switched from ground to VREF. This causes the "signal" side of the A to D converter to be roughly "signal" +VREF/2. If "signal" +VREF/2 is greater than the pixel reset value, the signal side of the A to D converter is returned to its initial value by switching the bottom plate of the C/2 capacitor back to ground. If pixel "signal" +VREF/2 is less than the pixel reset value, the bottom plate of the C/2 capacitor is kept at VREF. This set of operations is repeated for the remaining capacitors, in order of size, causing the "signal" side of the A to D converter to adjust in voltage increments of VREF/4, VREF/8, etc. As the algorithm proceeds the "signal" side of the A to D converter is forever approaching the reset side, until it is equal to it, to within the precision of the A to D converter. The voltage value VREF is produced by one of the on-chip DACs; changing this value alters the dynamic range and thus the gain of the A to D converter.

Due to fabrication inaccuracies, each A to D converter will have its own particular offset that will cause fixed

pattern noise. To suppress this fixed pattern noise, each A to D converter has offset correction circuitry. On the "signal" side of the A to D converter is a secondary bank of logarithmically scaled capacitors, used for this purpose. Before reading out a frame of data, the same voltage is applied to the two inputs of the A to D converter (pixel reset). The A to D converter operation, described above, is performed with the secondary bank of capacitors. The result for a perfect A to D converter would be zero, but in this case represents the A to D converter offset. This offset voltage is added to the signal side of the A to D converter to auto-zero the A to D converter in subsequent operations.

Certain analog references are needed on the chip. These analog references are used, for example, for the successive approximation A/D converter. They are also used for biasing the operational amps, such as tail currents in the operational amps, and the like. The analog references can also be used for adjusting the gain of the A/D converter. For example, one may want a high gain A/D converter for low light, but a low gain A/D converter for higher light operations. The current consumed by the A/D converter can be increased to make the A/D conversion occur faster. These references are generated with on-chip DACs thus eliminating the need for external analog reference generators and allowing the chip to have a complete digital interface.

All of these analog references are formed from a group of on-chip D to A converters, fed with a digital input. The A to D converter conversion time is also programmable. The clock cycle of the A/D converter can be increased in order to make the A/D conversion occur faster. This requires more current through the A/D converter to provide a faster settling time. For example, if the device is being used in a wireless camera, the throughput may be bandwidth limited. Therefore, A to D converter's conversion time can be reduced to save power.

This allows many of the operations to be carried out using digital external circuitry. The camera can be programmed and receive commands through a single digital pin **1002**. The programming includes the analog references noted above, and also programmable exposure time, programmable windowing, and subsampling. Also, pixel sample and hold time can be programmed in this way, by setting the amount of time that elapses between reset and sampling of the image in the correlated double sampling circuit.

A special advantage is obtained by using a single pin to obtain all interface into the chip by serially transferring the data. This also specially advantageous when used for wireless communication, as shown in the block diagram of FIG. 2. When a wireless control is effected, the control is inherently serial. The RF signal stream can then be downconverted and input on a single digital serial pin **202**. A special advantage of this system is that no data conversion is necessary since the chip accepts a serial command in the same form as the RF stream.

This system can also be programmed into a number of different imaging modes using the support circuitry. The modes are described herein.

This system can also be programmed into to support a number of different imaging modes using the support circuitry. It can be configured to image continuously or take a digital still. After taking a digital still the camera automatically enters a low power idle mode where it consumes 10 microwatts of power. The modes include a low power idle mode. These low power idle modes are well known in the art. Here it is implemented by turning off the digital-to-analog converters on the chip. That has the effect of turning off the other circuitry. Also, a switch can be placed in series with the analog circuitry, thereby turning off that circuitry. One of these exemplary modes is described in U.S. Pat. No. 5,504,909.

A warm-up timer can also be digitally programmed to delay image capture to some later time. A programmable warm-up timer enables determining how long to wait before capturing the image. For example, a warm-up timer may be used so that the user can take a picture of oneself. The warm-up timer uses a down counter which counts down from a digital preset number also input through the serial input pin. Hence, each of the preset numbers represents a time.

The image can be provided in a number of different formats, including serial and parallel. The preferred image format is serial 10-bits. However, one could obtain less resolution from the system. The image information can also be provided in full or half duplex.

The preferred image format: is serial 10-bits. However, one could obtain less resolution from the system. The chip can be programmed to insert edges in the serial output data stream to ease data recovery. It can also be configured to provide horizontal and vertical frame synes and pixel, row and frame clocks The chip can also be commanded to output the internal state of its registers. Allowing a user to verify settings such as the exposure time, window size and output data format. The way in which all of this would be done is well known in the art.

A number of pins are used to provide input to, and receive output from, the chip for various purposes. However, the system is designed to operate with only five pins, which are preferably connected to 8 of the 64 external pins. These eight essential pins are all located on one side of the chip, which reduces the post-packaging footprint area of the chip. Digital pads, when not connected, are automatically pulled to ground when the chip is powered on and thus do not require connections. This has advantages when it is desired to mount the chip in a special way, for example on the chip's edge as shown in FIG. **14**.

The five necessary pins are command, clock, data out, power, and ground. These five essential pins are all on one side of the chip. This allows, for example, a lens or other such device right on the chip. The five necessary pins include command, clock, data out, power, and ground. These five essential pins are all on one side of the chip. However, since the device is preferably included in a 32-pin chip, this enables 32 minus 5 which equals 27 other pins for other operations.

The physical size of the chip is minimized by allowing only wires connected to 8 pins on the chip with split power and ground. This leaves approximately 32−8=24 other pins. Preferably, the 8 pins used for power and ground are located on one side of the imager in order to minimize the post-packing footprint area.

FIG. **11**A shows the signal chain of the one-chip device, and FIG. **11**B shows the timing diagram. A major difference from the first embodiment is that the floating diffusion is normally maintained in reset. This means that a soft reset is not required.

In operation, as shown in FIGS. **11**B–C, first the reset and signal pixel values are sampled. They are then subtracted, digitized and output. This enable the operation to occur in a minimal amount of time.

A block diagram of the hardware operations carried out in the support circuitry is shown in FIG. 12. FIG. 12 shows this systems being used as a wireless camera **200**, however, it could also alternatively be used in a wired operation. FIG. 12 also shows the system with only the five necessary output

pins including the input data pin **202**, output data pin **204**, power and ground **206**, **208**, and the clock pin **210**. The clock is used for synchronization, and to indicate when the operation is ready.

An input data packet is shown in FIG. **13**. Line **1300** indicates the clock signal on line **210**. The falling edge of clock signal **1300** on line **210** indicates the start of the data packet **1310**. Data packet **1310** includes a header portion **1312** which is a reserved sequence, followed by a packet which has 20-bits of information, followed by a tail portion **1316**. The packet indicates some information, either a format of the information that will follow, or the actual further data for processing.

Although only a few embodiments have been described in detail above, other embodiments are contemplated by the inventor and are intended to be encompassed within the following claims. In addition, other modifications are contemplated and are also intended to be covered.

What is claimed is:

1. A single-chip camera apparatus, comprising:

a substrate, having integrated thereon a sensor array of photosensitive elements;

an A to D converter circuit, operating to convert outputs of said sensor array to a digital value;

timing and control and support circuitry, including a serial communication network,

said substrate including an external periphery with a plurality of sides, including connection pins extending from said periphery to circuitry inside said periphery, said chip being capable of operation with only power, ground, serial, clock, and output pins, wherein all of said necessary pins are located on one of said sides of said periphery, wherein said support circuitry includes an analog reference voltage associated therewith, wherein a digital word is input to said input pin indicating said analog reference, and said support circuitry includes a digital-to-analog converter, located on said substrate, for producing said analog reference.

2. A system as in claim **1** wherein said analog reference is a reference for a successive approximation A to D converter.

3. A system as in claim **1** wherein said reference is an exposure time for said camera.

4. A system as in claim **1** wherein said reference is a sample and hold time.

5. A system as in claim **1** wherein said reference is a time for a warm-up timer.

6. A totally digital single-chip camera apparatus, comprising:

a substrate, having integrated thereon a sensor array of photosensitive elements;

an A to D converter circuit, on said substrate, operating to convert outputs of said sensor array to a digital value as an output; and

timing and control and support circuitry, on said substrate, including a serial communication network, receiving digital values as input,

wherein at least one circuit on said substrate includes an analog reference voltage associated therewith, wherein a digital word is input indicating said analog reference, and said support circuitry includes a digital-to-analog converter, on said substrate chip, for producing said analog reference based on said digital word.

* * * * *

EXHIBIT E

US006555842B1

(12) **United States Patent**
Fossum et al.

(10) **Patent No.: US 6,555,842 B1**
(45) **Date of Patent: *Apr. 29, 2003**

(54) **ACTIVE PIXEL SENSOR WITH INTRA-PIXEL CHARGE TRANSFER**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 31 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/604,846**

(22) Filed: **Jun. 27, 2000**

Related U.S. Application Data

(63) Continuation of application No. 08/558,521, filed on Nov. 16, 1995, now Pat. No. 6,101,232, which is a continuation of application No. 08/188,032, filed on Jan. 28, 1994, now Pat. No. 5,471,515.

(51) **Int. Cl.**[7] **H01L 29/04**

(52) **U.S. Cl.** **257/59**; 257/222; 257/232; 257/234; 257/239; 257/292; 257/294

(58) **Field of Search** 257/222, 232, 257/234, 239, 292, 294

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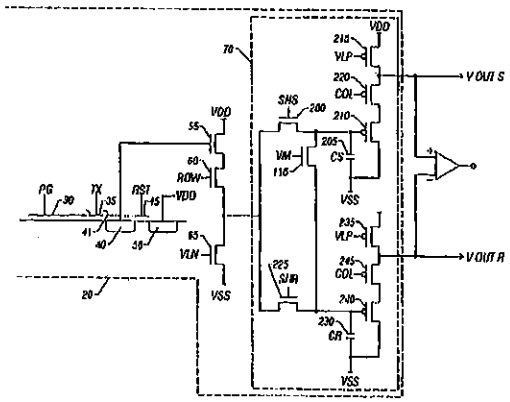
(57) **ABSTRACT**

An imaging device formed as a monolithic complementary metal oxide semiconductor integrated circuit in an industry standard complementary metal oxide semiconductor process, the integrated circuit including a focal plane array of pixel cells, each one of the cells including a photogate overlying the substrate for accumulating photo-generated charge in an underlying portion of the substrate, a readout circuit including at least an output field effect transistor formed in the substrate, and a charge coupled device section formed on the substrate adjacent the photogate having a sensing node connected to the output transistor and at least one charge coupled device stage for transferring charge from the underlying portion of the substrate to the sensing node.

19 Claims, 2 Drawing Sheets



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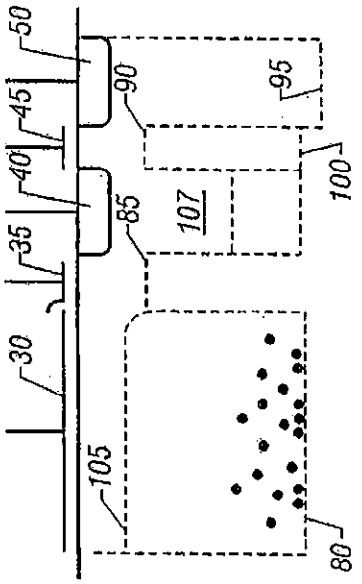

FIG. 4

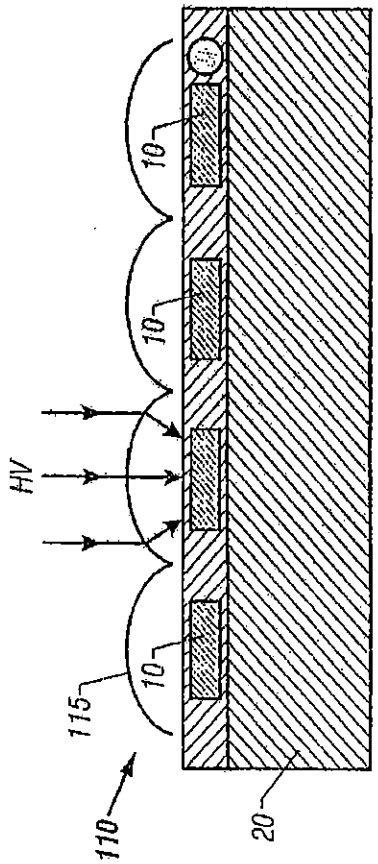

FIG. 5

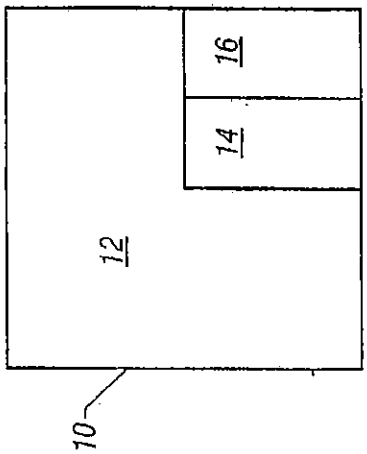

FIG. 1

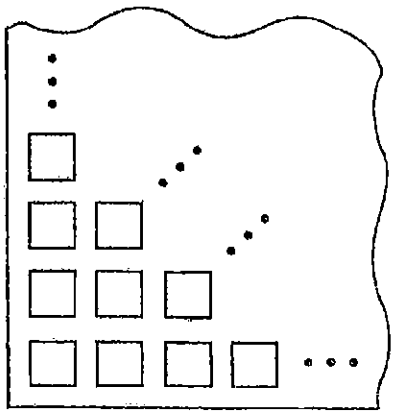

FIG. 2

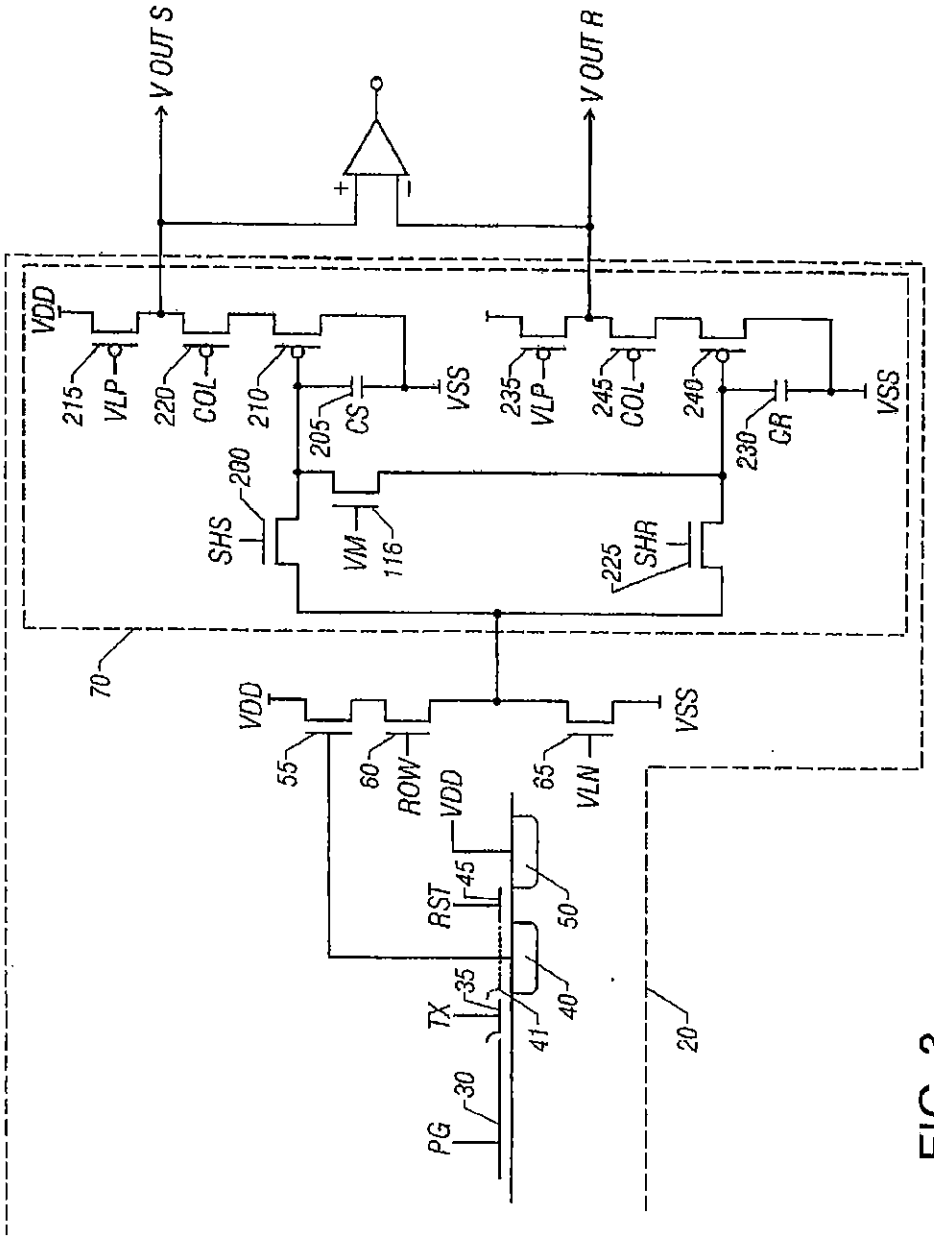
V OUT S
V OUT R
VDD
215
VLP
220
COL
210
205
CS
VSS
235
VLP
245
COL
240
230
GR
VSS
200
SHS
VM
116
225
SHR
70
VDD
55
60
ROW
VDD
65
VLN
VSS
RST
45
50
TX
35
40
41
20
PG
30

FIG. 3

ACTIVE PIXEL SENSOR WITH INTRA-PIXEL CHARGE TRANSFER

This application is a continuation of Ser. No. 08/558,521 filed Nov. 16, 1995 U.S. Pat. No. 6,101,232 which is a continuation of Ser. No. 08/188,032 filed Jan. 28, 1994 U.S. Pat. No. 5,471,515.

ORIGIN OF THE INVENTION

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

BACKGROUND OF THE INVENTION

1. Technical Field

The invention is related to semiconductor imaging devices and in particular to a silicon imaging device which can be fabricated using a standard CMOS process.

2. Background Art

There are a number of types of semiconductor imagers, including charge coupled devices, photodiode arrays, charge injection devices and hybrid focal plane arrays. Charge coupled devices enjoy a number of advantages because they are an incumbent technology, they are capable of large formats and very small pixel size and they facilitate noiseless charge domain processing techniques (such as binning and time delay integration). However, charge coupled device imagers suffer from a number of disadvantages. For example, they exhibit destructive signal read-out and their signal fidelity decreases as the charge transfer efficiency raised to the power of the number of stages, so that they must have a nearly perfect charge transfer efficiency. They are particularly susceptible to radiation damage, they required good light shielding to avoid smear and they have high power dissipation for large arrays.

In order to ameliorate the charge transfer inefficiency problem, charge coupled device (CCD) imagers are fabricated with a specialized CCD semiconductor fabrication process to maximize their charge transfer efficiency. The difficulty is that the standard CCD process is incompatible with complementary metal oxide semiconductor (CMOS) processing, while the image signal processing electronics required for the imager are best fabricated in CMOS. Accordingly, it is impractical to integrate on-chip signal processing electronics in a CCD imager. Thus, the signal processing electronics is off-chip. Typically, each column of CCD pixels is transferred to a corresponding cell of a serial output register, whose output is amplified by a single on-chip amplifier (e.g., a source follower transistor) before being processed in off-chip signal processing electronics. As a result, the read-out frame rate is limited by the rate at which the on-chip amplifier can handle charge packets divided by the number of pixels in the imager.

The other types of imager devices have problems as well. Photodiode arrays exhibit high noise due to so-called kTC noise which makes it impossible to reset a diode or capacitor node to the same initial voltage at the beginning of each integration period. Photodiode arrays also suffer from lag. Charge injection devices also suffer from high noise, but enjoy the advantage of non-destructive readout over charge coupled devices.

Hybrid focal plane arrays exhibit less noise but are prohibitively expensive for many applications and have relatively small array sizes (e.g., 512-by-512 pixels).

What is needed is an imager device which has the low kTC noise level of a CCD without suffering from the destructive readout tendencies of a CCD.

SUMMARY OF THE DISCLOSURE

The invention is embodied in an imaging device formed as a monolithic complementary metal oxide semiconductor integrated circuit in an industry standard complementary metal oxide semiconductor process, the integrated circuit including a focal plane array of pixel cells, each one of the cells including a photogate overlying the substrate for accumulating photo-generated charge in an underlying portion of the substrate, a readout circuit including at least an output field effect transistor formed in the substrate, and a charge coupled device section formed on the substrate adjacent the photogate having a sensing node connected to the output transistor and at least one charge coupled device stage for transferring charge from the underlying portion of the substrate to the sensing node.

In a preferred embodiment, the sensing node of the charge coupled device stage includes a floating diffusion, and the charge coupled device stage includes a transfer gate overlying the substrate between the floating diffusion and the photogate. This preferred embodiment can further include apparatus for periodically resetting a potential of the sensing node to a predetermined potential, including a drain diffusion connected to a drain bias voltage and a reset gate between the floating diffusion and the drain diffusion, the reset gate connected to a reset control signal.

Preferably, the output transistor is a field effect source follower transistor, the floating diffusion being connected to a gate of the source follower transistor. Preferably, the readout circuit further includes a double correlated sampling circuit having an input node connected to the output transistor. In the preferred implementation, the double correlated sampling circuit samples the floating diffusion immediately after it has been reset at one capacitor and then, later, at the end of the integration period at another capacitor. The difference between the two capacitors is the signal output. In accordance with a further refinement, this difference is corrected for fixed pattern noise by subtracting from it another difference sensed between the two capacitors while they are temporarily shorted.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating the architecture of an individual focal plane cell of the invention.

FIG. 2 is a plan view of an integrated circuit constituting a focal plane array of cells of the type illustrated in FIG. 1.

FIG. 3 is a schematic diagram of the cell of FIG. 1.

FIG. 4 is a graph of the surface potential in the charge transfer section of the cell of FIG. 3.

FIG. 5 is a cross-sectional view of an alternative embodiment of the focal plane array of FIG. 2 including a microlens layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a simplied block diagram of one pixel cell 10 of a focal plane array of many such cells formed in an integrated circuit. Each cell 10 includes a photogate 12, a charge transfer section 14 adjacent the photogate 12 and a readout circuit 16 adjacent the charge transfer section 14. FIG. 2 shows a focal plane array of many cells 10 formed on a silicon substrate 20. FIG. 3 is a simplified schematic dia-

gram of a cell 10. Referring to FIG. 3, the photogate 12 consists of a relative large photogate electrode 30 overlying the substrate 20. The charge transfer section 14 consists of a transfer gate electrode 35 adjacent the photogate electrode 30, a floating diffusion 40, a reset electrode 45 and a drain diffusion 50. The readout circuit 16 consists of a source follower field effect transistor (FET) 55, a row select FET 60, a load FET 65 and a correlated double sampling circuit 70.

Referring to the surface potential diagram of FIG. 4, the photogate electrode 30 is held by a photogate signal PG at a positive voltage to form a potential well 80 in the substrate 20 in which photo-generated charge is accumulated during an integration period. The transfer gate electrode 35 is initially held at a less positive voltage by transfer gate signal TX to form a potential barrier 85 adjacent the potential well 80. The floating diffusion 40 is connected to the gate of the source follower FET 55 whose drain is connected to a drain supply voltage VDD. The reset electrode 45 is initially held by a reset signal RST at a voltage corresponding to the voltage on the transfer gate 35 to form a potential barrier 90 thereunder. The drain supply voltage VDD connected to the drain diffusion 50 creates a constant potential well 95 underneath the drain diffusion 50.

During the integration period, electrons accumulate in the potential well 80 in proportion to photon flux incident on the substrate 20 beneath the photogate electrode 30. At the end of the integration period, the surface potential beneath the floating diffusion 40 is quickly reset to a potential level 100 slightly above the potential well 95. This is accomplished by the reset signal RST temporarily increasing to a higher positive voltage to temporarily remove the potential barrier 90 and provide a downward potential staircase from the transfer gate potential barrier 85 to the drain diffusion potential well 95, as indicated in the drawing of FIG. 4. After the reset gate 45 is returned to its initial potential (restoring the potential barrier 90), the readout circuit 70 briefly samples the potential of the floating diffusion 40, and then the cell 10 is ready to transfer the photo-generated charge from beneath the photogate electrode 30. For this purpose, the photogate signal PG decreases to a less positive voltage to form a potential barrier 105 beneath the photogate electrode 30 and thereby provide a downward staircase surface potential from the photogate electrode 30 to the potential well 100 beneath the floating diffusion 40. This transfers all of the charge from beneath the photogate electrode 30 to the floating diffusion 40, changing the potential of the floating diffusion 40 from the level (100) at which it was previously reset to a new level 107 indicative of the amount of charge accumulated during the integration period. This new potential of the floating diffusion 40 is sensed at the source of the source follower FET 55. However, before the readout circuit 70 samples the source of the source follower FET 55, the photogate signal PG returns to its initial (more positive) voltage. The entire process is repeated for the next integration period.

The readout circuit 70 consists of a signal sample and hold (S/H) circuit including an S/H FET 200 and a signal store capacitor 205 connected through the S/H FET 200 and through the row select FET 60 to the source of the source follower FET 55. The other side of the capacitor 205 is connected to a source bias voltage VSS. The one side of the capacitor 205 is also connected to the gate of an output FET 210. The drain of the output FET is a connected through a column select FET 220 to a signal sample output node VOUTS and through a load FET 215 to the drain voltage VDD. A signal called "signal sample and hold" (SHS) briefly turns on the S/H FET 200 after the charge accumulated beneath the photogate electrode 30 has been transferred to the floating diffusion 40, so that the capacitor 205 stores the source voltage of the source follower FET 55 indicating the amount of charge previously accumulated beneath the photogate electrode 30.

The readout circuit 70 also consists of a reset sample and hold (S/H) circuit including an S/H FET 225 and a signal store capacitor 230 connected through the S/H FET 225 and through the row select FET 60 to the source of the source follower FET 55. The other side of the capacitor 230 is connected to the source bias voltage VSS. The one side of the capacitor 230 is also connected to the gate of an output FET 240. The drain of the output FET 240 is connected through a column select FET 245 to a reset sample output node VOUTR and through a load FET 235 to the drain voltage VDD. A signal called "reset sample and hold" (SHR) briefly turns on the S/H FET 225 immediately after the reset signal RST has caused the resetting of the potential of the floating diffusion 40, so that the capacitor 230 stores the voltage at which the floating diffusion has been reset to.

The readout circuit provides correlated double sampling of the potential of the floating diffusion, in that the charge integrated beneath the photogate 12 each integration period is obtained at the end of each integration period from the difference between the voltages at the output nodes VOUTS and VOUTR of the readout circuit 70. This eliminates the effects of kTC noise because the difference between VOUTS and VOUTR is independent of any variation in the reset voltage RST, a significant advantage.

Referring to FIG. 5, a transparent refractive microlens layer 110 may be deposited over the top of the focal plane array of FIG. 2. The microlens layer 110 consists of spherical portions 115 centered over each of the cells 10 and contoured so as to focus light toward the center of each photogate 12. This has the advantage of using light that would otherwise fall outside of the optically active region of the photogate 12. For example, at least some of the light ordinarily incident on either the charger transfer section 14 or the readout circuit 16 (FIG. 1) would be sensed in the photogate area with the addition of the microlens layer 110.

Preferably, the focal plane array corresponding to FIGS. 1–4 is implemented in CMOS silicon using an industry standard CMOS fabrication process. Preferably, each of the FETs is a MOSFET, the FETs 55, 60, 65, 200 and 225 being n-channel devices and the FETs 210, 220, 225, 230. 240, 245 being p-channel devices. The n-channel MOSFETS and the CCD channel underlying the gate electrodes 30, 35, 45 and the diffusions 40 and 50 may be located in a p-well while the remaining (p-channel) devices are located outside of the p-well. The gate voltage VLP applied to the gates of the p-channel load FETs 215 and 235 is a constant voltage on the order of +2.5 volts. The gate voltage VLN applied to the n-channel load FET 65 is a constant voltage on the order of +1.5 volts.

Since the charge transfer section 14 involves only a single CCD stage between the photogate 12 and the floating diffusion 40 in the specific embodiment of FIG. 3, there is no loss due to charge transfer inefficiency and therefore there is no need to fabricate the device with a special CCD process. As a result, the readout circuit 70 as well as the output circuitry of the FETs 55, 60 and 65 can be readily implemented as standard CMOS circuits, making them extremely inexpensive. However, any suitable charge coupled device architecture may be employed to implement the charge transfer section 14, including a CCD having more

than one stage. For example, two or three stages may be useful for buffering two or three integration periods.

Other implementations of the concept of the invention may be readily constructed by the skilled worker in light of the foregoing disclosure. For example, the floating diffusion **40** may instead be a floating gate electrode. The signal and reset sample and hold circuits of the readout circuit **70** may be any suitable sample and hold circuits. Moreover, shielding of the type well-known in the art may be employed defining an aperture surrounding the photogate **12**. Also, the invention may be implemented as a buried channel device.

Another feature of the invention which is useful for eliminating fixed pattern noise due to variations in FET threshold voltage across the substrate **20** is a shorting FET **116** across the sampling capacitors **205**, **235**. After the accumulated charge has been measured as the potential difference between the two output nodes VOUTS and VOUTR, a shorting signal VM is temporarily applied to the gate of the shorting FET **116** and the VOUTS-to-VOUTR difference is measured again. This latter difference is a measure of the disparity between the threshold voltages of the output FETs **210**, **240**, and may be referred to as the fixed pattern difference. The fixed pattern difference is subtracted from the difference between VOUTS and VOUTR measured at the end of the integration period, to remove fixed pattern noise.

As previously mentioned herein, a floating gate may be employed instead of the floating diffusion **40**. Such a floating gate is indicated schematically in FIG. **3** by a simplified dashed line floating gate electrode **41**.

Preferably, the invention is fabricated using an industry standard CMOS process, so that all of the dopant concentrations of the n-channel and p-channel devices and of the various diffusions are in accordance with such a process. In one implementation, the area of the L-shaped photogate **12** (i.e., the photogate electrode **30**) was about 100 square microns; the transfer gate electrode **35** and the reset gate electrode were each about 1.5 microns by about 6 microns; the photogate signal PG was varied between about +5 volts (its more positive voltage) and about 0 volts (its less positive voltage; the transfer gate signal TX was about +2.5 volts; the reset signal RST was varied between about +5 volts (its more positive voltage) and about +2.5 volts (its less positive voltage); the drain diffusion **50** was held at about +5 volts.

While the invention has been described in detail by specific reference to preferred embodiments, it is understood that variations and modifications may be made without departing from the true spirit and scope of the invention.

What is claimed is:

1. An imaging device including a monolithic semiconductor integrated circuit substrate, said imaging device comprising a focal plane array of pixel cells, each of said cells comprising:

a photoreceptor, adjacent said substrate, to control accumulating photo-generated charge

a readout circuit comprising at least a buffering transistor and a selecting transistor, formed in said substrate;

a coupling section formed on said substrate adjacent said photoreceptor, having a sensing node connected to said output transistor and at least one coupling stage for transferring said photogenerated charge to said sensing node; and

wherein said transistors in said readout circuit are formed of an integrated circuit technology which is compatible with complimentary metal oxide semiconductor (CMOS) technology, formed on said substrate, said substrate being of a first conductivity type, said readout circuit comprising transistors of a first conductivity type, a well region of a second conductivity type in said substrate and plural semiconductor transistors of a second conductivity type formed in said well region.

2. An imaging device as in claim 1, further comprising a microlens layer formed on at least part of the substrate to refract light incident on an area of the substrate that includes circuitry including at least said readout circuit, to the photoreceptor.

3. An imaging device comprising a focal plane array of pixel cells, each of said pixel cells including a monolithic semiconductor integrated circuit substrate, each of said pixel cells comprising:

a photoreceptor overlying a first portion of said substrate and operating to accumulate photo-generated charge in the first portion of said substrate that underlies said photogate;

a charge transfer section, formed in said substrate adjacent said photogate, having a sensing node adjacent said photoreceptor and at least one charge coupling stage, operating to transfer charge from said first portion of said substrate to said sensing node; and

a readout circuit connected to said sensing node and to no other sensing node of any other one of said pixel cells, so that said readout circuit of each said one of said pixel cells is associated with only one photoreceptor and only one charge transfer section, said readout circuit including at least a buffering transistor and a selection transistor.

4. The imaging device of claim **3** wherein:

said sensing node of said charge transfer section stage comprises a floating node; and

said charge coupling stage comprises a transfer gate between said floating node and said photogate.

5. The imaging device of claim **4** wherein said floating node is one of: (a) a floating diffusion, and (b) a floating gate.

6. An imaging device as in claim **3**, wherein said readout circuit includes a sampling element which stores the charge received from said substrate, and a shorting element which shorts across the sampling element after the charge is read.

7. A device as in claim **6**, wherein said sampling element is a capacitor and said shorting element is a shorting FET.

8. An imaging device as in claim **3**, wherein said readout circuit is formed of an integrated circuit technology which is compatible with complimentary metal oxide semiconductor (CMOS) technology.

9. An imaging device, comprising:

a substrate of a type which can store optical charge therein, said substrate formed of a plurality of pixel cells, each pixel cell comprising:

an optical charge storage section, including a photoreceptor;

a charge transfer section, having a sensing node, and having a first state in which charge from the photoreceptor is isolated from the sensing node and a second state in which charge from the photoreceptor is coupled to said sensing node; and

a readout circuit, having an input connected to said sensing node, said readout circuit connected to no other nodes of any of the other pixel cells of the device so that each optical charge storage section and charge transfer section is associated with only one readout circuit.

10. A device as in claim **9**, wherein said sensing node of said charge transfer section includes a first floating element, which is initially isolated from charge and is later coupled to the charge.

11. An device as in claim 10, wherein said readout circuit includes a first sampling element for sampling an initial potential on the first floating element while said charge transfer section is isolated from said first floating element, and a second sampling element for sampling a later potential on said floating element when said charge transfer section is coupled to the first floating element.

12. A device as in claim 11, wherein said readout circuit includes double sampling circuitry subtracting said initial potential from said later potential to produce a difference, and wherein an output of said readout circuit is proportional to the difference.

13. A device as in claim 12, wherein said sampling elements comprise capacitors.

14. A device as in claim 9, wherein said readout circuit includes an input node to the readout circuit which is directly connected to the sensing node of said charge transfer section, said input node including a follower circuit.

15. A device as in claim 9, further comprising a microlens layer formed on at least part of the substrate to refract light incident on an area of the substrate that includes circuitry including at least said readout circuit, to the optical charge storage section.

16. An imaging device as in claim 9, wherein said readout circuit is formed of an integrated circuit technology which is compatible with complimentary metal oxide semiconductor (CMOS) technology.

17. An imaging device, comprising:

a focal plane array of pixel cells, including a substrate of a type which can store optical charge therein;

each pixel cell formed in a predetermined area of said substrate, and comprising:

an optical charge storage section, including a photoreceptor overlying a first portion of said predetermined area of said substrate which accumulates charge therein;

a plurality of circuitry elements, formed in a second portion of said predetermined area; and

a microlens, overlying at least said second portion, and directing light impinging on said second portion to said first portion.

18. An imaging device as in claim 17, wherein said plurality of circuitry elements comprises:

a charge transfer section, having a sensing node, and having a first state in which charge in the substrate is isolated from the sensing node and a second state in which charge in the substrate is coupled to said sensing node; and

a readout circuit, having an input connected to said sensing node, said readout circuit connected to no other nodes of any of the other pixel cells of the device so that each optical charge storage section and charge transfer section is associated with only one readout circuit.

19. An imaging device including a monolithic semiconductor integrated circuit substrate, said imaging device comprising a focal plane array of pixel cells, each one of said cells comprising:

a photosensor coupled to said substrate, and accumulating photo-generated charge in said substrate;

a readout circuit comprising at least a select transistor and a buffering transistor, formed in said substrate;

a coupling section, formed on said substrate adjacent said photgate, having a sensing node connected to said output transistor and at least one coupling stage which transfers charge from said underlying portion of said substrate to said sensing node.

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