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Attorneys for Plaintiff
ELPIDA MEMORY, INC.

E-FILING

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

ELPIDA MEMORY, INC.,

Plaintiff,

v.

NANYA TECHNOLOGY CORPORATION; NANYA TECHNOLOGY CORPORATION, U.S.A.; AND NANYA TECHNOLOGY CORPORATION DELAWARE

Defendants.

Case No. CV 11-04411

COMPLAINT FOR PATENT INFRINGEMENT

MEJ

DEMAND FOR JURY TRIAL

Plaintiff Elpida Memory, Inc. ("Elpida") for its complaint against Defendants Nanya Technology Corporation; Nanya Technology Corporation, U.S.A.; and Nanya Technology Corporation Delaware (collectively, "Nanya") alleges as follows:

PARTIES

1. Plaintiff Elpida is organized under the laws of Japan with its principal place of business at 2-1, Yaesu 2-chome, Chuo-ku, Tokyo 104-0028 Japan.

2. On information and belief Defendant Nanya Technology Corporation ("NTC Taiwan") is organized under the laws of Taiwan with its principal place of business at Hwa Ya Technology Park 669, Fu Hsing 3rd Road, Kueishan, Taoyuan, Taiwan, R.O.C.

3. On information and belief Defendant Nanya Technology Corporation, U.S.A. ("NTC USA") is organized under the laws of California with its principal place of business at 5104 Old Ironsides Dr., Suite 113, Santa Clara, CA 95054, and has as an agent for service of process located at 818 W Seventh St., Los Angeles, CA 90017.

4. On information and belief, NTC USA is a wholly owned independent subsidiary of NTC Taiwan and is responsible for sales and marketing of NTC Taiwan's SDRAM products throughout the United States.

5. On information and belief, in addition to its sales force, NTC USA employs field application engineers who provide technical support for NTC Taiwan's products that are being offered for sale or have been sold. The NTC engineers provide in-depth technical knowledge of NTC Taiwan's products in both pre-sales and post-sales roles.

6. On information and belief, the majority of NTC USA's employees works at NTC USA's headquarters in Santa Clara, California and lives within the Northern District of California. The officers and the majority of the senior management for NTC USA work at the Santa Clara headquarters, including Ken Hurley (Chief Executive Officer), Steve Hsu (Vice-President-CFO), and Brian Donahue (Sales & Marketing Director).

7. On information and belief Defendant Nanya Technology Corporation Delaware is organized under the laws of Delaware with its principal place of business at 5104 Old Ironsides Dr., Suite 113, Santa Clara, CA 95054, and has an agent for service of process located at 818 W Seventh St., Los Angeles, CA 90017.

JURISDICTION AND VENUE

8. This action arises under the patent laws of the United States, 35 U.S.C. §§ 1 *et*

seq., for infringement by Nanya of U.S. patents owned by Elpida. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338.

9. This Court has personal jurisdiction over Nanya because, on information and belief, Nanya does business and/or maintains a principal place of business in the State of California to satisfy both the requirements of due process and Rule 4(k)(2) of the Federal Rules of Civil Procedure. On information and belief, Nanya maintains a principal place of business in and has engaged in acts of infringement within the Northern District of California.

10. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391(b)-(d) and 1400(b).

INTRADISTRICT ASSIGNMENT

11. This action for patent infringement is assigned on a district-wide basis under Civil L.R. 3-2(c).

COUNT I

(Infringement of U.S. Patent No. 5,838,036)

12. Elpida is the owner of U.S. Patent No. 5,838,036 ("the '036 patent"), entitled "Semiconductor Memory Device Capable of Realizing a Minimum Memory Cell Area Approximate to a Theoretical Value." The '036 patent was duly and legally issued by the U.S. Patent and Trademark Office on November 17, 1998. A true and correct copy of the '036 patent is attached as Exhibit 1.

13. On information and belief, Nanya, by making, using, offering to sell, and/or selling in the United States, or importing into the United States, including this district, one or more products claimed in one or more claims of the '036 patent including, without limitation, Nanya's DDR3 SDRAM products including the Nanya Elixir N2CB2G80BN-CG 2Gbit DDR3 SDRAM, has committed acts of direct, contributory, and/or inducement of infringement under 35 U.S.C. § 271.

14. On information and belief, Nanya's infringement has been with full knowledge of the '036 patent and is, has been, and continues to be willful and deliberate.

15. Nanya's infringement has injured and damaged Elpida. Elpida is entitled to

recover damages adequate to compensate Elpida for Nanya's infringing activities in an amount to be determined at trial, but in no event less than a reasonably royalty, together with interest and costs.

16. Nanya's acts of infringement will continue unless and until enjoined by this Court, irreparably damaging Elpida.

COUNT II

(Infringement of U.S. Patent No. 6,894,363)

17. Elpida realleges and incorporates by reference the allegations stated in Paragraphs 1 through 11.

18. Elpida is the owner of U.S. Patent No. 6,894,363 ("the '363 patent"), entitled "Semiconductor Device Using Shallow Trench Isolation and Method of Fabricating the Same." The '363 patent was duly and legally issued by the U.S. Patent and Trademark Office on May 17, 2005. A true and correct copy of the '363 patent is attached as Exhibit 2.

19. On information and belief, Nanya, by making, using, offering to sell, and/or selling in the United States, or importing into the United States, including this district, one or more products claimed in one or more claims of the '363 patent including, without limitation, Nanya's DDR3 SDRAM products including the Nanya Elixir N2CB2G80BN-CG 2Gbit DDR3 SDRAM, has committed acts of direct, contributory, and/or inducement of infringement under 35 U.S.C. § 271.

20. On information and belief, Nanya's infringement has been with full knowledge of the '363 patent and is, has been, and continues to be willful and deliberate.

21. Nanya's infringement has injured and damaged Elpida. Elpida is entitled to recover damages adequate to compensate Elpida for Nanya's infringing activities in an amount to be determined at trial, but in no event less than a reasonably royalty, together with interest and costs.

22. Nanya's acts of infringement will continue unless and until enjoined by this Court, irreparably damaging Elpida.

COUNT III

(Infringement of U.S. Patent No. 7,060,588)

23. Elpida realleges and incorporates by reference the allegations stated in Paragraphs 1 through 11.

24. Elpida is the owner of U.S. Patent No. 7,060,588 ("the '588 patent"), entitled "Semiconductor Device Using Shallow Trench Isolation and Method of Fabricating the Same." The '588 patent was duly and legally issued by the U.S. Patent and Trademark Office on June 13, 2006. A true and correct copy of the '588 patent is attached as Exhibit 3.

25. On information and belief, Nanya, by making, using, offering to sell, and/or selling in the United States, or importing into the United States, including this district, one or more products made by a process claimed in one or more claims of the '588 patent including, without limitation, Nanya's DDR3 SDRAM products including the Nanya Elixir N2CB2G80BN-CG 2Gbit DDR3 SDRAM, has committed acts of direct, contributory, and/or inducement of infringement under 35 U.S.C. § 271.

26. On information and belief, Nanya's infringement has been with full knowledge of the '588 patent and is, has been, and continues to be willful and deliberate.

27. Nanya's infringement has injured and damaged Elpida. Elpida is entitled to recover damages adequate to compensate Elpida for Nanya's infringing activities in an amount to be determined at trial, but in no event less than a reasonably royalty, together with interest and costs.

28. Nanya's acts of infringement will continue unless and until enjoined by this Court, irreparably damaging Elpida.

COUNT IV

(Infringement of U.S. Patent No. 7,709,366)

29. Elpida realleges and incorporates by reference the allegations stated in Paragraphs 1 through 11.

30. Elpida is the owner of U.S. Patent No. 7,709,366 ("the '366 patent"), entitled "Semiconductor Device and Method of Manufacturing the Same." The '366 patent was duly and

legally issued by the U.S. Patent and Trademark Office on May 4, 2010. A true and correct copy of the '366 patent is attached as Exhibit 4.

31. On information and belief, Nanya, by making, using, offering to sell, and/or selling in the United States, or importing into the United States, including this district, one or more products made by a process claimed in one or more claims of the '366 patent including, without limitation, Nanya's DDR3 SDRAM products including the Nanya Elixir N2CB2G80BN-CG 2Gbit DDR3 SDRAM, has committed acts of direct, contributory, and/or inducement of infringement under 35 U.S.C. § 271.

32. On information and belief, Nanya's infringement has been with full knowledge of the '366 patent and is, has been, and continues to be willful and deliberate.

33. Nanya's infringement has injured and damaged Elpida. Elpida is entitled to recover damages adequate to compensate Elpida for Nanya's infringing activities in an amount to be determined at trial, but in no event less than a reasonably royalty, together with interest and costs.

34. Nanya's acts of infringement will continue unless and until enjoined by this Court, irreparably damaging Elpida.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Elpida requests that this Court enter judgment:

a. finding that Nanya has infringed and is infringing the '036, '363, '588, and '366 patents;

b. preliminarily and permanently enjoining Nanya and its officers, directors, agents, servants, employees, parents, subsidiaries, principals, and all other persons in active concert or participation with them from further infringement of the '036, '363, '588, and '366 patents;

c. requiring Nanya to pay damages pursuant to 35 U.S.C. § 284 in an amount to be determined at trial;

d. awarding increased damages, pursuant to 35 U.S.C. § 284, by reason of Nanya's willful infringement of the '036, '363, '588, and '366 patents;

e. ordering Nanya to pay damages for any post-trial, pre-judgment infringement in an amount determined by the Court;

f. ordering Nanya to pay pre-judgment interest, costs, and expenses to Elpida;

g. ordering Nanya to pay post-judgment interest until paid at the maximum lawful rate;

h. declaring this case exceptional under 35 U.S.C. § 285 and awarding Elpida its reasonable attorneys fees, expenses and costs incurred; and

i. granting Elpida such other and further relief as this Court may deem just and equitable, or that Elpida may be entitled to as a matter of law or equity.

Dated: September 6, 2011

MORGAN, LEWIS & BOCKIUS LLP

By _____
ANDREW J. GRAY IV

Attorneys for Plaintiff ELPIDA MEMORY, INC.

Of Counsel:
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Fax: (202) 739-3001
rbusby@morganlewis.com

JURY DEMAND

Plaintiff Elpida demands a trial by jury.

Dated: September 6, 2011

MORGAN, LEWIS & BOCKIUS LLP

By _____
ANDREW J. GRAY IV

Attorneys for Plaintiff ELPIDA MEMORY, INC.

Exhibit 1

US005838036A

United States Patent [19]

Mori

[11] Patent Number: 5,838,036

[45] Date of Patent: Nov. 17, 1998

[54] **SEMICONDUCTOR MEMORY DEVICE CAPABLE OF REALIZING A MINIMUM MEMORY CELL AREA APPROXIMATE TO A THEORETICAL VALUE**

[75] Inventor: **Hidemitsu Mori**, Tokyo, Japan

[73] Assignee: **NEC Corporation**, Japan

[21] Appl. No.: **746,440**

[22] Filed: **Nov. 8, 1996**

[30] **Foreign Application Priority Data**

Nov. 10, 1995 [JP] Japan 7-293198

[51] **Int. Cl.**^{6} **H01L 27/108**

[52] **U.S. Cl.** **257/296**; 257/306

[58] **Field of Search** 257/296, 301, 257/306, 532

[56] **References Cited**

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5,363,326	11/1994	Nakajima	365/149
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Eimori et al; "A Newly Designed Planar Stacked Capacitor Cell with High dielectric Constant Film for 256Mbit DRAM"; 1993; pp. 631–634; IEDM Tech. Dig.

Shibahara et al; "IGDRAM Cell with Diagonal Bit-Line (DBL) Configuration and Edge Operation MOS (EOS) FET"; 1994; pp. 639–642; IEDM Tech. Dig.

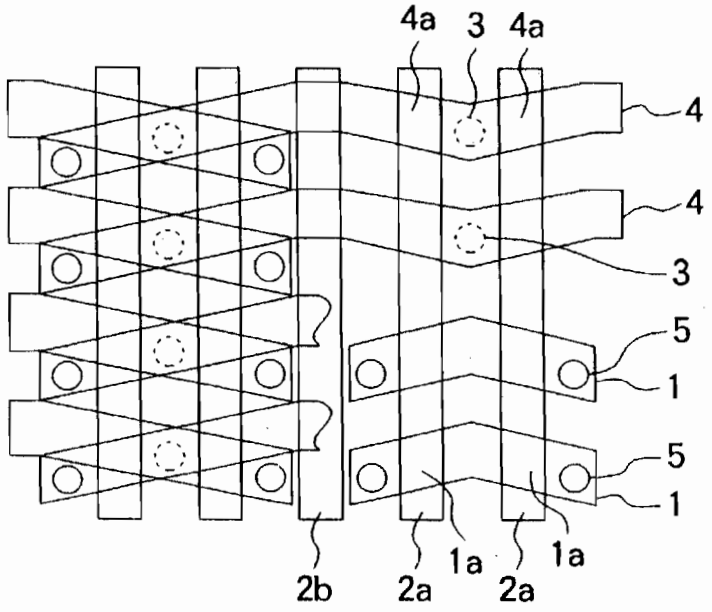
Primary Examiner—Sara W. Crane

Attorney, Agent, or Firm—Hayes, Soloway, Hennessey, Grossman, Hage, P.C.

[57] **ABSTRACT**

In semiconductor memory device, word lines (**2***a*) are arranged in parallel to each other on a semiconductor substrate (**9**). Each of the device active regions (**1**) has first oblique intersection portions (**1***a*) which obliquely intersect adjacent two of the word lines (**2***a*) in first oblique directions with a distance left between each of the device active regions (**1**) and the adjacent two of the word lines (**2***a*). Each of bit lines (**4**) has second oblique intersection portions (**4***a*) which obliquely intersect the adjacent two of the word lines (**4**) in second oblique directions reverse with respect to the first oblique directions with another distance left between each of the bit lines (**4**) and the adjacent two of the word lines (**2***a*). The first oblique directions of the first oblique intersection portions (**1***a*) of each of the device active regions (**1**) are reversed at every memory cell (or at every two memory cells). The second oblique directions of the second oblique intersection portions (**4***a*) of each of the bit lines (**4**) are reversed at every memory cell (or at every two memory cells).

5 Claims, 11 Drawing Sheets



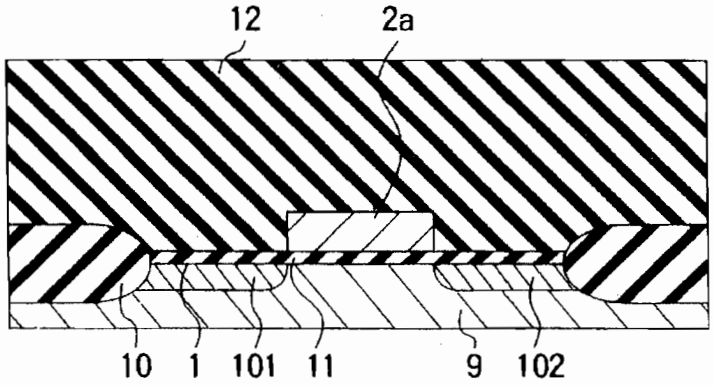


FIG. 1A
PRIOR ART

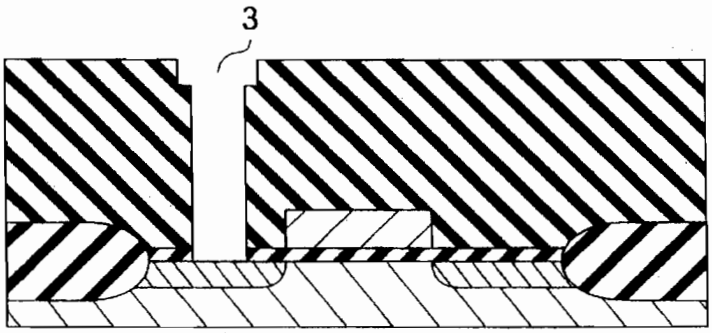


FIG. 1B
PRIOR ART

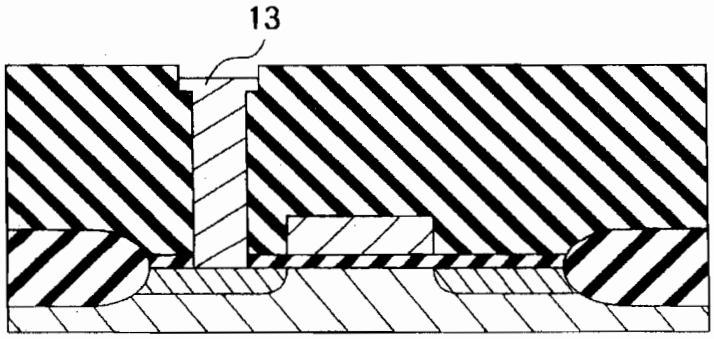


FIG. 1C
PRIOR ART

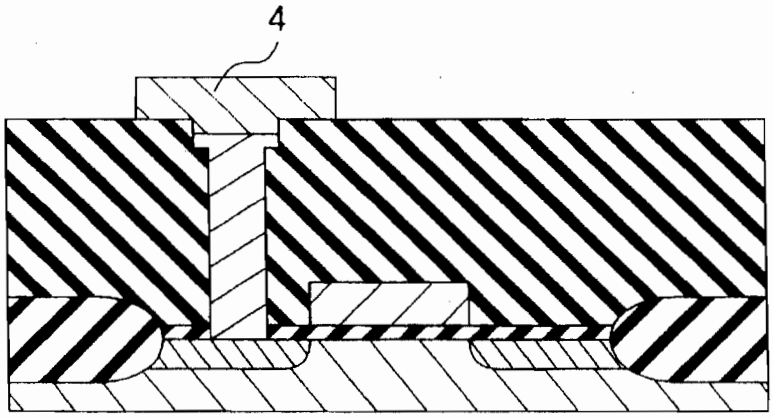


FIG. 1D
PRIOR ART

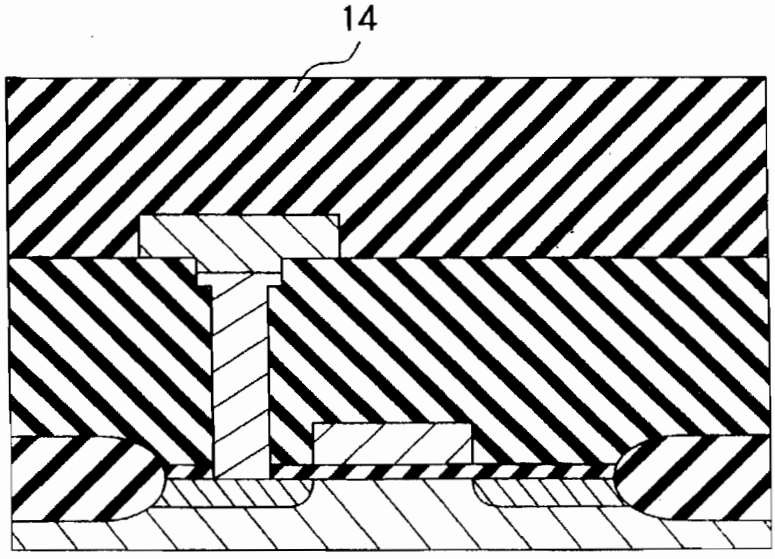


FIG. 1E
PRIOR ART

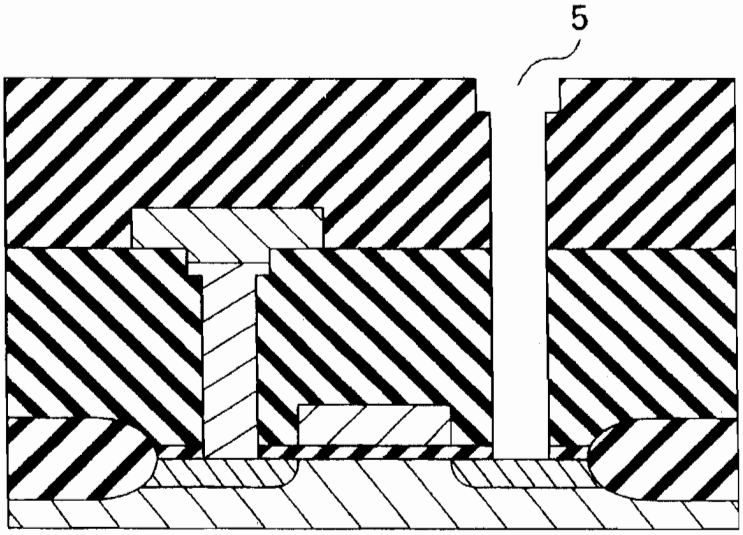


FIG. 1F
PRIOR ART

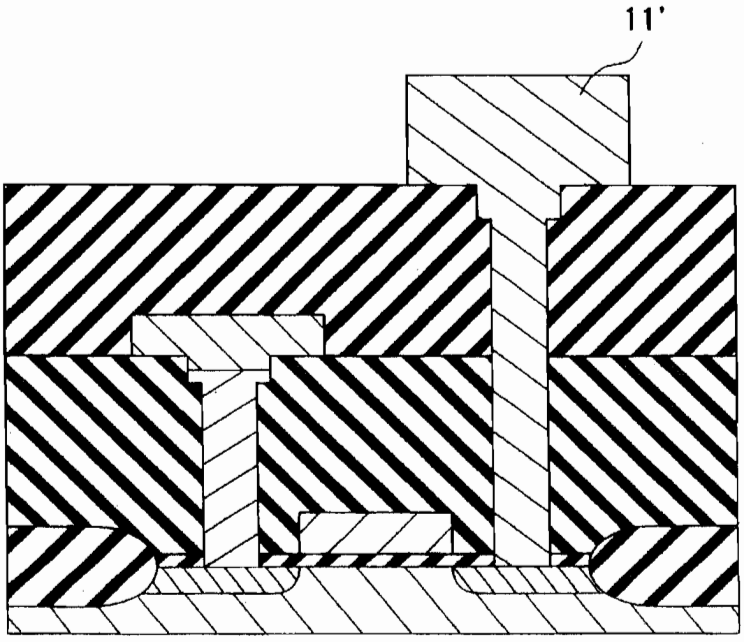


FIG. 1G
PRIOR ART

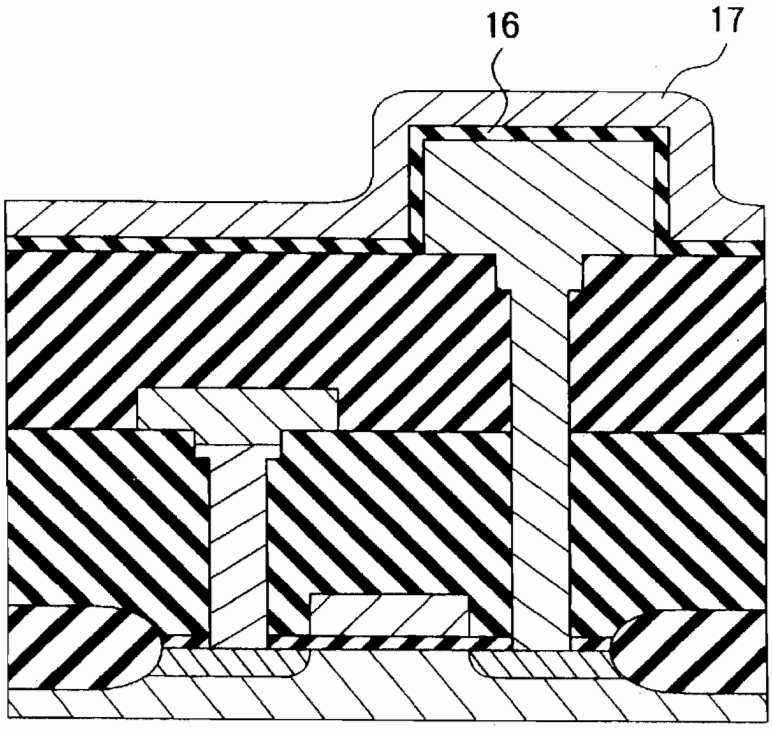


FIG. 1H
PRIOR ART

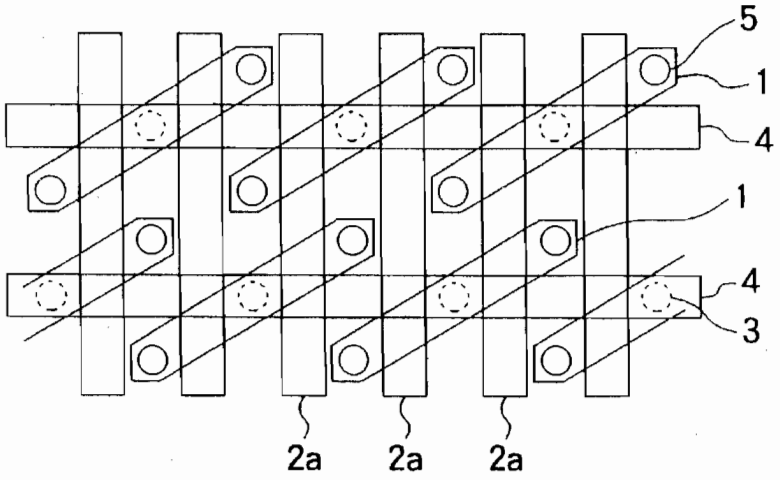


FIG. 2
PRIOR ART

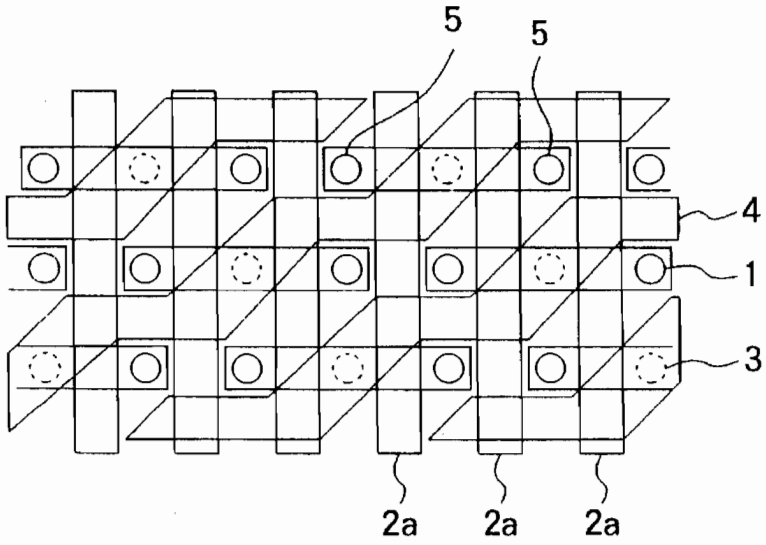


FIG. 3
PRIOR ART

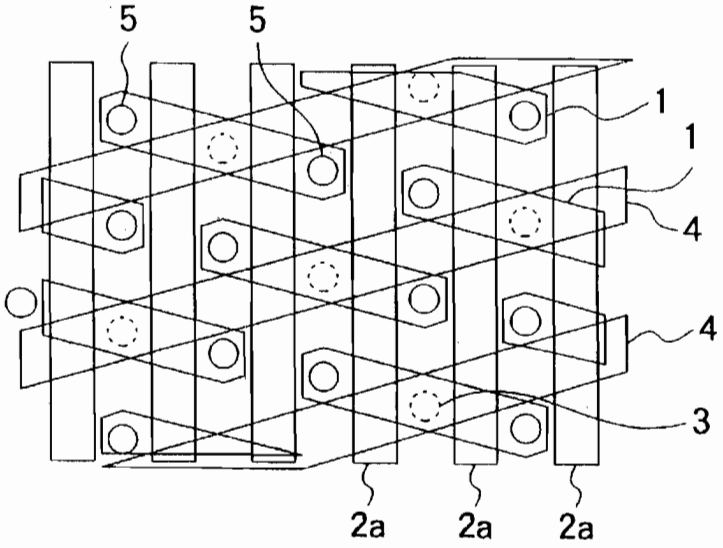


FIG. 4
PRIOR ART

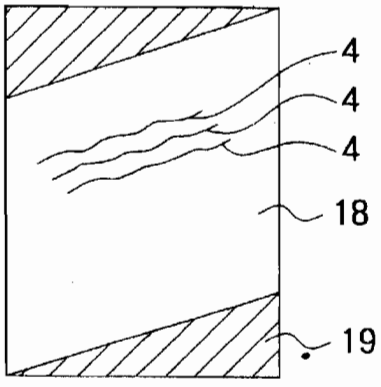


FIG. 5
PRIOR ART

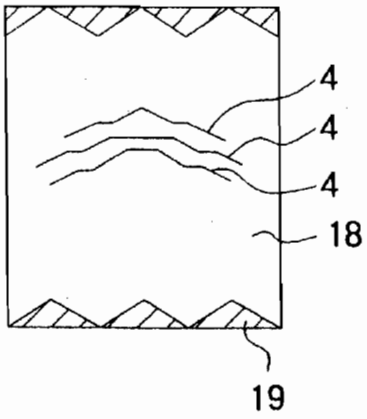


FIG. 6A
PRIOR ART

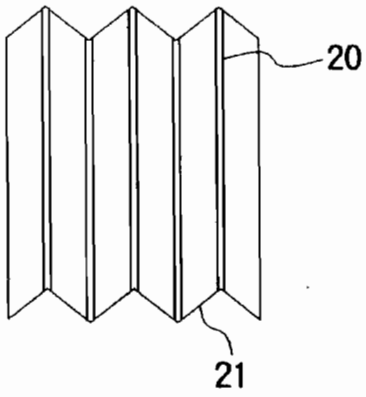


FIG. 6B
PRIOR ART

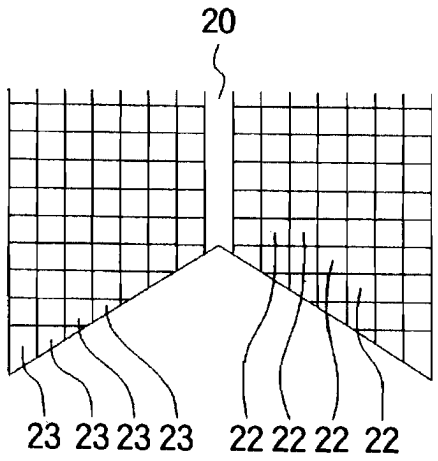


FIG. 7
PRIOR ART

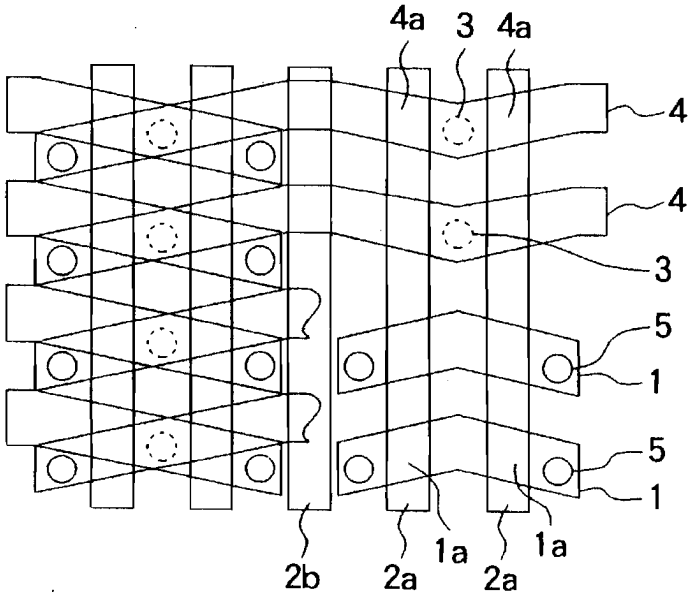


FIG. 8

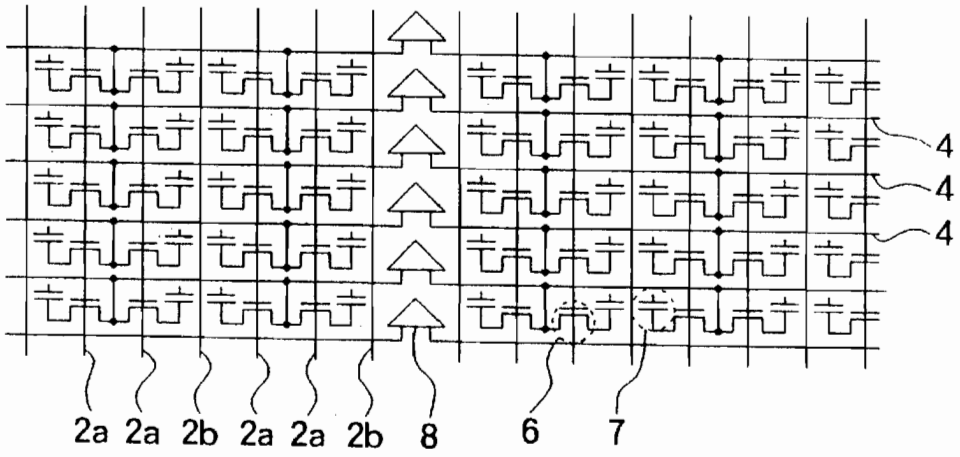


FIG. 9

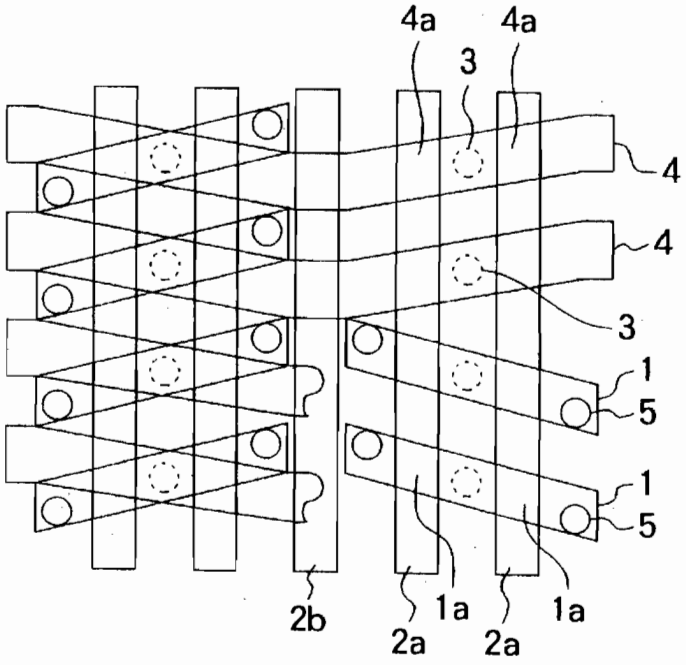


FIG. 10

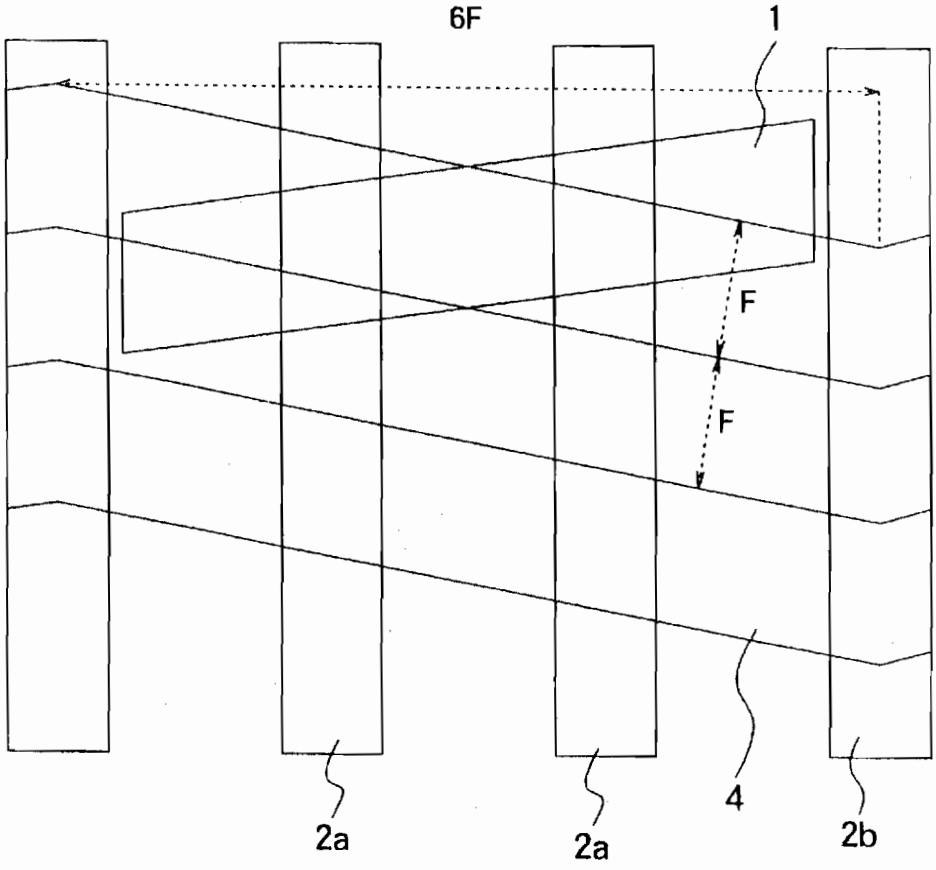


FIG. 11

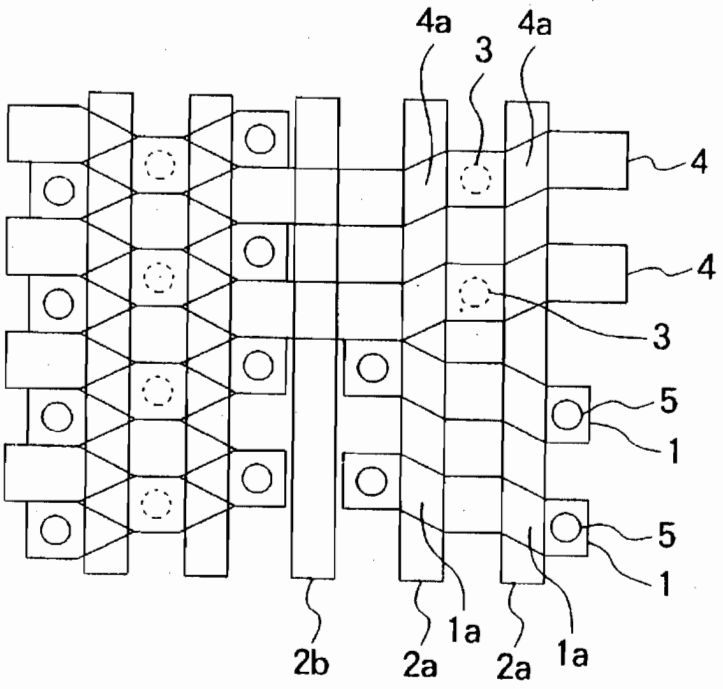


FIG. 12

SEMICONDUCTOR MEMORY DEVICE CAPABLE OF REALIZING A MINIMUM MEMORY CELL AREA APPROXIMATE TO A THEORETICAL VALUE

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a semiconductor memory device and, in particular, to an arrangement of memory cells in a dynamic random access memory (DRAM).

With development of DRAM memory cells of finer structure, a sufficient capacitor storage capacity becomes difficult to obtain. In this connection, use has widely been made of a COB (Capacitor Over Bit-line) structure in which the capacitor is formed at an uppermost portion of a cell structure. This is because total surface area of a capacitor storage electrode can be increased with the above-mentioned structure.

However, conventional DRAM's of the COB structure have various problems which will later be described.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a semiconductor memory device having memory cells of an open-bit-line COB structure, which is capable of realizing a minimum memory cell area approximate to a theoretical value.

Other objects of this invention will become clear as the description proceeds.

According to this invention, there is provided a semiconductor memory device comprising: a semiconductor substrate; device active regions separately formed on the semiconductor substrate; a memory cell array comprising a matrix of memory cell pairs, each pair of the memory cell pairs being formed on each of the device active regions and comprising a pair of memory cells, each of which comprises a charge-storage capacitor and a selection MOS transistor having a gate region and first and second regions, the first region being a predetermined one of a source region and a drain region, the second region being a remaining one of the source and the drain regions that is connected to the charge-storage capacitor; word lines connected to the gate regions of the selection MOS transistors of the memory cells and arranged in parallel to each other on the semiconductor substrate; and bit lines connected to the first regions of the selection MOS transistors of the memory cells. Each of the device active regions has first oblique intersection portions which obliquely intersect adjacent two of the word lines in first oblique directions with a distance left between each of the device active regions and the adjacent two of the word lines. Each of the bit lines has second oblique intersection portions which obliquely intersect the adjacent two of the word lines in second oblique directions reverse with respect to the first oblique directions with another distance left between each of the bit lines and the adjacent two of the word lines.

BRIEF DESCRIPTION OF THE DRAWING

FIGS. **1**A through **1**H are sectional views for describing a process of manufacturing a DRAM of a typical COB structure;

FIG. **2** is a plan view of a memory cell arrangement of a conventional semiconductor memory device;

FIG. **3** is a plan view of a memory cell arrangement of another conventional semiconductor memory device;

FIG. **4** is a plan view of a memory cell arrangement of still another conventional semiconductor memory device;

FIG. **5**. shows a whole memory cell region in the conventional semiconductor memory device illustrated in FIGS. **3** or **4**;

FIGS. **6**A and **6**B show the whole memory cell region of the conventional semiconductor memory device illustrated in FIGS. **3** or **4**;

FIG. **7** is an enlarged view of a corner portion in the whole memory cell region illustrated in FIGS. **6**A and **6**B;

FIG. **8** is a plan view of a memory cell arrangement of a semiconductor memory device according to a first embodiment of this invention;

FIG. **9** is a circuit diagram of an equivalent circuit of an open-bit-line type in the first embodiment of this invention;

FIG. **10** is a plan view of a memory cell arrangement of a semiconductor memory device according to a second embodiment of this invention;

FIG. **11** is a plan view for describing an arrangement where a memory cell size is minimized in this invention; and

FIG. **12** is a plan view of a memory cell arrangement of a semiconductor memory device according to a third embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIGS. **1**A through **1**H, description will first be made as regards a process of manufacturing a DRAM having a COB structure for a better understanding of this invention,

FIGS. **1**A through **1**H are sectional views for describing a process of manufacturing a DRAM having a COB structure. At first referring to FIG. **1**A, a field oxide film **10** is formed on a P^--type semiconductor substrate **9** by typical local oxidation of silicon (LOCOS) or the like. A gate oxide film **11** is formed on a device active region **1** bounded by the field oxide film **10**. Thereafter, a conductor film such as a polysilicon film or a tungsten silicide film Is grown on an overall surface to a thickness on the order of 200 nm and then patterned into a predetermined shape to form a word line **2***a* which serves as a gate region. An impurity is doped into the substrate in the device active region **1** to form a source region **101** and a drain region **102**. Then, a first interlayer insulator film **12** such as a silicon oxide film containing an impurity such as phosphorus or boron is grown on an overall surface to a thickness on the order of 300 nm.

Next, as illustrated in FIG. **1**B, an aperture **3** is formed by typical photolithography and etching. The aperture **3** serves to connect the source region of the device active region **1** and a bit line (later illustrated).

As illustrated in FIG. **1**C, a polysilicon film containing an impurity such as phosphorus is grown on an overall surface to a thickness on the order of 600 nm and etched back to form a first buried conductor layer **13** in the aperture **3** as a contact layer.

As illustrated in FIG. **1**D, a conductor layer such as a tungsten silicide film is grown on an overall surface to a thickness on the order of 150 nm and patterned into a predetermined shape to form the bit line **4**.

As illustrated in FIG. **1**E, a second interlayer insulator film **14** such as a silicon oxide film containing an impurity such as phosphorus or boron is grown on an overall surface to a thickness on the order of 300 nm.

As illustrated in FIG. 1F, an aperture **5** is formed by the typical photolithography and etching. The aperture **5** serves to connect the device active region **1** and a storage node electrode **11'** which will later be formed .

As illustrated in FIG. 1G, a polysilicon film containing an impurity such as phosphorus is grown on an overall surface to a thickness on the order of 600 nm and then patterned into a predetermined shape to form the storage node electrode **11'**. If the storage node electrode **11'** has a three-dimensional structure such as a fin shape or a cylindrical shape, the storage capacity of the capacitor can further be increased.

As illustrated in FIG. 1H, a capacitor insulator film **16** such as a silicon nitride film is grown on an overall surface to a thickness on the order of 6 nm. A polysilicon film containing an impurity such as phosphorus is grown on an overall surface to a thickness on the order of 150 nm and patterned into a predetermined shape to form a plate electrode **17**. Thus, a DRAM memory cell is completed.

In FIGS. 1A through 1H, a single memory cell is formed on each device active region **1** bounded by the field oxide film **10** for brevity of description and illustration. This single memory cell comprises a charge-storage capacitor (**16** and **17**) and a selection MOS transistor (**101, 102, 11**, and **2***a*). In the following description, description will be made as regards a case where a pair of the memory cells are formed on each device active region **1** as a memory cell pair.

In the COB structure described above, the aperture **5** connecting the node electrode **11'** and the device active region **1** is formed above the bit line **4** after the bit line **4** is formed. Accordingly, the aperture **5** must be formed in a manner that the aperture **5** can avoid the word line **2***a* and the bit line **4** already formed.

In the meanwhile, arrangement of the DRAM memory cells is carried out in various manners mainly classified into a folded-bit-line type and an open-bit-line type. The difference therebetween resides in whether two bit lines connected to a sense amplifier is arranged on one side or opposite sides. It is assumed that each layer within the cell has a minimum size F in line width and in line interval. In this event, a theoretical minimum memory cell area is equal to $6F^2$ for the open-bit-line type. In case of an open-bit-line cell, however, a skillful technique is required in order to form the aperture **5** at a position avoiding each conductor line. Specifically, such technique includes oblique arrangement of any layer and formation of a diffusion layer in a convex shape. FIG. **2** shows one approach (see T. Eimori et al, IEDM Tech. Dig., p611, 1993) in which the device active regions **1** are obliquely arranged with respect to the word lines **2***a* and the bit lines **4**. However, because the device active regions **1** are obliquely arranged, even a minimum memory cell area is considerably greater than the theoretical value in order to satisfy that the line width and the line interval are equal to F at minimum. Specifically, the area is on the order of about $7F^2$ with the word lines at about 2F pitch and the bit line side at about 3.5 pitch.

On the other hand, as one approach to achieve a very small cell area, it is proposed to arrange the bit lines **4** in an oblique direction with respect to the word lines **2***a*, as illustrated in FIG. **3** (see K. Shibahara et al., IEDM Tech. Dig., 1994, p639) and FIG. **4** (see Japanese Unexamined Patent Publication No. 279055/1992). In case of FIG. **3**, it is possible to arrange the memory cells so that the memory cell area is equal to $6F^2$. It is noted here that, in case of FIGS. **3** and **4**, the memory cell region **18** has a parallelogramic shape as a whole as illustrated in FIG. **5** because the bit lines **4** are oblique. As a result, an area loss **19** is formed over and under the memory cell region **18**. In order to minimize the area loss **19**, proposal has been made of a folded structure illustrated in FIGS. **6A** and **6B**. The folded structure is realized by dividing a cell array into double mini-arrays symmetrical with respect to a direction of the word lines and connecting them through a connecting portion. In case of an oblique-bit-line cell, the minimum cell size is on the order of about $6.3F^2$ including the above-mentioned area loss **19**.

A first problem of the conventional technique is frequent occurrence of pattern defect upon the photolithography in case of the oblique-bit-line cells as shown in FIGS. **3** and **4**. Specifically, as illustrated in FIGS. **6A** and **6B**, the memory cell region **18** includes bit line folding portions **20** where the memory cells are discontinuous, and corner portions **21** around which a greater part is vacant without any cell arranged therein. In case of the photolithography using light beam exposure, those portions with a discontinuity of the memory cells or with a few cells therearound are susceptible to a pattern defect that a pattern is thickened or thinned as compared with the remaining portions. In a DRAM of 1 G, 4 G, or a greater scale, it is expected that the light beam exposure encounters the limit and electron beam exposure is used instead. In the current status, the electron beam exposure is carried out by a combination of a simultaneous block exposure portion **22** and a variable shape exposure portion **23**. The simultaneous block exposure is a technique of carrying out exposure by irradiation of an electron beam over a particular mask in the manner similar to normal light beam exposure. Currently, such mask has a size including no more than several cell regions. On the other hand, the variable shape exposure is a technique of direct writing by the electron beam in accordance with predetermined data. In case of the oblique-open-bit-line cell, the memory cell region inevitably has the corner portions **21**. The corner portions **21** must be exposed by the use of the variable shape exposure. In this event, misalignment or dimensional error is often caused to occur at a boundary between the simultaneous block exposure portion **22** and the variable shape exposure portion **23**.

A second problem of the conventional technique is an increase in cell area in case of the cell having the oblique diffusion layer as shown in FIG. **2**. Specifically, the pattern defect described above is difficult to occur in the memory cell region having a rectangular shape because the memory cells are continuously formed to the end of the cell regions However, in order to make a whole of the memory cell region have a normal rectangular shape, the memory cell in the conventional technique has a shape illustrated in FIG. **2**. Thus, although the memory cell region has a rectangular shape as a whole, even the minimum memory cell area is equal to $7F^2$ which is much greater than the theoretical value.

This invention provides a semiconductor memory device having memory cells of an open-bit-line COB structure, which is capable of avoiding pattern defect upon photolithography.

This invention also provides a semiconductor memory device having open-bit-line memory cells as small as $6.1F^2$ at minimum, which is approximate to a theoretical value of $6F^2$.

Now, description will be made as regards a few embodiments of this invention with reference to the drawing.

FIG. **6** is a plan view of a memory cell arrangement of a semiconductor memory device according to a first embodiment of this invention. For convenience of illustration, device active regions **1** are omitted in a right upper portion

in FIG. **8** while bit lines **4** are excluded in a right lower portion. In order to help distinguishment between layers, word lines **2***a* and dummy word lines **2***b* in FIG. **1** are written with a line width slightly small and with a line interval slightly great although the line width and the line interval are both equal to a minimum size F. The memory cell arrangement according to this embodiment includes a portion where the device active regions **1** and the bit lines **4** intersect with the word lines **2***a* and the dummy word lines **2***b* in oblique directions reverse from each other. The oblique directions are alternately reversed at every single cell. In FIG. **8**, the line width and the line interval of the device active regions **1** and the bit lines **4** are illustrated as being slightly great although they are equal to the minimum size F. Theoretically, the cell area can be made smaller than that seen from the figure. Every third one of the all word lines is the dummy word line **2***b*. The dummy word lines **2***b* are adapted, for example, to the case where an aperture portion **5** connecting a node electrode and each device active region is formed by self-matching. However, the dummy word lines **2***b* do not serve as word lines of a cell transistor and can therefore be omitted for the purpose of transistor operation. An equivalent circuit for the above-mentioned open-bit-line memory cell is illustrated in FIG. **9**. It is understood from the figure that the dummy word lines **2***b* are irrelevant to reading operation of memory cell data.

FIG. **10** is a plan view of a memory cell arrangement of a semiconductor memory device according to a second embodiment of this invention. Like in FIG. **8**, the device active regions **1** and the bit lines **4** extend in oblique directions reverse from each other. The oblique directions are alternately reversed at every two cells. Consideration will be made as regards the angle of such oblique lines in FIGS. **8** and **10**. The cell area is minimized when the device active regions **1** and the bit lines **4** are reversely oblique at the same angle. Particularly, an extreme minimum is obtained with an arrangement illustrated in FIG. **11**. Specifically, the bit lines **4** are reversely oblique at every 6F where F represents the minimum size. In this event, the minimum cell area is equal to about $6.085F^2$ where the line widths and the line intervals of the device active regions **1**, all of the word lines **2***a* and **2***b*, and the bit lines **4** satisfy the minimum size F.

FIG. **12** is a plan view of a memory cell arrangement of a semiconductor memory device according to a third embodiment of this invention. In this case, the device active regions **1** and the bit lines **4** are oblique to all of the word lines **2***a* and **2***b* in restricted portions in the vicinity of the word lines. The remaining portions are formed by straight lines perpendicular to the word lines. In the above-mentioned arrangement, the most part of the area to be provided with the aperture portions **3** and **5** correspond to such straight line portions where all of the word lines **2***a* and **2***b* and the bit lines **4** perpendicularly intersect with each other. Accordingly, the above-mentioned memory cell arrangement is adapted to the case where the apertures are formed by self-matching.

Summarizing FIGS. **8** and **9**, the semiconductor memory device according to the first embodiment of this invention comprises device active regions **1** (FIG. **8**) and a memory cell array illustrated in FIG. **9**. The device active regions **1** are separately formed on a semiconductor substrate **9** (FIG. **1A**).

In FIG. **9**, the memory cell array comprises a matrix of memory cell pairs. Each pair of the memory cell pairs is formed on each of the device active regions **1** and comprises a pair of memory cells. Each of the memory cells comprises a charge-storage capacitor **7** and a selection MOS transistor **6** which has a gate region and first and second regions. The first region is a predetermined one of source and drain regions **101** and **102** (FIG. **1A**). The second region is a remaining one of the source and the drain regions **101** and **102** that is connected to the charge-storage capacitor **7**. Word lines **2***a* are connected to the gate regions of the selection MOS transistors **6** of the memory cells. Bit lines **4** are connected to the first regions of the selection MOS transistors **6** of the memory cells.

In FIG. **8**, the word lines **2***a* are arranged in parallel to each other on the semiconductor substrate **9**. Each of the device active regions **1** has first oblique intersection portions **1***a* which obliquely intersect adjacent two of the word lines **2***a* in first oblique directions with a distance left between each of the device active regions **1** and each of the adjacent two of the word lines **2**.

Each of the bit lines **4** has second oblique intersection portions **4***a* which obliquely intersect the adjacent two of the word lines **2***a* in second oblique directions reverse with respect to the first oblique directions with another distance left between each of the bit lines **4** and each of the adjacent two of the word lines **2***a*.

The first oblique directions of the first oblique intersection portions **1***a* of each of the device active regions **1** are reversed at every memory cell. The second oblique directions of the second oblique intersection portions **4***a* of each of the bit lines **4** are reversed at every memory cell.

One of the first oblique intersection portions **1***a* of each of the device active regions **1** obliquely intersects one of the adjacent two of the word lines **2***a* at a predetermined angle with respect to the above-mentioned one of the adjacent two of the word lines **2***a* in a counterclockwise direction, A remaining one of the first oblique intersection portions **1***a* of each of the device active regions **1** obliquely intersects a remaining one of the adjacent two of the word lines **2***a* at the predetermined angle with respect to the remaining one of the adjacent two of the word lines **2***a* in a clockwise direction.

One of the second oblique intersection portions **4***a* of each of the bit lines **4** obliquely intersects the above-mentioned one of the adjacent two of the word lines **2***a* at the predetermined angle with respect to the above-mentioned one of the adjacent two of the word lines **2***a* in the clockwise direction. A remaining one of the second oblique intersection portions **4***a* of each of the bit lines **4** obliquely intersects the remaining one of the adjacent two of the word lines **2***a* at the predetermined angle with respect to the remaining one of the adjacent two of the word lines **2***a* in the counterclockwise direction.

Summarizing FIGS. **10** and **12**, each of the semiconductor memory devices according to the second and the third embodiments of this invention is similar to the semiconductor memory device according to the first embodiment of this invention except that the first oblique directions of the first oblique intersection portions **1***a* of adjacent two of the device active regions **1** adjacent to each other in a transverse direction of the word line **2***a* are reversed at every memory cell pair (namely, two memory cells) and that the second oblique directions of the second oblique intersection portions **4***a* of each of the bit lines **4** are reversed at every memory cell pair.

One of the first oblique intersection portions **1***a* of each of the device active regions **1** obliquely intersects one of the adjacent two of the word lines **2***a* at a predetermined angle with respect to the above-mentioned one of the adjacent two of the word lines **2***a* in a counterclockwise direction. A

remaining one of the first oblique intersection portions 1*a* of each of the device active regions **1** obliquely intersects a remaining one of the adjacent two of the word lines **2***a* at the predetermined angle with respect to the remaining one of the adjacent two of the word lines **2***a* in the counter-clockwise direction.

One of the second oblique intersection portions **4***a* of each of the bit lines **4** obliquely intersects the above-mentioned one of the adjacent two of the word lines **2***a* at the predetermined angle with respect to the above-mentioned one of the adjacent two of the word lines **2***a* in the clockwise direction. A remaining one of the second oblique intersection portions **4***a* of each of the bit lines **4** obliquely intersects the remaining one of the adjacent two of the word lines **2***a* at the predetermined angle with respect to the remaining one of the adjacent two of the word lines **2***a* in the clockwise direction.

In the manner illustrated in FIGS. **1A** through **1H** by reference numerals **16** and **17**, the charge-storage capacitor **7** of each of the memory cells may be formed farther from the semiconductor substrate **9** than the word and the bit lines **2***a* and **4**.

As a first merit of this invention, it is possible to realize the small memory cell area on the order of about $6.1F^2$ at minimum, which is approximate to the theoretical value of $6F^2$. The reason is as follows. According to this invention, the memory cell arrangement includes the portion where the device active regions and the bit lines are reversely oblique to the word lines. Therefore, as compared with the case where the diffusion layer alone is oblique, the angles of these oblique lines can be nearly equal to the right angle with respect to the word lines.

As a second merit of this invention, it is possible in case of the light beam exposure to prevent the pattern defect from occurring upon the photolithography at the portions where the memory cells are discontinuous and where the surrounding cells are small in number. In case of the electron beam exposure, misalignment or dimensional error is avoided at the boundary between the simultaneous block exposure portion and the variable shape exposure portion. The reason is as follows. According to this invention, the bit lines are formed by a series of the oblique portions which are alternately reversely oblique to the word lines. Therefore, it is possible to arrange a whole of the memory cell region in a continuous fashion and in a rectangular shape.

What is claimed is:

1. A semiconductor memory device comprising:

a semiconductor substrate;

device active regions separately formed on semiconductor substrate;

a memory cell array comprising a matrix of memory cell pairs, each pair of said memory cell pair being formed on each of said device active regions and comprising a pair of memory cells, each of which comprises a charge-storage capacitor and a selection MOS transistor having a gate region and first and second regions, said first region being a predetermined one of a source region and a drain region, said second region being a remaining one of said source and said drain regions that is connected to said charge-storage capacitor;

word lines connected to said gate regions of the selection MOS transistors of said memory cells and arranged in parallel to each other on said semiconductor substrate; and

bit lines connected to said first regions of the selection MOS transistors of said memory cells;

each of said device active regions having first oblique intersection portions which obliquely intersect adjacent two of said word lines in first oblique directions with a distance left between each of said device active regions and each of said adjacent two of the word lines;

each of said bit lines having second oblique intersection portions which obliquely intersect said adjacent two of the word lines in second oblique directions reverse with respect to said first oblique directions with another distance left between each of said bit lines and each of said adjacent two of the word lines;

said first oblique direction of the first oblique intersection portion of each of said device active regions being reversed at every memory cell; and

said second oblique directions of the second oblique intersection portions of each of said bit lines being reversed at every memory cell.

2. A semiconductor memory device as claimed in claim **1**, wherein:

one of the first oblique intersection portions of each of said device active regions obliquely intersects one of said adjacent two of the word lines at a predetermined angle with respect to said one of the adjacent two of said word lines in a counterclockwise direction, a remaining one of the first oblique intersection portions of each of said device active regions obliquely intersecting a remaining one of said adjacent two of the word lines at said predetermined angle with respect to said remaining one of the adjacent two of said word lines in a clockwise direction;

one of the second oblique intersection portions of each of said bit lines obliquely intersecting said one of the adjacent two of said word lines at said predetermined angle with respect to said one of the adjacent two of said word lines in said clockwise direction, a remaining one of the second oblique intersection portions of each of said bit lines obliquely intersecting said remaining one of the adjacent two of said word lines at said predetermined angle with respect to said remaining one of the adjacent two of said word lines in said counterclockwise direction.

3. A semiconductor memory device comprising:

a semiconductor substrate;

device active regions separately formed on said semiconductor substrate;

a memory cell array comprising a matrix of memory cell pairs, each pair of said memory cell pairs being formed on each of said device active regions and comprising a pair of memory cells, each of which comprises a charge-storage capacitor and a selection MOS transistor having a gate region and first and second regions, said first region being a predetermined one of a source region and a drain region, said second region being a remaining one of said source and said drain regions that is connected to said charge-storage capacitor;

word lines connected to said gate regions of the selection MOS transistors of said memory cells and arranged in parallel to each other on said semiconductor substrate; and

bit lines connected to said first regions of the selection MOS transistors of said memory cells;

each of said device active regions having first oblique intersection portions which obliquely intersect adjacent

two of said word lines in first oblique directions with a distance left between each of said device active regions and each of said adjacent two of the word lines;

each of said bit lines having second oblique intersection portions which obliquely intersect said adjacent two of the word lines in second oblique directions reverse with respect to said first oblique directions with another distance left between each of said bit lines and each of said adjacent two of the word lines;

said first oblique directions of the first oblique intersection portions of adjacent two of said device active regions adjacent in a transverse direction of said word lines being reversed at every memory cell pair; and

said second oblique directions of the second oblique intersection portions of each of said bit lines being reversed at every memory cell pair.

4. A semiconductor memory device as claimed in claim **1**, wherein the charge-storage capacitor of each of said memory cells is formed farther from said semiconductor substrate than said word and said bit lines.

5. A semiconductor memory device as claimed in claim **3**, wherein the charge-storage capacitor of each of said memory cells is formed farther from said semiconductor substrate than said word and bit lines.

* * * * *

Exhibit 2

US006894363B2

(12) **United States Patent**
Tamura

(10) **Patent No.: US 6,894,363 B2**
(45) **Date of Patent: May 17, 2005**

(54) **SEMICONDUCTOR DEVICE USING SHALLOW TRENCH ISOLATION AND METHOD OF FABRICATING THE SAME**

(75) Inventor: **Kazuhiro Tamura**, Tokyo (JP)

(73) Assignee: **Elpida Memory, Inc.** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/260,484**

(22) Filed: **Sep. 30, 2002**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Oct. 9, 2001 (JP) 2001/312034

(51) **Int. Cl.**[7] **H01L 29/00**

(52) **U.S. Cl.** **257/510**; 257/506; 257/508; 438/424; 438/435; 438/439

(58) **Field of Search** 257/510, 506, 257/508; 438/424, 435, 439

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Primary Examiner—Nathan J. Flynn
Assistant Examiner—Remmon R. Fordé
(74) *Attorney, Agent, or Firm*—Hayes Soloway P.C.

(57) **ABSTRACT**

A semiconductor device adopting shallow trench isolation for reducing an internal stress of a semiconductor substrate. The semiconductor device is composed of a semiconductor substrate provided with a trench for isolation, and an insulating film formed to cover the trench for relaxing an internal stress of the semiconductor substrate. The insulating film includes a first portion disposed to be opposed to a bottom of the trench, and a second portion disposed to be opposed to a side of the trench. A first thickness of the first portion is different from a second thickness of the second portion.

10 Claims, 8 Drawing Sheets

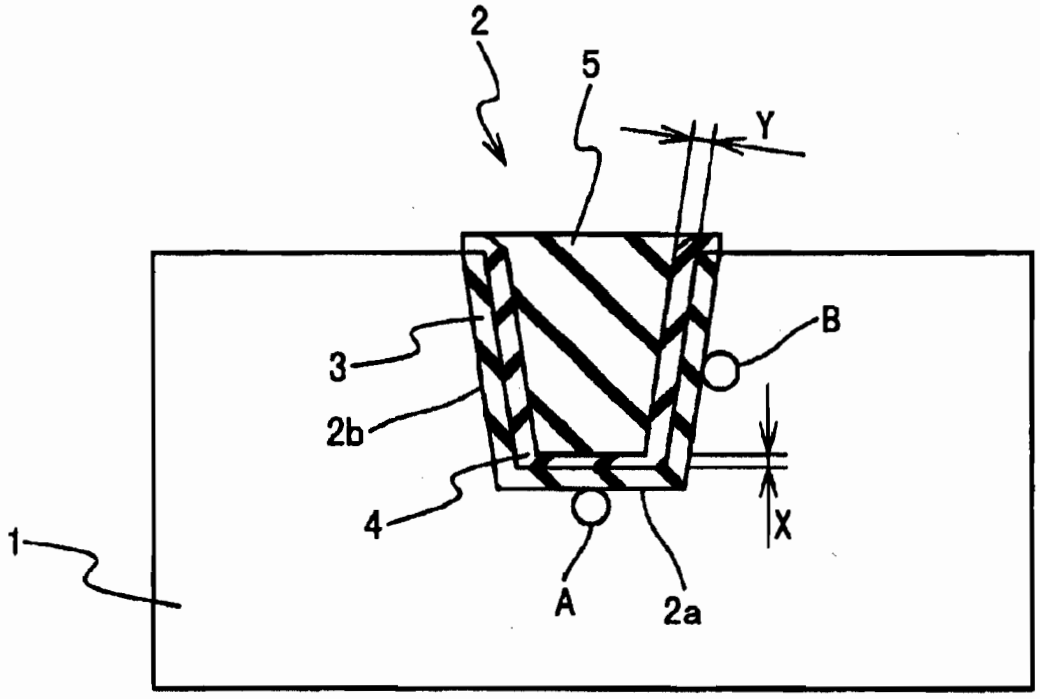


Fig. 1 PRIOR ART

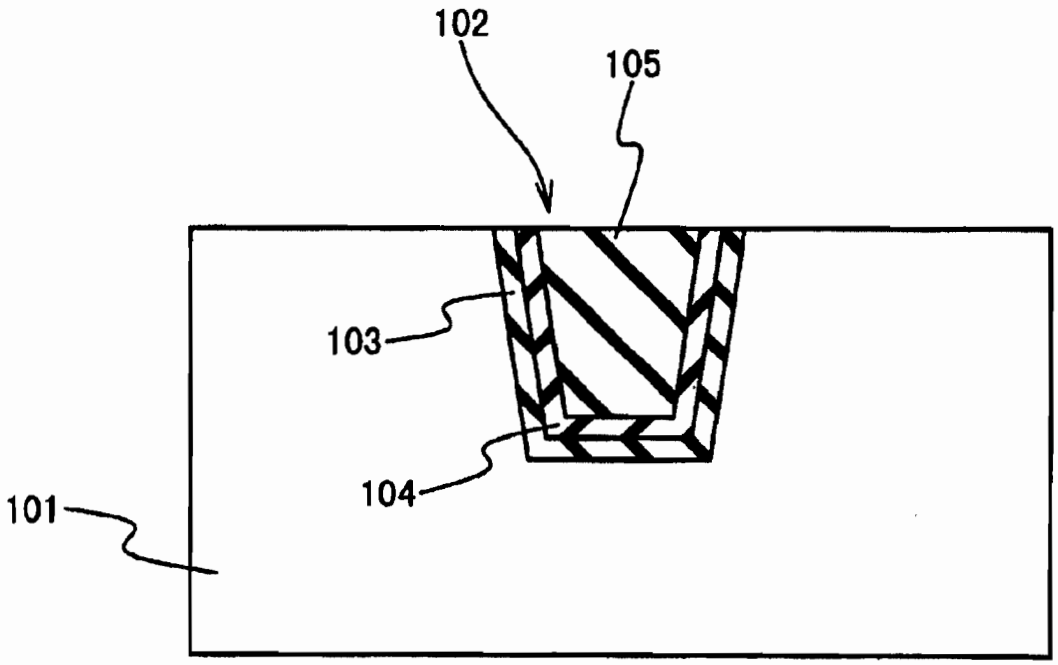


Fig. 2

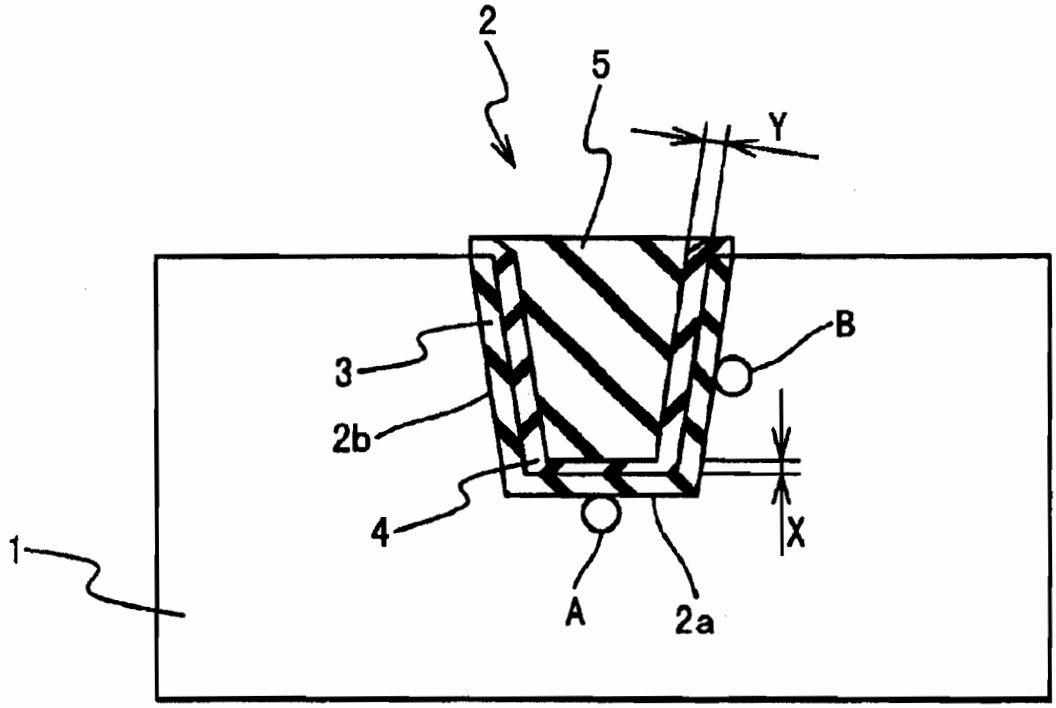


Fig. 3

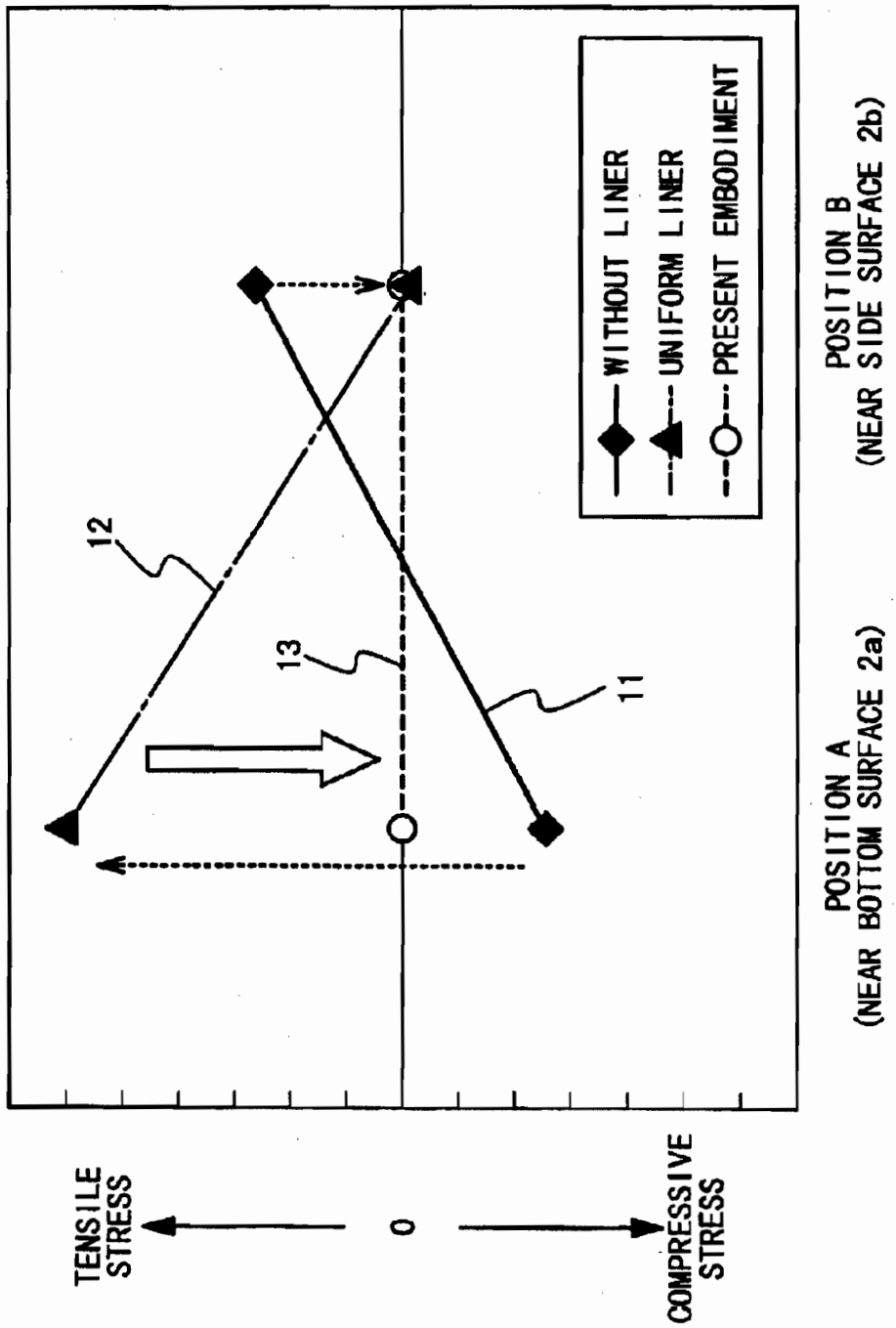

WITHOUT LINER
UNIFORM LINER
PRESENT EMBODIMENT
12
13
11
TENSILE STRESS
0
COMPRESSIVE STRESS
POSITION A
(NEAR BOTTOM SURFACE 2a)
POSITION B
(NEAR SIDE SURFACE 2b)

Fig. 4

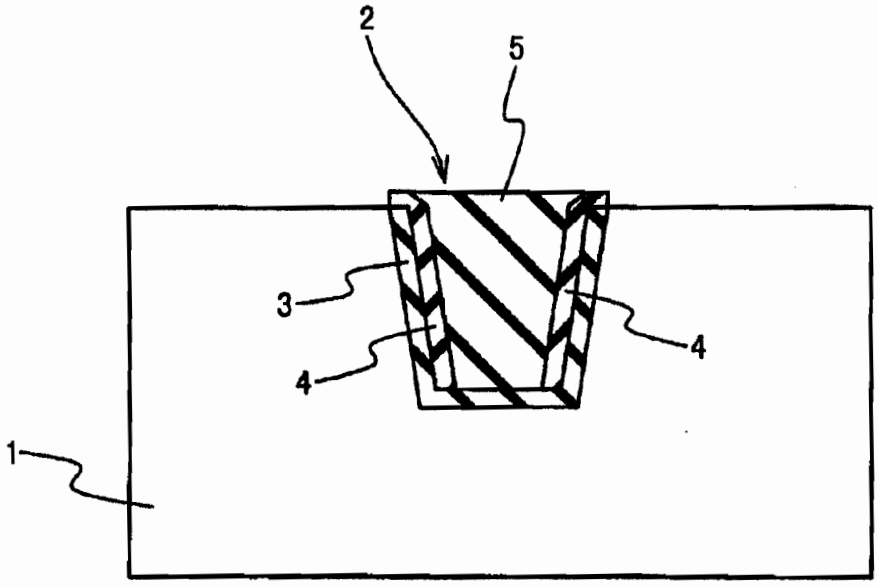


Fig. 5

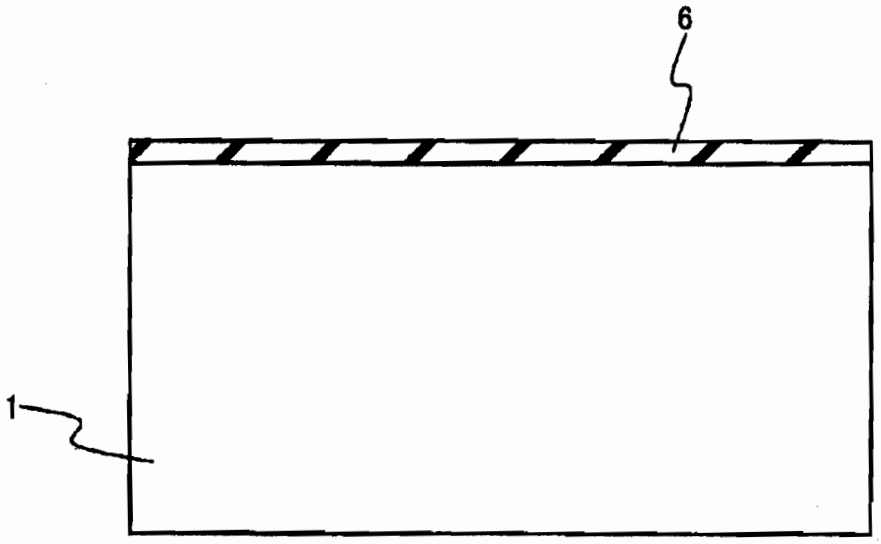


Fig. 6

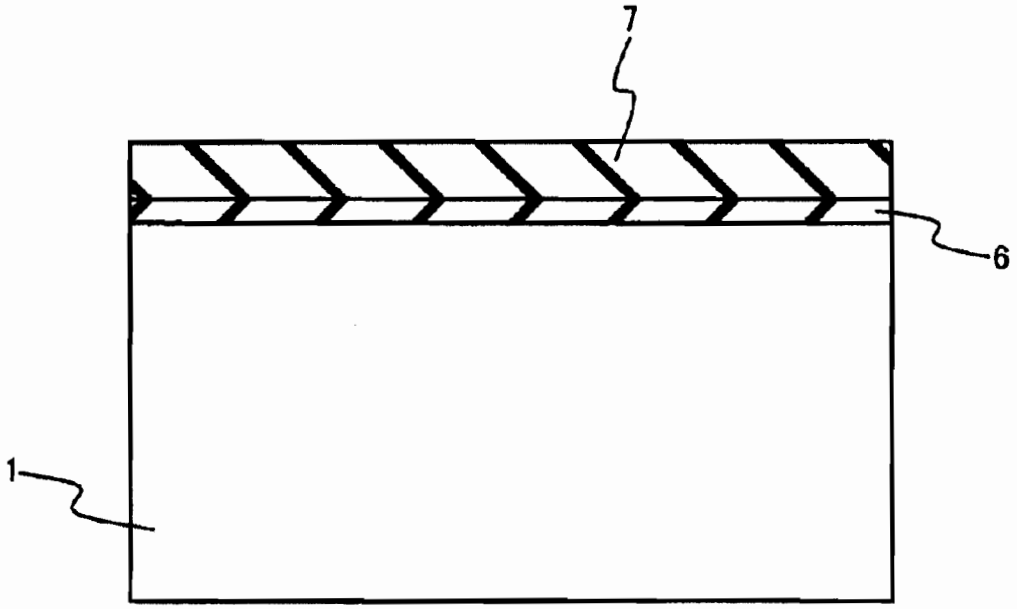


Fig. 7

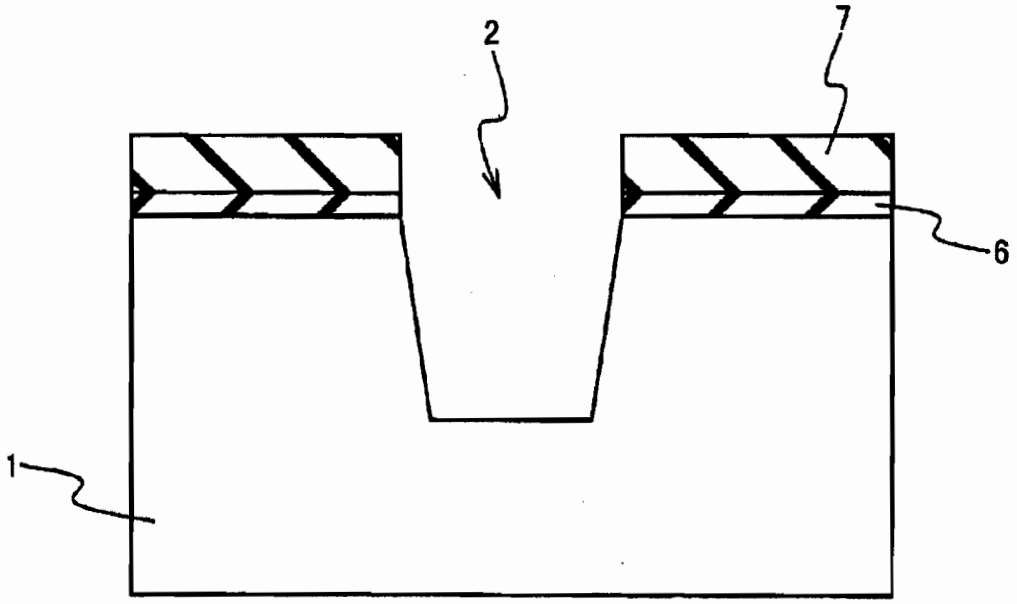


Fig. 8

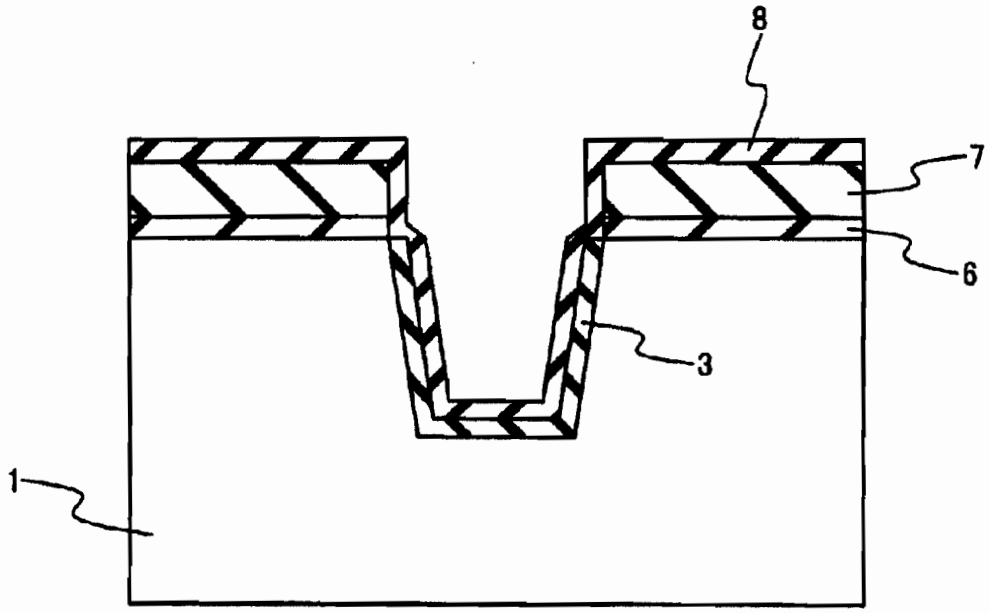


Fig. 9

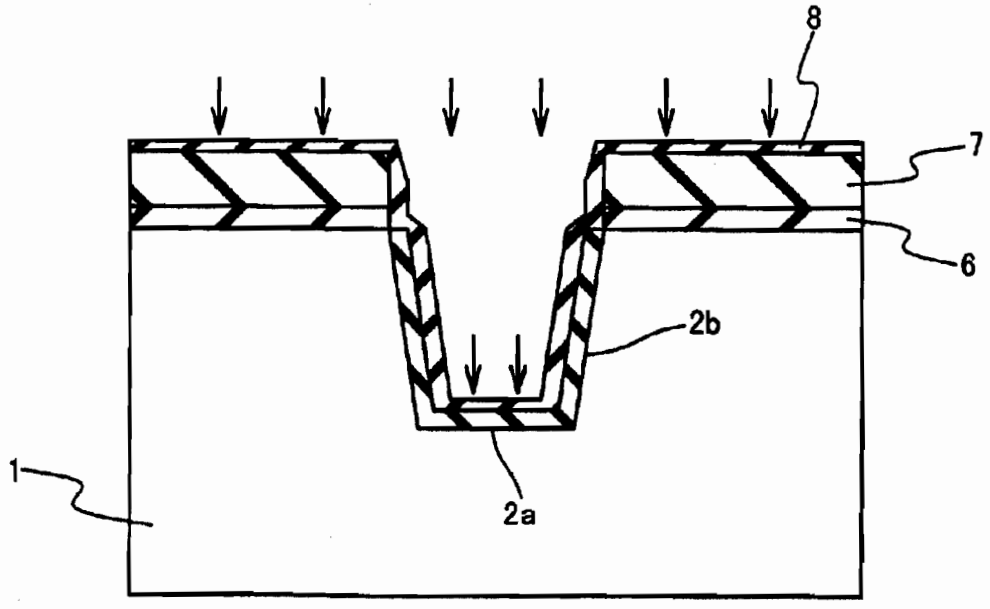


Fig. 10

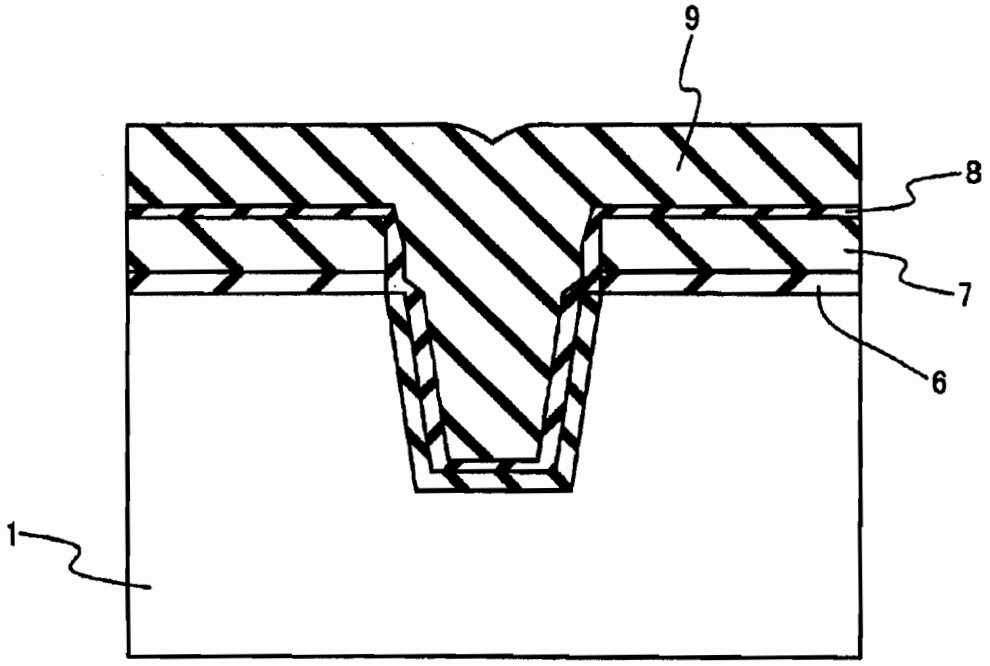


Fig. 11

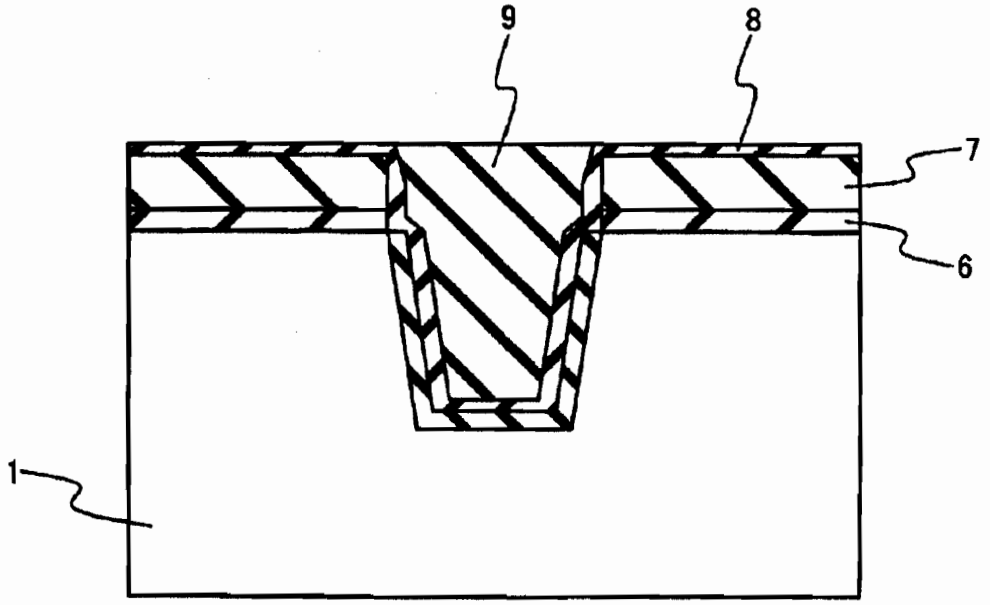
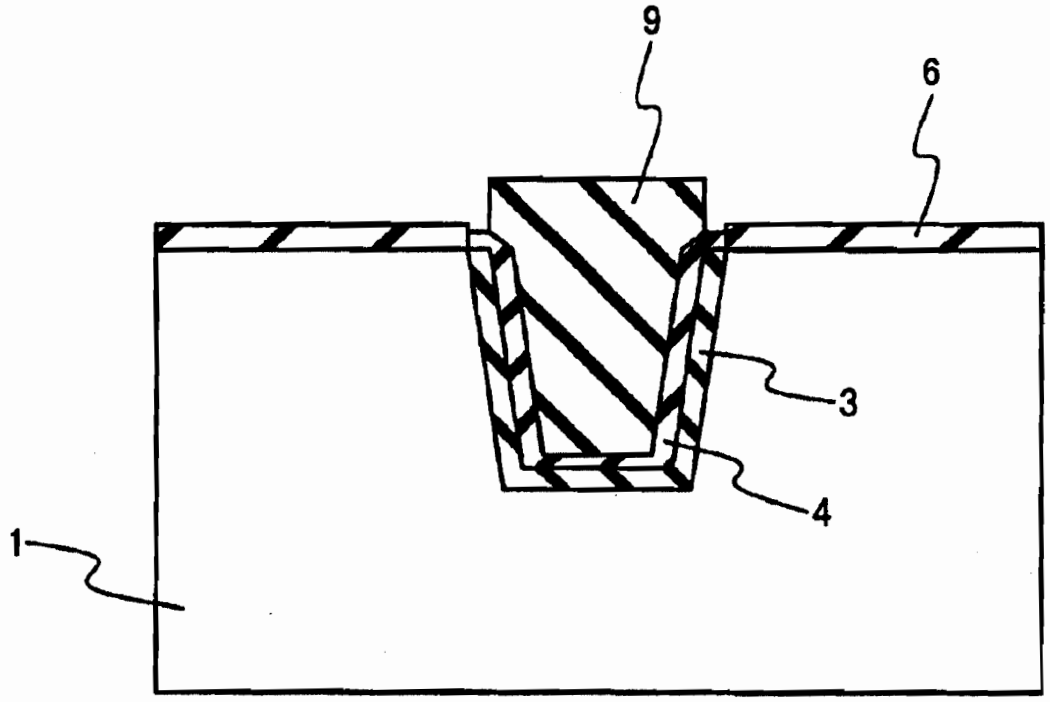


Fig. 12



SEMICONDUCTOR DEVICE USING SHALLOW TRENCH ISOLATION AND METHOD OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and a method of fabricating the same. More particularly, the present invention relates to a semiconductor device using shallow trench isolation.

2. Description of the Related Art

Highly integrated semiconductor devices often adopt shallow trench isolation. Isolation has been conventionally achieved by a LOCOS (Local Oxidation of Silicon) technique. However, the LOCOS technique has difficulties in fabricating highly integrated semiconductor devices, such as bird's beaks and poor isolation abilities. This situation encourages the adoption of the shallow trench isolation.

FIG. **1** shows a conventional structure of a semiconductor devices using shallow trench isolation. A trench **102** is formed on a silicon substrate **101**. The inner surface of the trench **102** is coated by a silicon oxide film **103** formed by thermal oxidization. A liner **104** made of silicon nitride is formed on the silicon oxide film **103**. A silicon oxide film **105** is formed on the liner **104** to fill the trench **102**.

The liner **104** relaxes the interior stress induced in the silicon substrate **101**. The shallow trench isolation causes the interior stress to be applied to the silicon substrate **101**, because of the difference in thermal expansion coefficients between the silicon substrate **101** and the silicon oxide film **105**. The stress applied to the silicon substrate **101** induces crystal defects in the silicon substrate, and thus increases junction leak currents. The increase in the junction leak currents causes improper operations of semiconductor devices. The relaxation of the internal stress by the liner **104** reduces the junction leak current and thus improves the reliability of the semiconductor device.

It is desired that the internal stress of the semiconductor substrate be further reduced. The reduction of the internal stress efficiently improves the reliability of the semiconductor device.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a technique for further reducing the internal stress applied to the semiconductor substrate of the semiconductor device in which the shallow trench isolation is employed.

In an aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, and an insulating film formed to cover the trench for relaxing an internal stress of the semiconductor substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is different from a second thickness of the second portion.

The first thickness of the first portion may be thinner than the second thickness of the second portion.

When the semiconductor device further includes another insulating film in the trench and the other insulating film exerts a compressive stress on the semiconductor substrate, the insulating film preferably exerts a tensile stress on said semiconductor substrate.

The insulating film is preferably formed of one selected from a group consisting of silicon nitride and silicon oxinitride.

In another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, and an insulating film formed to cover the trench for relaxing an internal stress of the semiconductor substrate. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film formed on the silicon oxide film. The insulating film exerts a tensile stress on the semiconductor substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is thinner than a second thickness of the second portion.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film formed on the silicon oxide film. The insulating film exerts a tensile stress on the semiconductor substrate. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film disposed on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is thinner than a second thickness of the second portion.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film disposed on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a method of fabricating a semiconductor device is composed of:

forming a trench for isolation in the semiconductor substrate;

forming an insulating film to cover the trench for relaxing an internal stress of the silicon substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. The first thickness of the first portion is different from a second thickness of the second portion. The first thickness of the first portion may be thinner than the second thickness of the second portion.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming an insulating film to cover the trench for relaxing an internal stress of the silicon substrate, wherein the insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover the trench; and

forming an insulating film on the silicon oxide film, wherein the insulating film exerts a compressive stress on the silicon substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is thinner than a second thickness of the second portion.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover the trench;

forming an insulating film on the silicon oxide film. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover the trench; and

forming an insulating film on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is different from a second thickness of the second portion.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover the trench; and

forming an insulating film on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a conventional semiconductor device adopting shallow trench isolation;

FIG. **2** shows a semiconductor device in an embodiment of the present invention;

FIG. **3** shows internal stresses exerted on a silicon substrate;

FIG. **4** shows a modification of the semiconductor device in the embodiment; and

FIGS. **5** to **12** are section views showing a fabrication process of the semiconductor device in the embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of a semiconductor apparatus according to the present invention and a method of manufacturing the same will be described below with reference to the attached drawings.

In an embodiment of the semiconductor device according to the present invention, as shown in FIG. **2**, a trench **2** is formed on a silicon substrate **1**. An inner surface of the trench **2** is coated by a silicon oxide film **3**. The silicon oxide film **3** is coated by a liner **4**. A silicon oxide film **5** is formed on the liner **4**. The trench **2** is filled with the silicon oxide film **3**, the liner **4** and the silicon oxide film **5**.

The liner **4** is formed of an insulating film that has a compressive internal stress. The silicon oxide films **3**, **5** have the tensile internal stresses, and thus exerts compression stresses on the silicon substrate **1**. The liner **4**, which has a compressive internal stress, exerts a tensile stress on the silicon substrate **1**, and thus relaxes the internal stress of the silicon substrate **1**. The liner **4** is preferably formed of silicon nitride or silicon oxinitride.

The liner **4** includes a bottom portion that is opposed to the bottom surface **2***a* of the trench **2**, and a side portion that is opposed to the side surface **2***b* of the trench **2**. A film thickness X of the bottom portion of the liner **4** is thinner than a film thickness Y of the side portion of the liner **4**. This structure further reduces the internal stress of the silicon substrate **1**. The inventor has discovered that an internal stress of the silicon substrate **1** in the vicinity of the bottom **2***a* of the trench **2** is weaker than that in the vicinity of the side **2***b* of the trench **2**. The difference in the film thicknesses of the bottom and side portions causes the different stresses on the vicinity of the bottom surface **2***a* and side surface **2***b*, and effectively reduces the internal stress of the silicon substrate **1**.

FIG. **3** shows the internal stresses of the silicon substrate **1** at positions A and B indicated by the circles in FIG. **2**. The position A is located near the bottom surface **2***a* of the trench **2**, and the position B is located near the side of the trench **2**. The internal stresses of the silicon substrate **1** are measured by a convergent beam electron diffraction (CBED) method.

Three samples have been fabricated; a first sample has a structure in which the liner **4** is excluded from the structure shown in FIG. **2**, a second sample has a structure in which the liner **4** is conformal or uniform in thickness, and a third sample has the structure shown in FIGS. **2**. A line **11** in FIG. **3** represents the internal stresses of the silicon substrate without the liner **4**. A line **12** represents the internal stresses of the silicon substrate **1** when the liner **4** is uniform in the film thickness. A line **13** represents the internal stresses of the silicon substrate **1** in the semiconductor device having the structure shown in FIG. **2**.

In regard to the case that the film thickness of the liner **4** is uniform, the internal stress of the silicon substrate **1** is weak at the position B as indicated by the line **12**. However, the considerably strong tensile stress is applied to the silicon substrate **1** at the position A, which is located near the bottom plane of the trench **2**. This implies that the uniform liner **4** exerts the excessive tensile stress on the silicon substrate **1** at the position A.

The line **13** implies that the structure in which the film thickness X of the bottom portion of the liner **4** is thinner than the film thickness Y of the side portion remarkably reduces the internal stress of the silicon substrate **1** at the position A. The thinner film thickness of the bottom portion prevents an excessive tensile stress from being exerted on the silicon substrate **1**.

With reference to FIG. **2**, the film thickness X of the bottom portion of the liner **4** is adjusted on the basis of the internal stress applied to the silicon substrate **1**. It should be noted that the adjusted film thickness X of the bottom portion might be zero as shown in FIG. **4**. That is, the liner **4** may be designed such that the liner **4** is not opposed to the bottom surface **2***a* of the trench **2**.

The method of fabricating the semiconductor device shown in FIG. **2** will be described below.

As shown in FIG. **5**, the surface of the silicon substrate **1** is thermally oxidized to thereby form a sacrificed oxide film **6**. A film thickness of the sacrificed oxide film **6** is typically 10 to 20 nm.

A silicon nitride film **7** is then formed on the sacrificed oxide film **6**, as shown in FIG. **6**. A film thickness of the silicon nitride film **7** is typically 100 to 200 nm.

After the formation of the silicon nitride film **7**, as shown in FIG. **7**, the sacrificed oxide film **6** and the silicon nitride film **7** are patterned by an etching technique, which is well known in the art. The silicon substrate **1** is then etched to form the trench **2** by using the patterned sacrificed oxide film **6** and silicon nitride film **7** as a mask.

After the formation of the trench **2**, the inner surface of the trench **2** is thermally oxidized to thereby form the silicon oxide film **3**. A film thickness of the silicon oxide film **3** is typically 10 to 30 nm.

A silicon nitride film **8** is then formed to cover the entire structure as shown in FIG. **8**. The silicon nitride film **8** is exemplarily formed by using an LPCVD (Low Pressure Chemical Vapor Deposition) method. A film thickness of the silicon nitride film **8** is substantially uniform, and is typically 3 to 10 nm. The silicon nitride film **8** is formed in the conditions that the formed silicon nitride film **8** has the compressive internal stress. The other insulation film having a compressive internal stress may be used instead of the silicon nitride film **8**. For example, a silicon oxide nitride film may be formed instead of the silicon nitride film **8**.

After the formation of the silicon nitride film **8**, as shown in FIG. **9**, the silicon nitride film **8** is anisotropically etched in the direction perpendicular to the major surface of the silicon substrate **1**. A bottom portion of the silicon nitride film **8**, which is opposed to the bottom surface **2***a*, is partially removed. This causes the film thickness of the bottom portion of the silicon nitride film **8** to be thinner than that of the side portion opposed to the side **2***b* of the trench **2**. It should be noted that the bottom portion of the silicon nitride film **8** might be totally removed to form the structure shown in FIG. **4**. The etching of the silicon nitride film **8** may be executed by the physical etching such as ion milling or the physical and chemical etching.

A silicon oxide film **9** is then formed to cover the entire structure by using a CVD method as shown in FIG. **10**. The trench **2** is totally filled with the silicon oxide film **9**.

After the formation of the silicon oxide film **9**, as shown in FIG. **11**, a portion of the silicon oxide film **9** outside the trench **2** is removed to expose the surface of the silicon nitride film **8**. The partial removal of the silicon oxide film **9** is achieved by a CMP (Chemical Mechanical Polishing) method. The silicon nitride film **8** and the silicon nitride film **7** function as stoppers during the CMP process.

The silicon substrate **1** is then processed by heated phosphoric acid to remove the silicon nitride film **7** and a portion of the silicon nitride film **8** outside the trench **2** as shown in FIG. **12**. The remaining portion of the silicon nitride film **8** constitutes the liner **4**.

The silicon substrate **1** is then processed by hydrofluoric acid to remove the sacrificed oxide film **6** and a portion of the silicon oxide film **9** outside the trench **2**. The removal of the sacrificed oxide film **6** and the portion of the silicon oxide film **9** completes the formation of the structure shown in FIG. **2** (or, FIG. **4**). MOS transistors and other elements are then formed on the silicon substrate **1** to fabricate an LSI (Large Scale Integrated circuit).

As described, the semiconductor device in this embodiment has the structure in which the film thickness X of the bottom portion of the liner **4** is thinner than the film thickness Y of the side portion, or the film thickness X of the bottom portion is zero. This structure effectively reduces the internal stress of the silicon substrate **1**.

Although the invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form has been changed in the details of construction and the combination and arrangement of parts may be resorted to without departing from the spirit and the scope of the invention as hereinafter claimed.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate provided with a trench for isolation; and

an insulating film formed in a single layer to cover said trench for relaxing an internal stress of said semiconductor substrate, wherein said insulating film includes:

a first portion disposed to be opposed to a bottom of said trench, and

a second portion disposed to be opposed to a side of said trench, and

wherein a first thickness of said first portion is different from a second thickness of said second portion.

2. The semiconductor device according to claim **1**, wherein said first thickness of said first portion is thinner than said second thickness of said second portion.

3. The semiconductor device according to claim **2**, further comprising another insulating film in said trench, wherein said another insulating film exerts a compressive stress on said semiconductor substrate, and

wherein said insulating film exerts a tensile stress on said semiconductor substrate.

4. The semiconductor device according to claim **2**, wherein said insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride.

5. A semiconductor device comprising:

a semiconductor substrate provided with a trench for isolation; and

an insulating film formed in a single layer to cover said trench for relaxing an internal stress of said semiconductor substrate, wherein said insulating film is opposed to a side of said trench bind is not opposed to a bottom of said trench.

6. The semiconductor device according to claim **5**, further comprising another insulating him in said trench, wherein said another insulating film exerts a compressive stress on said semiconductor substrate, and

wherein said insulating film exerts a tensile stress on said semiconductor substrate.

7. The semiconductor device according to claim **5**, wherein said insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride.

8. A semiconductor device comprising:

a semiconductor substrate provided with a trench for isolation;

a silicon oxide film formed to cover said trench; and

an insulating film formed in a single layer on said silicon oxide film, wherein said insulating film exerts a tensile stress on said semiconductor substrate, and

wherein said insulating film includes:

a first portion disposed to be opposed to a bottom of said trench, and

a second portion disposed to be opposed to a side of said trench, and

wherein a first thickness of said first portion is thinner than a second thickness of said second portion.

9. The semiconductor device according to claim **8**, wherein said insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride.

10. A semiconductor device comprising:

a semiconductor substrate provided with a trench for isolation;

a silicon oxide film formed to cover said trench; and

an insulating film disposed in a single layer on said silicon oxide film, wherein said insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride, and

wherein said insulating film includes:

a first portion disposed to be opposed to a bottom of said trench, and

a second portion disposed to the opposed to a side of said trench, and

wherein a first thickness of said first portion is thinner than a second thickness of said second portion.

* * * * *

Exhibit 3

US007060588B2

(12) **United States Patent**
Tamura

(10) **Patent No.: US 7,060,588 B2**
(45) **Date of Patent: Jun. 13, 2006**

(54) **SEMICONDUCTOR DEVICE USING SHALLOW TRENCH ISOLATION AND METHOD OF FABRICATING THE SAME**

(75) Inventor: **Kazuhiro Tamura**, Tokyo (JP)

(73) Assignee: **Elpida Memory, Inc.** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/731,747**

(22) Filed: **Dec. 9, 2003**

(65) **Prior Publication Data**

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Related U.S. Application Data

(62) Division of application No. 10/260,484, filed on Sep. 30, 2002.

(30) **Foreign Application Priority Data**

Oct. 9, 2001 (JP) 2001-312034

(51) **Int. Cl.**
H01L 21/76 (2006.01)

(52) **U.S. Cl.** **438/424**; 438/435; 438/437; 438/981

(58) **Field of Classification Search** 438/424, 438/435, 437, 724, 757, 981
See application file for complete search history.

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Primary Examiner—Mary Wilczewski
Assistant Examiner—Toniae M. Thomas
(74) *Attorney, Agent, or Firm*—Hayes Soloway P.C.

(57) **ABSTRACT**

A semiconductor device adopting shallow trench isolation for reducing an internal stress of a semiconductor substrate. The semiconductor device is composed of a semiconductor substrate provided with a trench for isolation, and an insulating film formed to cover the trench for relaxing an internal stress of the semiconductor substrate. The insulating film includes a first portion disposed to be opposed to a bottom of the trench, and a second portion disposed to be opposed to a side of the trench. A first thickness of the first portion is different from a second thickness of the second portion.

7 Claims, 8 Drawing Sheets

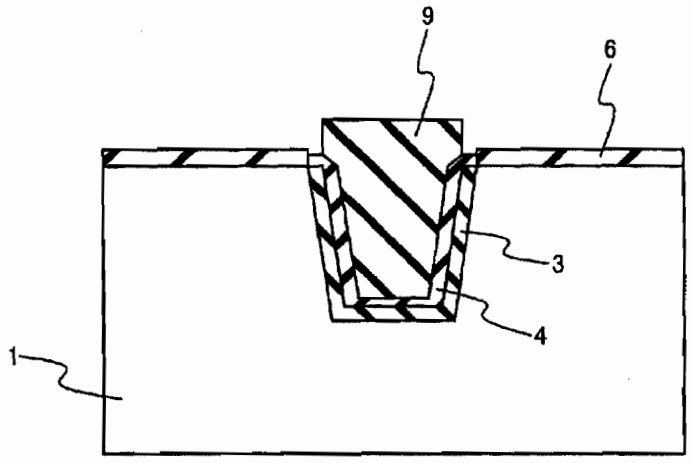


Fig. 1 PRIOR ART

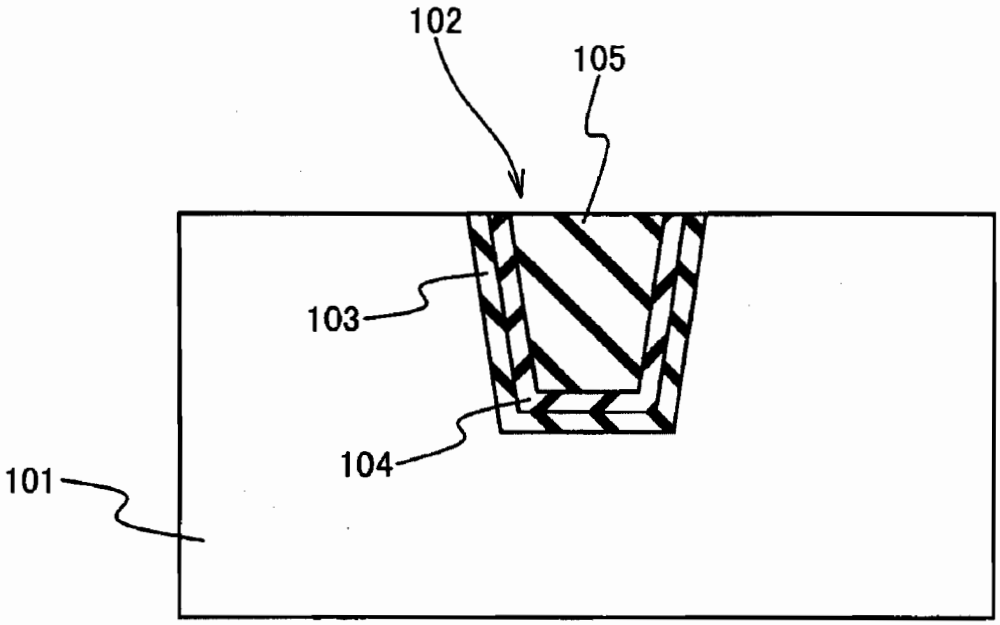


Fig. 2

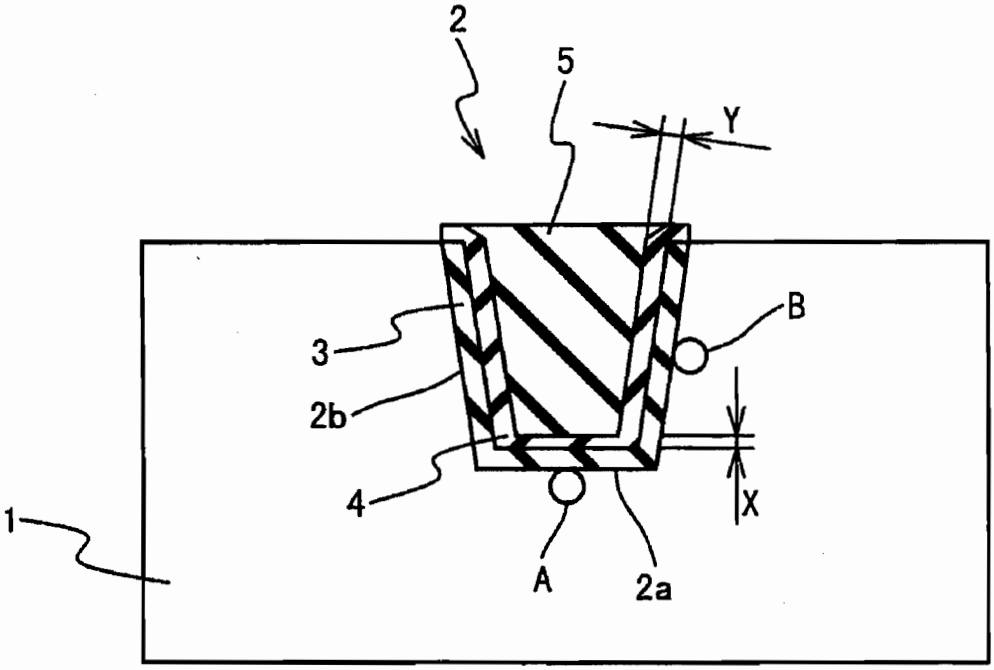


Fig. 3

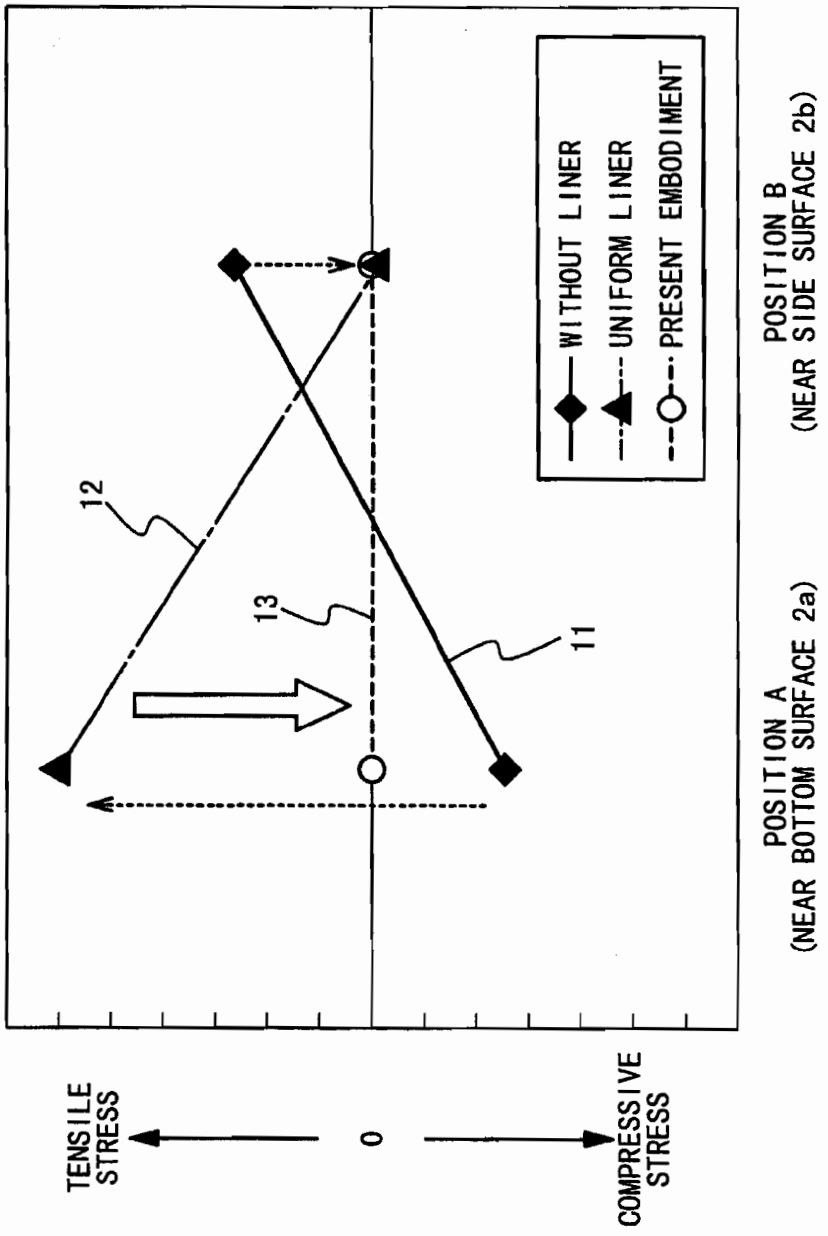

WITHOUT LINER
UNIFORM LINER
PRESENT EMBODIMENT
12
13
11
POSITION A
(NEAR BOTTOM SURFACE 2a)
POSITION B
(NEAR SIDE SURFACE 2b)
TENSILE STRESS
0
COMPRESSIVE STRESS

Fig. 4

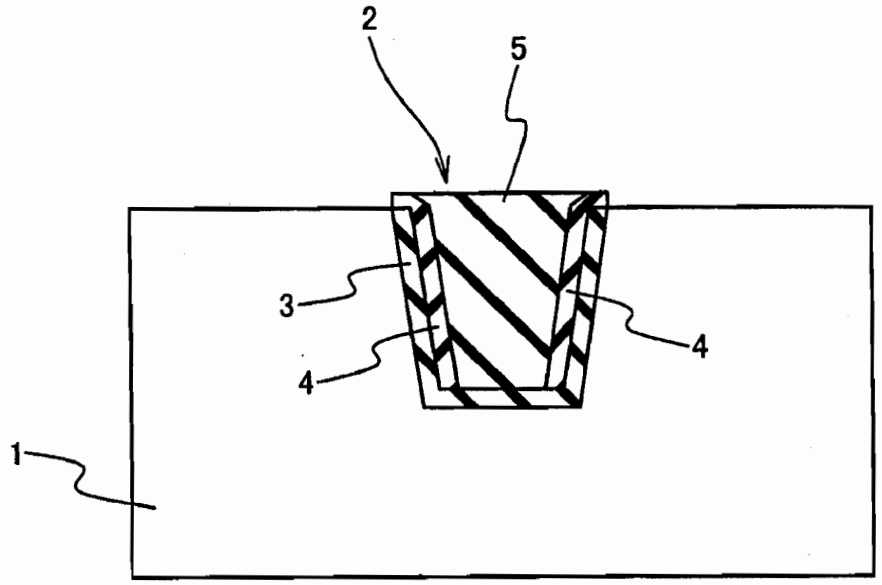


Fig. 5

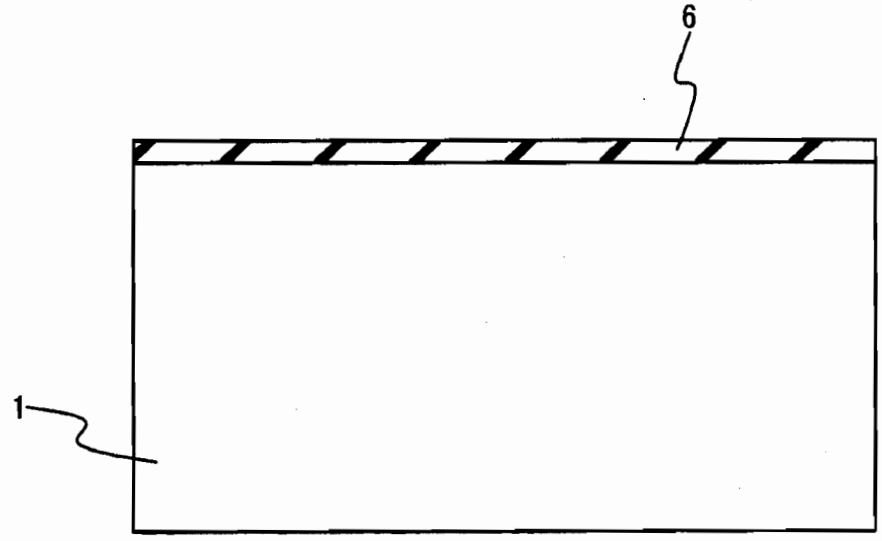


Fig. 6

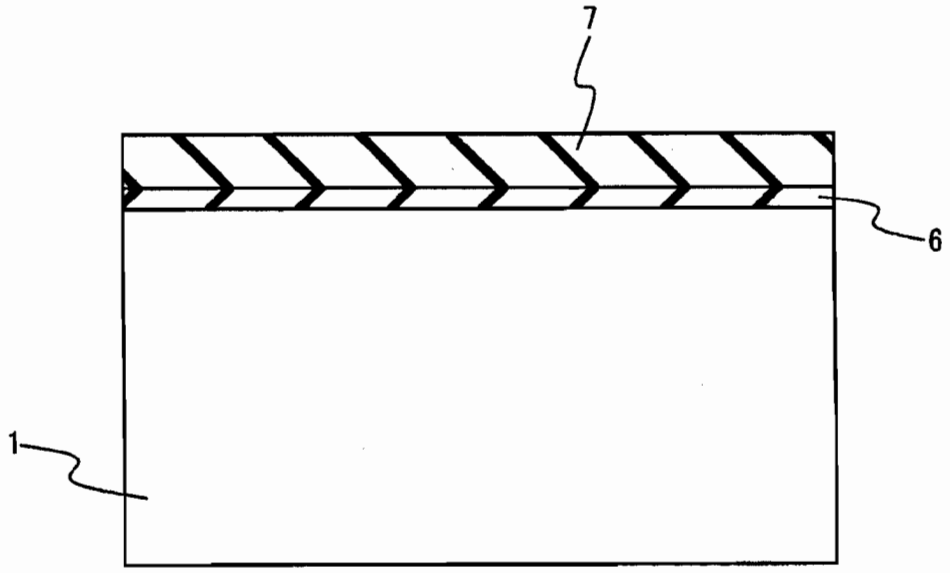


Fig. 7

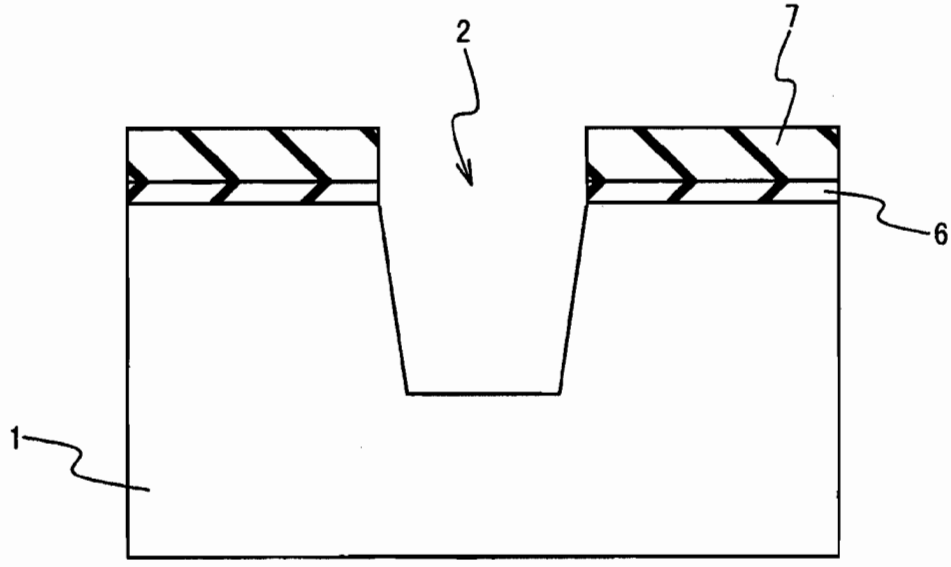


Fig. 8

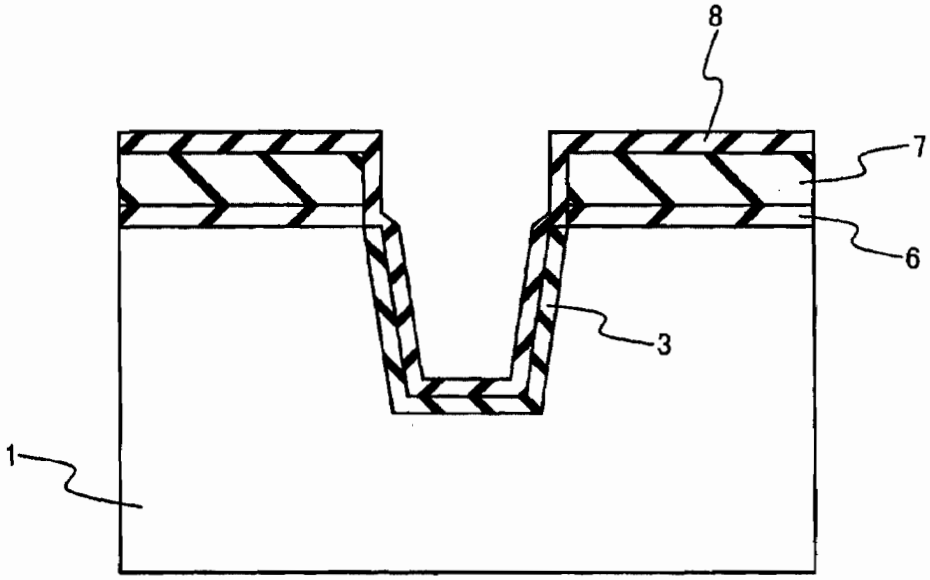


Fig. 9

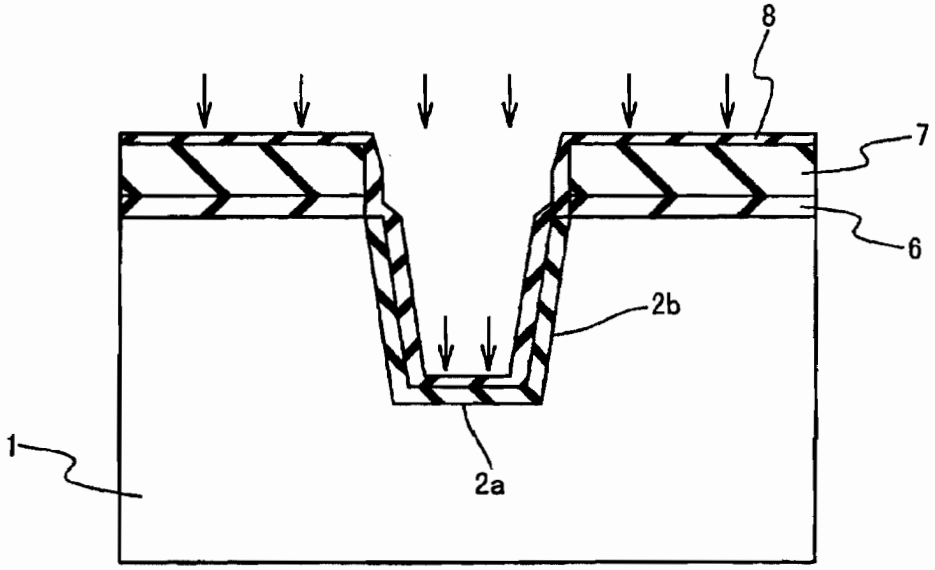


Fig. 10

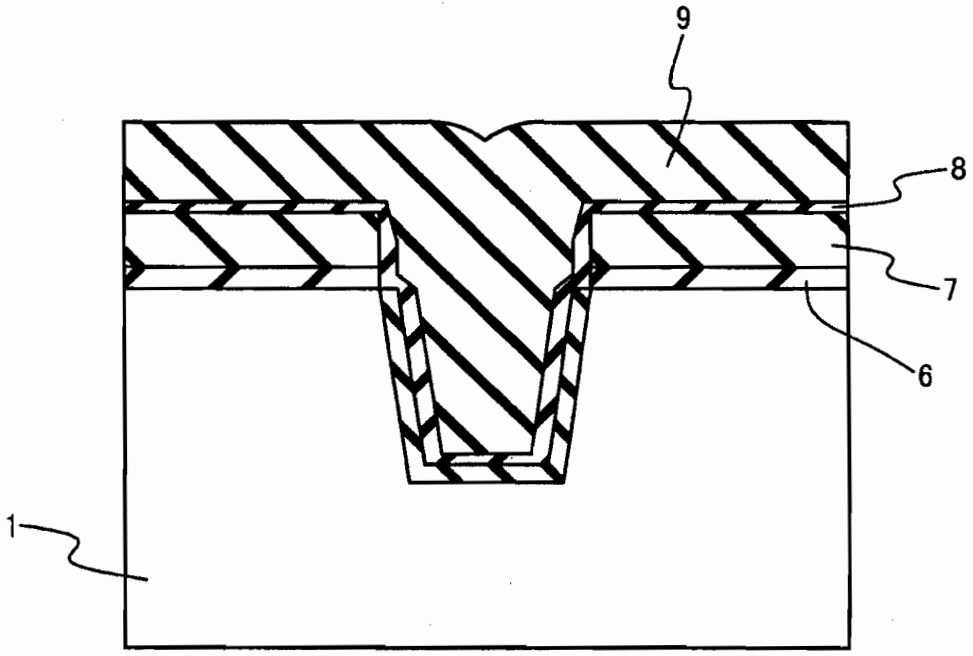


Fig. 11

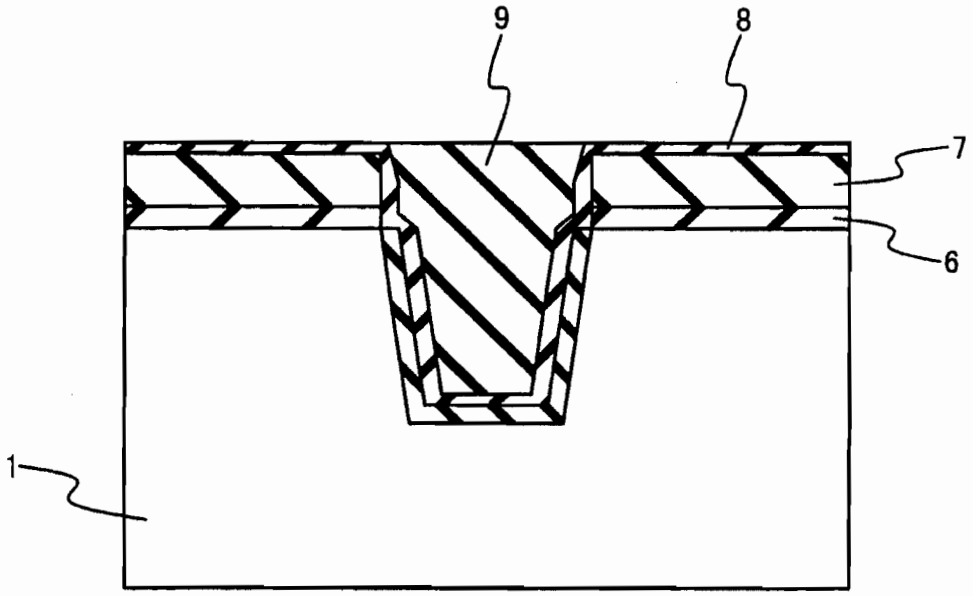
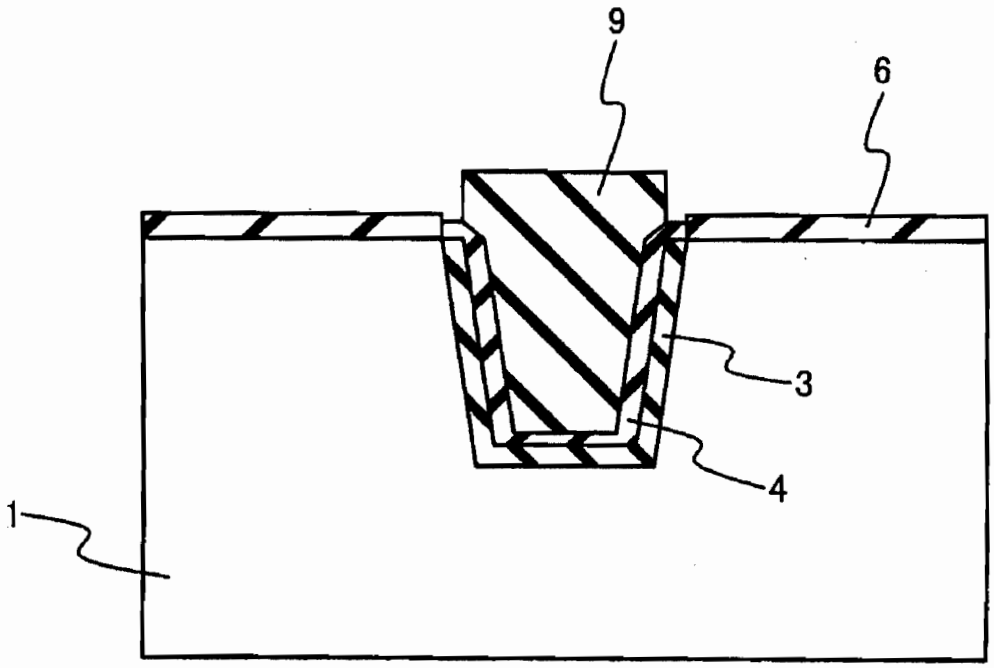


Fig. 12



SEMICONDUCTOR DEVICE USING SHALLOW TRENCH ISOLATION AND METHOD OF FABRICATING THE SAME

This Application is a divisional application of U.S. application Ser. No. 10/260,484, filed Sep. 30, 2002.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and a method of fabricating the same. More particularly, the present invention relates to a semiconductor device using shallow trench isolation.

2. Description of the Related Art

Highly integrated semiconductor devices often adopt shallow trench isolation. Isolation has been conventionally achieved by a LOCOS (Local Oxidation of Silicon) technique. However, the LOCOS technique has difficulties in fabricating highly integrated semiconductor devices, such as bird's beaks and poor isolation abilities. This situation encourages the adoption of the shallow trench isolation.

FIG. **1** shows a conventional structure of a semiconductor devices using shallow trench isolation. A trench **102** is formed on a silicon substrate **101**. The inner surface of the trench **102** is coated by a silicon oxide film **103** formed by thermal oxidization. A liner **104** made of silicon nitride is formed on the silicon oxide film **103**. A silicon oxide film **105** is formed on the liner **104** to fill the trench **102**.

The liner **104** relaxes the interior stress induced in the silicon substrate **101**. The shallow trench isolation causes the interior stress to be applied to the silicon substrate **161**, because of the difference in thermal expansion coefficients between the silicon substrate **101** and the silicon oxide film **105**. The stress applied to the silicon substrate **101** induces crystal defects in the silicon substrate, and thus increases junction leak currents. The increase in the junction leak currents causes improper operations of semiconductor devices. The relaxation of the internal stress by the liner **104** reduces the junction leak current and thus improves the reliability of the semiconductor device.

It is desired that the internal stress of the semiconductor substrate be further reduced. The reduction of the internal stress efficiently improves the reliability of the semiconductor device.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a technique for further reducing the internal stress applied to the semiconductor substrate of the semiconductor device in which the shallow trench isolation is employed.

In an aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, and an insulating film formed to cover the trench for relaxing an internal stress of the semiconductor substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is different from a second thickness of the second portion.

The first thickness of the first portion may be thinner than the second thickness of the second portion.

When the semiconductor device further includes another insulating film in the trench and the other insulating film exerts a compressive stress on the semiconductor substrate, the insulating film preferably exerts a tensile stress on said semiconductor substrate.

The insulating film is preferably formed of one selected from a group consisting of silicon nitride and silicon oxynitride.

In another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, and an insulating film formed to cover the trench for relaxing an internal stress of the semiconductor substrate. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film formed on the silicon oxide film. The insulating film exerts a tensile stress on the semiconductor substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is thinner than a second thickness of the second portion.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film formed on the silicon oxide film. The insulating film exerts a tensile stress on the semiconductor substrate. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film disposed on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxynitride. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is thinner than a second thickness of the second portion.

In still another aspect of the present invention, a semiconductor device includes a semiconductor substrate provided with a trench for isolation, a silicon oxide film formed to cover the trench, and an insulating film disposed on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxynitride. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a method of fabricating a semiconductor device is composed of:

forming a trench for isolation in the semiconductor substrate;

forming an insulating film to cover the trench for relaxing an internal stress of the silicon substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. The first thickness of the first portion is different from a second thickness of the second portion. The first thickness of the first portion may be thinner than the second thickness of the second portion.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming an insulating film to cover the trench for relaxing an internal stress of the silicon substrate, wherein the insu-

lating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming an insulating film on the silicon oxide film, wherein the insulating film exerts a tensile stress on the silicon substrate. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is thinner than a second thickness of the second portion.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover the trench;

forming an insulating film on the silicon oxide film. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover the trench; and

forming an insulating film on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxynitride. The insulating film includes a first portion opposed to a bottom of the trench, and a second portion opposed to a side of the trench. A first thickness of the first portion is different from a second thickness of the second portion.

In still another aspect of the present invention, a method for fabricating a semiconductor device is composed of:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover the trench; and

forming an insulating film on the silicon oxide film. The insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride. The insulating film is opposed to a side of the trench and is not opposed to a bottom of the trench.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a conventional semiconductor device adopting shallow trench isolation;

FIG. **2** shows a semiconductor device in an embodiment of the present invention;

FIG. **3** shows internal stresses exerted on a silicon substrate;

FIG. **4** shows a modification of the semiconductor device in the embodiment; and

FIGS. **5** to **12** are section views showing a fabrication process of the semiconductor device in the embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of a semiconductor apparatus according to the present invention and a method of manufacturing the same will be described below with reference to the attached drawings.

In an embodiment of the semiconductor device according to the present invention, as shown in FIG. **2**, a trench **2** is formed on a silicon substrate **1**. An inner surface of the trench **2** is coated by a silicon oxide film **3**. The silicon oxide film **3** is coated by a liner **4**. A silicon oxide film **5** is formed on the liner **4**. The trench **2** is filled with the silicon oxide film **3**, the liner **4** and the silicon oxide film **5**.

The liner **4** is formed of an insulating film that has a compressive internal stress. The silicon oxide films **3**, **5** have the tensile internal stresses, and thus exerts compression stresses on the silicon substrate **1**. The liner **4**, which has a compressive internal stress, exerts a tensile stress on the silicon substrate **1**, and thus relaxes the internal stress of the silicon substrate **1**. The liner **4** is preferably formed of silicon nitride or silicon oxynitride.

The liner **4** includes a bottom portion that is opposed to the bottom surface **2***a* of the trench **2**, and a side portion that is opposed to the side surface **2***b* of the trench **2**. A film thickness X of the bottom portion of the liner **4** is thinner than a film thickness Y of the side portion of the liner **4**. This structure further reduces the internal stress of the silicon substrate **1**. The inventor has discovered that an internal stress of the silicon substrate **1** in the vicinity of the bottom **2***a* of the trench **2** is weaker than that in the vicinity of the side **2***b* of the trench **2**. The difference in the film thicknesses of the bottom and side portions causes the different stresses on the vicinity of the bottom surface **2***a* and side surface **2***b*, and effectively reduces the internal stress of the silicon substrate **1**.

FIG. **3** shows the internal stresses of the silicon substrate **1** at positions A and B indicated by the circles in FIG. **2**. The position A is located near the bottom surface **2***a* of the trench **2**, and the position B is located near the side of the trench **2**. The internal stresses of the silicon substrate **1** are measured by a convergent beam electron diffraction (CBED) method.

Three samples have been fabricated; a first sample has a structure in which the liner **4** is excluded from the structure shown in FIG. **2**, a second sample has a structure in which the liner **4** is conformal or uniform in thickness, and a third sample has the structure shown in FIG. **2**. A line **11** in FIG. **3** represents the internal stresses of the silicon substrate without the liner **4**. A line **12** represents the internal stresses of the silicon substrate **1** when the liner **4** is uniform in the film thickness. A line **13** represents the internal stresses of the silicon substrate **1** in the semiconductor device having the structure shown in FIG. **2**.

In regard to the case that the film thickness of the liner **4** is uniform, the internal stress of the silicon substrate **1** is weak at the position B as indicated by the line **12**. However, the considerably strong tensile stress is applied to the silicon substrate **1** at the position A, which is located near the bottom plane of the trench **2**. This implies that the uniform liner **4** exerts the excessive tensile stress on the silicon substrate **1** at the position A.

The line **13** implies that the structure in which the film thickness X of the bottom portion of the liner **4** is thinner than the film thickness Y of the side portion remarkably reduces the internal stress of the silicon substrate **1** at the position A. The thinner film thickness of the bottom portion prevents an excessive tensile stress from being exerted on the silicon substrate **1**.

With reference to FIG. **2**, the film thickness X of the bottom portion of the liner **4** is adjusted on the basis of the internal stress applied to the silicon substrate **1**. It should be noted that the adjusted film thickness X of the bottom portion might be zero as shown in FIG. **4**. That is, the liner **4** may be designed such that the liner **4** is not opposed to the bottom surface **2***a* of the trench **2**.

The method of fabricating the semiconductor device shown in FIG. **2** will be described below.

As shown in FIG. **5**, the surface of the silicon substrate **1** is thermally oxidized to thereby form a sacrificed oxide film **6**. A film thickness of the sacrificed oxide film **6** is typically 10 to 20 nm.

A silicon nitride film **7** is then formed on the sacrificed oxide film **6**, as shown in FIG. **6**. A film thickness of the silicon nitride film **7** is typically 100 to 200 nm.

After the formation of the silicon nitride film **7**, as shown in FIG. **7**, the sacrificed oxide film **6** and the silicon nitride film **7** are patterned by an etching technique, which is well known in the art. The silicon substrate **1** is then etched to form the trench **2** by using the patterned sacrificed oxide film **6** and silicon nitride film **7** as a mask.

After the formation of the trench **2**, the inner surface of the trench **2** is thermally oxidized to thereby form the silicon oxide film **3**. A film thickness of the silicon oxide film **3** is typically 10 to 30 nm.

A silicon nitride film **8** is then formed to cover the entire structure as shown in FIG. **8**. The silicon nitride film **8** is exemplarily formed by using an LPCVD (Low Pressure Chemical Vapor Deposition) method. A film thickness of the silicon nitride film **8** is substantially uniform, and is typically 3 to 10 nm. The silicon nitride film **8** is formed in the conditions that the formed silicon nitride film **8** has the compressive internal stress. The other insulation film having a compressive internal stress may be used instead of the silicon nitride film **8**. For example, a silicon oxide nitride film may be formed instead of the silicon nitride film **8**.

After the formation of the silicon nitride film **8**, as shown in FIG. **9**, the silicon nitride film **8** is anisotropically etched in the direction perpendicular to the major surface of the silicon substrate **1**. A bottom portion of the silicon nitride film **8**, which is opposed to the bottom surface **2***a*, is partially removed. This causes the film thickness of the bottom portion of the silicon nitride film **8** to be thinner than that of the side portion opposed to the side **2***b* of the trench **2**. It should be noted that the bottom portion of the silicon nitride film **8** might be totally removed to form the structure shown in FIG. **4**. The etching of the silicon nitride film **8** may be executed by the physical etching such as ion milling or the physical and chemical etching.

A silicon oxide film **9** is then formed to cover the entire structure by using a CVD method as shown in FIG. **10**. The trench **2** is totally filled with the silicon oxide film **9**.

After the formation of the silicon oxide film **9**, as shown in FIG. **11**, a portion of the silicon oxide film **9** outside the trench **2** is removed to expose the surface of the silicon nitride film **8**. The partial removal of the silicon oxide film **9** is achieved by a CMP (Chemical Mechanical Polishing) method. The silicon nitride film **8** and the silicon nitride film **7** function as stoppers during the CMP process.

The silicon substrate **1** is then processed by heated phosphoric acid to remove the silicon nitride film **7** and a portion of the silicon nitride film **8** outside the trench **2** as shown in FIG. **12**. The remaining portion of the silicon nitride film **8** constitutes the liner **4**.

The silicon substrate **1** is then processed by hydrofluoric acid to remove the sacrificed oxide film **6** and a portion of the silicon oxide film **9** outside the trench **2**. The removal of the sacrificed oxide film **6** and the portion of the silicon oxide film **9** completes the formation of the structure shown in FIG. **2** (or, FIG. **4**). MOS transistors and other elements are then formed on the silicon substrate **1** to fabricate an LSI (Large Scale Integrated circuit).

As described, the semiconductor device in this embodiment has the structure in which the film thickness X of the bottom portion of the liner **4** is thinner than the film thickness Y of the side portion, or the film thickness X of the bottom portion is zero. This structure effectively reduces the internal stress of the silicon substrate **1**.

Although the invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form has been changed in the details of construction and the combination and arrangement of parts may be resorted to without departing from the spirit and the scope of the invention as hereinafter claimed.

What is claimed is:

1. A method of fabricating a semiconductor device comprising:

forming a trench for isolation in a semiconductor substrate; and

forming an insulating film to cover said trench for relaxing an internal stress of said semiconductor substrate, wherein said insulating film comprises:

a first portion disposed to be opposed to a bottom of said trench, and

a second portion disposed to be opposed to a side of said trench, and

wherein a first thickness of said first portion throughout is different from a second thickness of said second portion throughout, and wherein the second thickness of said second portion is substantially uniform along the entirety of said second portion.

2. The method according to claim **1**, wherein said first thickness of said first portion is thinner than said second thickness of said second portion.

3. The method according to claim **2**, further comprising:

forming another insulating film in said trench, wherein said another insulating film exerts a compressive stress on said semiconductor substrate, and said insulating film exerts a tensile stress on said semiconductor substrate.

4. The method according to claim **2**, wherein said insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxynitride.

5. A method for fabricating a semiconductor device comprising:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover said trench; and

forming an insulating film on said silicon oxide film, wherein said insulating film exerts a tensile stress on said semiconductor substrate, and

wherein said insulating film comprises:

a first portion disposed to be opposed to a bottom of said trench, and

a second portion disposed to be opposed to a side of said trench, and

wherein a first thickness of said first portion throughout is thinner than a second thickness of said second portion throughout, and wherein the second thickness of said second portion is substantially uniform along the entirety of said second portion.

6. The method according to claim **5**, wherein said insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxynitride.

7. A method for fabricating a semiconductor device comprising:

forming a trench for isolation in a semiconductor substrate;

forming a silicon oxide film to cover said trench; and

forming an insulating film on said silicon oxide film, wherein said insulating film is formed of one selected from a group consisting of silicon nitride and silicon oxinitride, wherein said insulating film comprises:

a first portion disposed to be opposed to a bottom of said trench, and

a second portion disposed to be opposed to a side of said trench, and

wherein a first thickness of said first portion throughout is different from a second thickness of said second portion throughout, and wherein the second thickness of said second portion is substantially uniform along the entirety of said second portion.

* * * * *

Exhibit 4

US007709366B2

(12) **United States Patent**
Koga

(10) **Patent No.: US 7,709,366 B2**
(45) **Date of Patent: May 4, 2010**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventor: **Hiroki Koga**, Tokyo (JP)

(73) Assignee: **Elpida Memory, Inc.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 824 days.

(21) Appl. No.: **11/116,036**

(22) Filed: **Apr. 27, 2005**

(65) **Prior Publication Data**

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Related U.S. Application Data

(62) Division of application No. 10/251,062, filed on Sep. 20, 2002, now Pat. No. 6,914,309.

(30) **Foreign Application Priority Data**

Sep. 20, 2001 (JP) 2001-286140

(51) **Int. Cl.**
H01L 21/3205 (2006.01)

(52) **U.S. Cl.** **438/586**; 438/637; 438/639; 438/675; 257/E21.507

(58) **Field of Classification Search** 438/257, 438/585, 656, 399, 586, 637, 639, 675, 300, 438/301; 257/E21.199, E21.507, E21.166
See application file for complete search history.

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Primary Examiner—W. David Coleman
Assistant Examiner—Latanya Crawford
(74) *Attorney, Agent, or Firm*—Katten Muchin Rosenman LLP

(57) **ABSTRACT**

A semiconductor device has a pair of impurity regions in a semiconductor substrate. A silicon layer is formed on the impurity region. A gate insulating film is formed between the impurity regions. A gate electrode is formed on the gate insulating film. A first silicon nitride film is formed on the gate electrode. A silicon oxide film is formed on a side surface of the gate electrode. A second silicon nitride film is partially formed on the silicon layer and on a side surface of the silicon oxide film. A conductive layer is formed on the silicon layer.

21 Claims, 7 Drawing Sheets

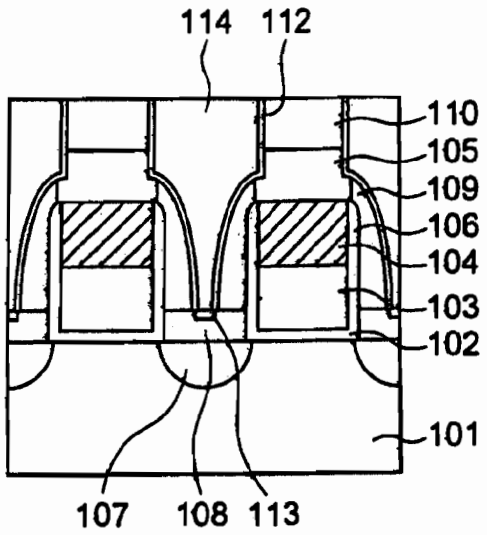

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FIG. 1A
PRIOR ART

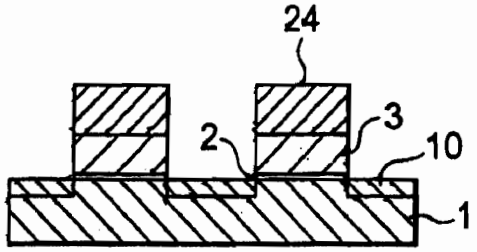


FIG. 1B
PRIOR ART

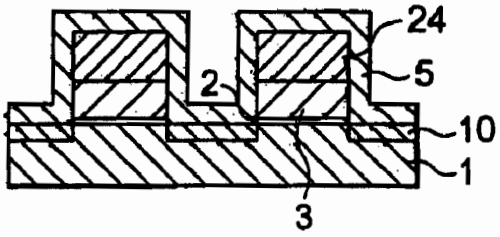


FIG. 1C
PRIOR ART

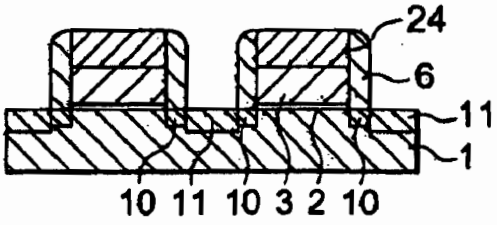


FIG. 1D
PRIOR ART

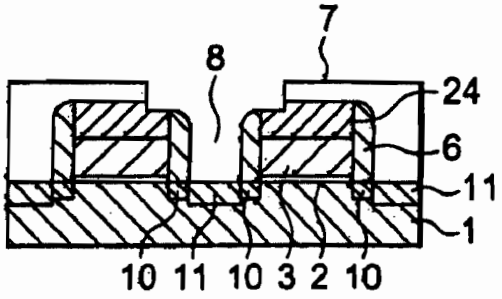


FIG. 1E
PRIOR ART

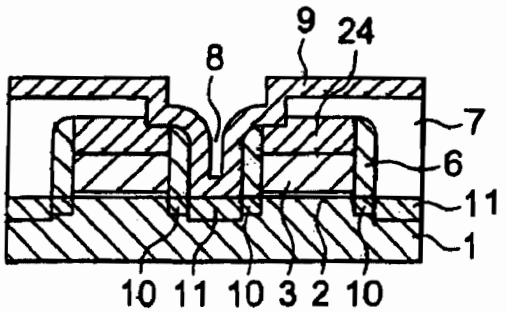


FIG. 2A
PRIOR ART

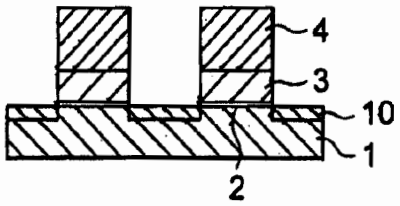


FIG. 2B
PRIOR ART

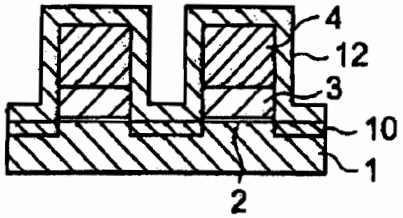


FIG. 2C
PRIOR ART

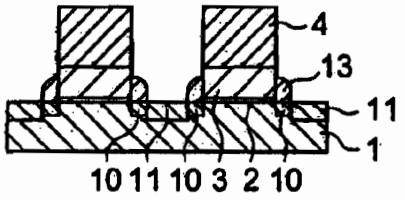


FIG. 2D
PRIOR ART

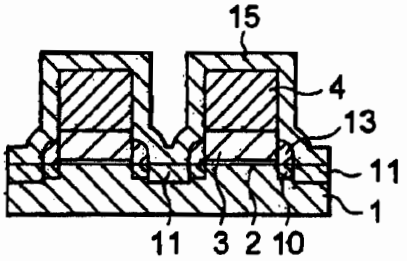


FIG. 2E
PRIOR ART

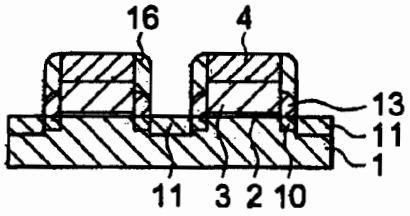


FIG. 2F
PRIOR ART

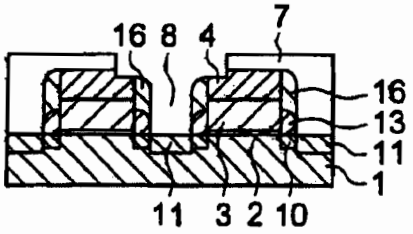
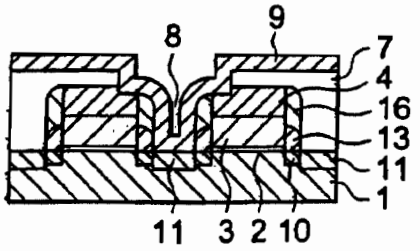


FIG. 2G
PRIOR ART



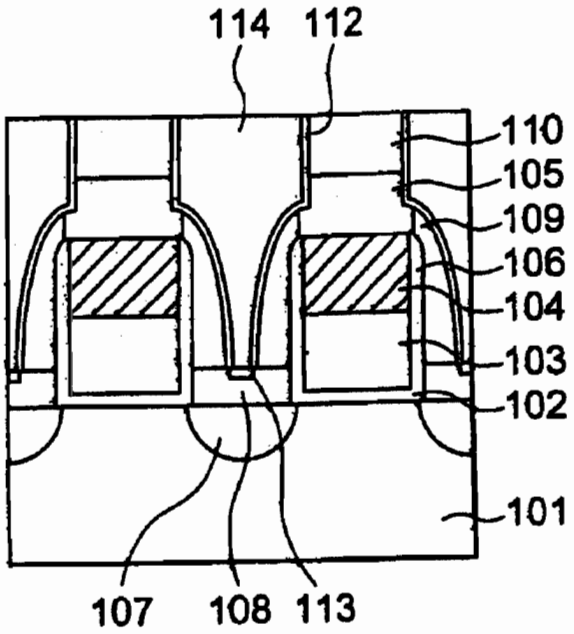

114
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FIG. 3

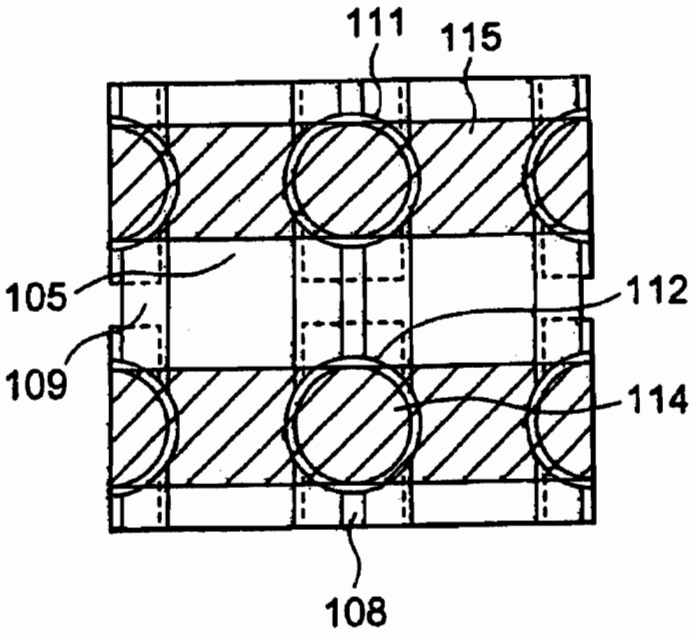
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FIG. 4

FIG. 5A

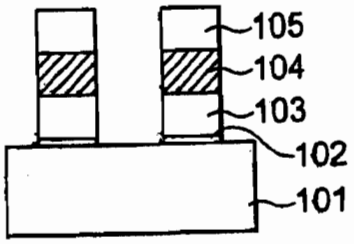


FIG. 5B

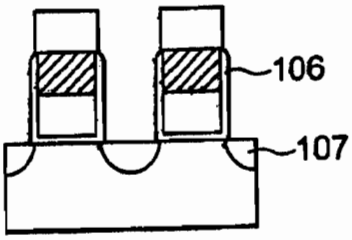


FIG. 5C

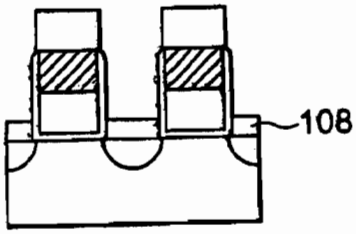


FIG. 5D

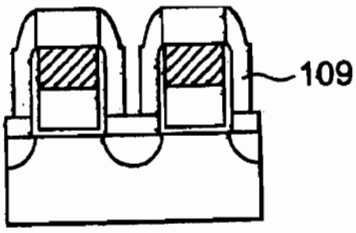


FIG. 5E

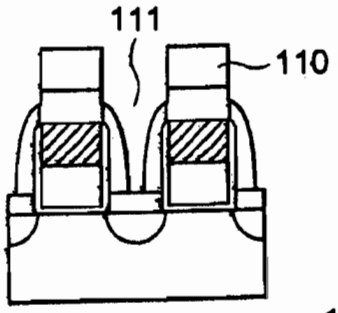


FIG. 5F

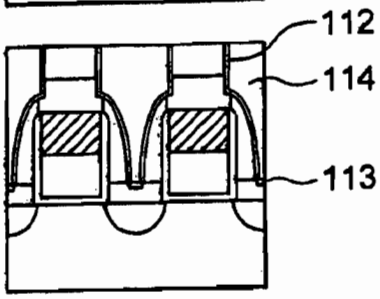


FIG. 6A

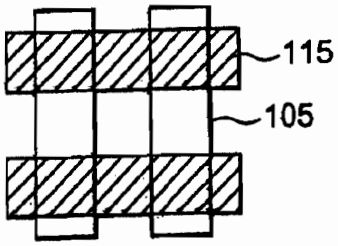


FIG. 6B

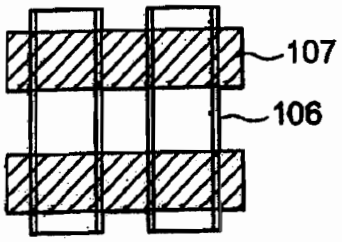


FIG. 6C

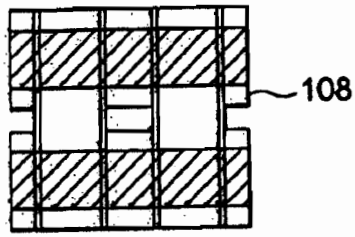


FIG. 6D

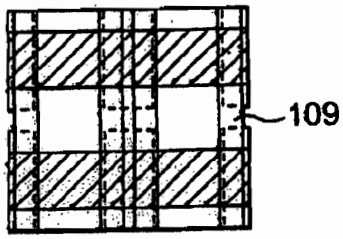


FIG. 6E

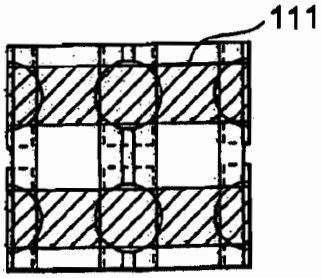


FIG. 6F

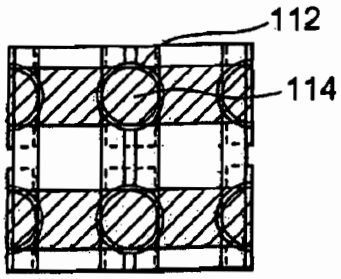


FIG. 7A

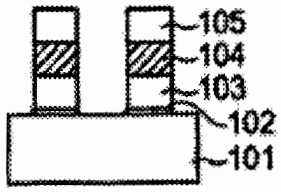


FIG. 7B

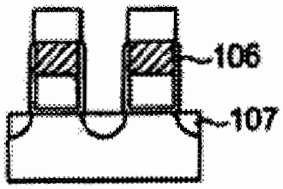


FIG. 7C

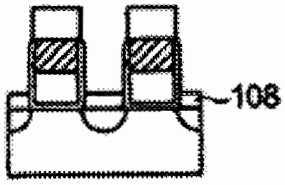


FIG. 7D

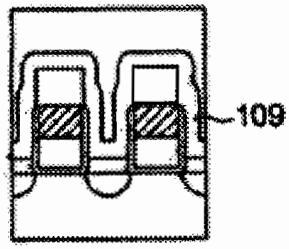


FIG. 7E

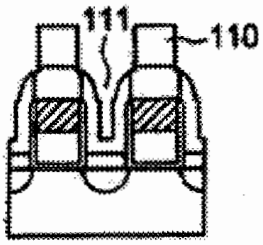


FIG. 7F

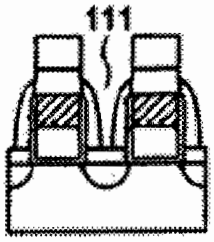


FIG. 7G

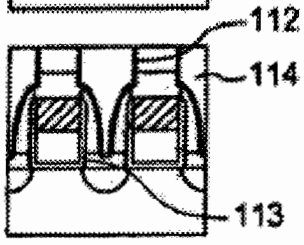


FIG. 8A

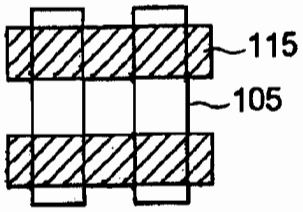


FIG. 8B

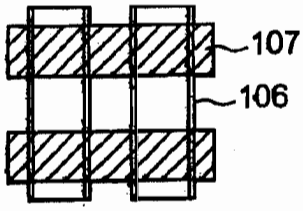


FIG. 8C

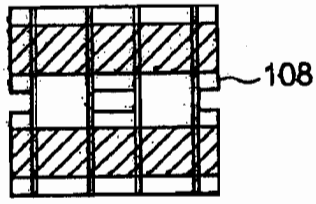


FIG. 8D

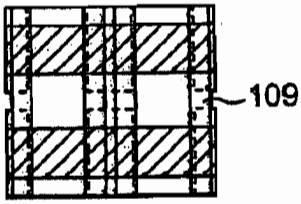


FIG. 8E

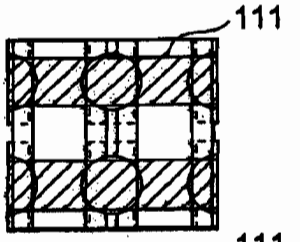


FIG. 8F

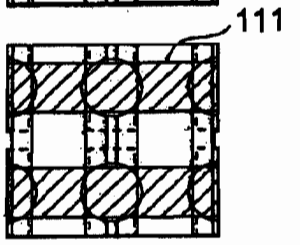
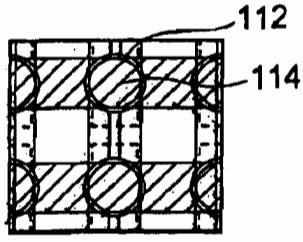


FIG. 8G



SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. application Ser. No. 10/251,062 filed on Sep. 20, 2002 now U.S. Pat. No. 6,914,309, and claims priority under 35 USC 119 from Japanese Patent Application 2001-286140 filed Sep. 20, 2001, the contents of which are herein wholly incorporated by reference.

BACKGROUND OF THE INVENTION

This invention relates to a semiconductor device and a method of manufacturing the same. More specifically, this invention relates to transistors arranged with high-density by the use of silicon selective growth technique and contact formation technique based on self-alignment, and a method of manufacturing the same.

In order to achieve high-density in the semiconductor device, the recent trend is directed to the miniaturization technique of the devices. For achieving the device with a greater scale of high-density, a mask alignment margin between a contact and an underlayer wiring pattern has been reduced.

As a method of reducing such mask alignment margin, a technique for forming the contact by the use of the self-alignment is exemplified.

In the technique, the underlayer wiring pattern is covered with a silicon nitride film and the contact is opened by etching having a high-etching selective ratio between the silicon oxide film as an interlayer insulating film and the silicon nitride film for protecting the underlayer wiring pattern. Such conventional technique is disclosed in, for example, Japanese Unexamined Patent Publication (JP-A) No. Hei. 9-213949.

Referring now to FIGS. **1**A through **1**E, the conventional technique will be described below.

At first, a gate oxide film **2** is deposited on a semiconductor substrate **1** as illustrated in FIG. **1**A. Thereafter, a polysilicon film **3** and a silicon nitride film **24** are sequentially deposited thereon, and an unnecessary portion is removed by the use of photolithography and anisotropic dry etching. Thereby a gate electrode made of the polysilicon film **3** is formed such that the silicon nitride film **24** is laminated or stacked thereon. Next, a low-concentration impurity region **10** is formed on the semiconductor substrate **1** by using ion implantation.

Successively, a silicon nitride film **5** is deposited on a whole surface, as illustrated in FIG. **1**B.

Then the silicon nitride film **5** is partially etched-back by the use of the anisotropic dry-etching such that a sidewall film **6** is left only on a sidewall portion of the gate electrode, as illustrated in FIG. **1**C. Thereafter, a high-concentration impurity region **11** is formed by the ion implantation.

Successively, an interlayer insulating film **7** as the silicon oxide film is entirely deposited thereon, and a contact hole **8** is opened by removing an unnecessary portion by the use of the photolithography and the anisotropic dry-etching, as illustrated in FIG. **1**D.

In such anisotropic dry-etching, an etching rate of the silicon nitride film is lower than that of the silicon oxide film so that an etching selective ratio becomes higher.

As a consequence, even when an upper opening dimension of the contact hole **8** is larger than a space between the sidewall films **6** of adjacent gate electrodes, the gate electrode is protected by the silicon nitride film **24** and the sidewall film **6** so that the gate electrode is not electrically shorted with a wiring layer **9** which will be formed later.

Next, a conductive film is deposited on the whole surface, and the wiring layer **9** is formed by removing an unnecessary portion by the photolithography as well as the anisotropic dry-etching, as illustrated in FIG. **1**E.

In the above-described conventional technique, however, the silicon nitride film, which readily traps a hot electron, is used as the sidewall film **6** of the gate electrode. Consequently, a transistor characteristic is easily deteriorated. The above-mentioned conventional publication also discloses a method of solving such a problem, and this method will be explained with reference to FIGS. **2**A through **2**G.

At first, the gate oxide film **2** is deposited on the semiconductor substrate **1**, as illustrated in FIG. **2**A. Thereafter, the polysilicon film **3** and the silicon nitride film **4** are sequentially deposited thereon, and an unnecessary portion is removed by the photolithography and the anisotropic dry etching. Thus, the gate electrode as the polysilicon film **3**, on which the silicon nitride film **4** is laminated, is formed.

Next, the low-concentration impurity region **10** is formed in the semiconductor substrate **1** by the ion implantation.

Subsequently, the silicon oxide film **12** is deposited on the whole surface, as illustrated in FIG. **2**B.

Successively, the silicon oxide film **12** is partially etched-back by the use of the anisotropic dry-etching so that a first sidewall film **13** is left only on the sidewall portion of the polysilicon film **3** as the gate electrode, as illustrated in FIG. **2**C.

In such anisotropic dry-etching, the etching selective ratio between the silicon oxide film and the silicon nitride film becomes high. As a result, while the first sidewall film **13** has the substantially same height as that of the polysilicon film **3** by adjusting etching time, a film thickness of the silicon nitride film **4** on the polysilicon film **3** is not largely reduced. Thereafter, the high-concentration impurity region **11** is formed by using the ion implantation.

Subsequently, the silicon nitride film **15** is deposited on the whole surface with the substantially same film thickness as that of the sidewall film **13**, as illustrated in FIG. **2**D.

Next, the silicon nitride film **15** is partially etched-back by using the anisotropic dry-etching so that a second sidewall film **16** is left only on the sidewall portion of the silicon nitride film **4** on the gate electrode and the polysilicon film **3** as the gate electrode, as illustrated in FIG. **2**E. In this event, the etching time is adjusted such that the silicon nitride film **15** is not left on the side surface of the first sidewall film **13**.

Successively, the interlayer insulating film **7** as the silicon oxide film is deposited on the whole surface, and the contact hole **8** is opened by removing an unnecessary portion by the use of the photolithography and the dry-etching, as illustrated in FIG. **2**F.

In such anisotropic dry-etching, the etching selective ratio between the silicon oxide film and the silicon nitride film is selected to a high value. Thereby, even if the upper opening of the contact hole **8** has the dimension larger than the space between the sidewall films **6** of the adjacent gate electrodes, the gate electrode is protected by the silicon nitride film **4**, the first sidewall film **13** and the second sidewall film **16**. As a consequence, the gate electrode is not electrically shorted with the wiring film which will be formed later.

Next, the conductive film is deposited on the whole surface, and the wiring layer **9** is formed by removing an unnecessary portion by using the photolithography and the anisotropic dry-etching, as illustrated in FIG. **2**G.

By employing the above-described technique, both the first sidewall film **13** and the second sidewall film **16** are placed

between the polysilicon film **3** as the gate electrode and the wiring layer **9**. In consequence, even when the dimension of the upper opening of the contact hole **8** is larger than the space between the sidewall films of the adjacent gate electrodes, the gate electrode is not electrically shorted with the wiring layer **9**.

Further, the lower portion of the sidewall film of the gate electrode is formed of the silicon oxide film. Thereby, the hot carrier can not be readily trapped as compared with the case of the silicon nitride film. Therefore, the transistor characteristic is not easily deteriorated.

Upon formation of the second sidewall film **16**, the etch-back must be carried out so that the silicon nitride film **15** formed on the side surface of the first sidewall film **13** is completely removed.

However, the silicon nitride film **15** may be partially left on the side surface of the first sidewall film **13** in the practical use in the cause of variation of the film thickness of the silicon nitride film **15** and variation of the anisotropic dry-etching rate upon etch-back.

Under such circumstances, the bottom portion of the contact hole **8** becomes smaller in dimension than the predetermined value, so that contact resistance is increased inevitably.

Upon the etch-back of the silicon nitride film **15**, the surface of the high-concentration impurity region **11** is subjected to etch-back atmosphere during long time, resulting in etching damage. As a consequence, the transistor characteristic is degraded.

In addition, the first sidewall film **13** is formed of the silicon oxide film. Therefore, the first sidewall film **13** is also etched in a step of processing hydrofluoric acid chemical liquid for removing a natural oxide film on the bottom portion of the contact before forming the wiring layer. Consequently, the polysilicon film **3** may be electrically shorted with the wiring layer **6**

Depending upon the kinds of products, only the low concentration impurity regions **10** are used as source/drain regions of the transistor but the high concentration impurity regions may be not formed.

For example, a dynamic random access memory (DRAM) adopts such a structure in order to reduce a leak current in a reverse direction at a PN junction between an N-type low concentration impurity regions **10** as source/drain regions and a P-well region in many cases.

With this structure, it is difficult to employ metal material for the wiring layer **9**. This reason will be explained below. Namely, in case where a silicide layer as compound of metal and silicon is formed between the wiring layer **9** and the low concentration impurity region **10**, a depletion layer formed at the PN junction is widely extended towards an N-side so that the silicide layer is entrapped inside the depletion layer.

The silicide layer can serves as a generation recombination center, that is, a GR center, and therefore, the leak current in the reverse direction is increased. The wiring layer **9** is often made of the polysilicon such that no silicide layer is formed between the wiring layer **9** and the low concentration impurity region **10**. In this case, the contact resistance is increased in comparison with the metal wiring layer.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a semiconductor device which has a contact formed by a self-alignment with low resistance and in which a transistor characteristic is not readily deteriorated, and a method of manufacturing the same.

Other objects of this invention will become clear as the description proceeds.

According to a first aspect of this invention, there is provided a semiconductor device having a pair of impurity regions in a semiconductor substrate, comprising:

a silicon layer which is formed on the iinpurity region;

a gate insulating film which is formed between the impurity regions;

a gate electrode which is formed on the gate insulating film;

a first silicon nitride film which is formed on the gate electrode;

a silicon oxide film which is formed on a side surface of the gate electrode;

a second silicon nitride film which is partially formed on the silicon layer and which is formed on a side surface of the silicon oxide film; and

a conductive layer which is formed on the silicon layer.

Preferably, the gate electrode is made of apolysilicon layer and a metal layer or a metal silicide layer.

Preferably, the silicon oxide film and the second silicon nitride film constitute a double sidewall spacer.

Preferably, the silicon layer is insulated from the gate electrode only by the silicon oxide film, and a lower edge of the second nitride film contacts with an upper surface of the silicon layer.

Preferably, the conductive layer is insulated from the gate electrode by the first silicon nitride film and the double sidewall spacer.

Preferably, a silicide layer is placed between the conductive layer and the silicon layer.

Preferably, a depletion layer is formed near the impurity region, and the silicon layer serves so as to prevent the depletion layer from reaching the titanium silicide layer.

According to a second aspect of this invention, there is provided a method of manufacturing a semiconductor device, comprising the steps of:

forming a gate insulating film on the semiconductor substrate;

forming a gate electrode on the gate insulating film;

forming a first silicon nitride film on the gate electrode;

forming a silicon oxide film at a side surface of the gate electrode;

forming impurity regions at both sides of the gate electrode in the semiconductor substrate;

forming a silicon layer on the impurity region;

partially forming a second silicon nitride film on the silicon layer at a side surface of the silicon oxide film; and

forming a conductive layer on the silicon layer.

Preferably, the gate electrode is formed of a polysilicon layer and a metal layer or a metal silicide layer.

Preferably, the silicon layer is selectively grown on the impurity region by selective epitaxial growth.

The method further may comprise the following steps of:

forming a titanium/titanium nitride lamination film on the silicon layer; and

forming a titanium silicide layer on the silicon layer by thermal treatment.

Preferably, depletion layer is formed near the impurity region, and the silicon layer serves so as to prevent the depletion layer from reaching the titanium silicide layer.

Preferably, the silicon oxide film and the second silicon nitride film constitute a double sidewall spacer.

Preferably, a hot carrier is generated at an edge of the impurity region, and a distance between the edge of the impurity region and the second silicon nitride film is selected such that the hot carrier is not trapped in the second silicon nitride film.

According to a third aspect of this invention, there is provided a method of manufacturing a semiconductor device, comprising the steps of:

forming a gate insulating film on the semiconductor substrate;

sequentially forming a polysilicon film and a metal film or a metal silicide film and a first silicon nitride film on the semiconductor substrate;

forming a gate electrode by removing an unnecessary portion by lithography and anisotropic dry-etching;

oxidizing at least a side surface of the polysilicon film in oxidation atmosphere;

exposing a surface of the silicon substrate by etching-back an oxide film by anisotropic dry etching;

forming source/drain regions by ion-implantation;

growing silicon layers on the source/drain regions by a silicon selective growth;

entirely growing a second silicon nitride film;

exposing the silicon layer by etching-back the second silicon nitride film by anisotropic dry etching;

forming an interlayer insulating film made of a silicon oxide film; and

opening a contact hole by lithography and dry-etching.

According to this invention, the distance between the edge of the drain region and the sidewall spacer becomes large. Herein, the hot carrier is readily generated at the edge of the drain region while the sidewall spacer is made of the silicon nitride film. Under this circumstance, the transistor characteristic is not deteriorated because no hot carrier is trapped inside the sidewall spacer.

In addition, the depletion layer formed at the PN junction is largely extended towards the N-type impurity region. However, the depletion layer is prevented from being extended and does not reach the titanium silicide layer because the silicon formed on the impurity region is the N+type region including phosphorous with 1E20/cm^3. As a consequence, the silicide layer does not proceed inside the depletion layer, so that the leak current in the reverse direction is not increased.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A through **1**E are cross sectional views explaining the conventional contact formation technique by self-alignment;

FIGS. **2**A through **2**G are cross sectional views showing a method of manufacturing the conventional semiconductor device;

FIG. **3** is a cross sectional view showing a semiconductor device according to this invention;

FIG. **4** is a plan view showing a semiconductor device according to this invention;

FIGS. **5**A through **5**F are cross sectional views showing a method of manufacturing a semiconductor device according to a first embodiment of this invention;

FIGS. **6**A through **6**F are plan views showing a method of manufacturing a semiconductor device according to a first embodiment of this invention;

FIGS. **7**A through **7**G are cross sectional views showing a method of manufacturing a semiconductor device according to a second embodiment of this invention; and

FIGS. **8**A through **8**G are plan views showing a method of manufacturing a semiconductor device according to a second embodiment of this invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to FIGS. **3** and **4**, description will be made about a semiconductor device such as a field effect transistor (FET) according to this invention.

A semiconductor device (a field effect transistor) comprises a gate electrode made of a polysilicon **103** and a tungsten silicide **104** placed on a semiconductor substrate **101** via a gate insulating film **102**, an impurity region **107**, and a silicon layer **108** grown selectively only on the impurity region **107**.

With such a structure, a double sidewall spacer consisting of a silicon oxide film **106** and a second silicon nitride film **109** is entirely or partially arranged on the side surface of the gate electrode of the transistor. The grown silicon layer **108** is insulated from the gate electrode only by the silicon oxide film **106** as the sidewall spacer while the lower edge of the second silicon nitride film **109** as the sidewall spacer contacts with the upper surface of the silicon nitride film **108**.

A conductive layer (for example, a tungsten layer) **114** filling a contact hole **111** is insulated from the gate electrode by a first silicon nitride film **105** placed over the, gate electrode and the sidewall spacer.

On the first silicon nitride film **105**, a silicon oxide film **110** is placed, and the conductive layer **114** is covered with a titanium/titanium nitride lamination film **112**. A titanium silicide **113** is arranged between the conductive layer **114** and the silicon layer **108**.

Referring to now to FIGS. **5**A through **5**F and FIG. **6**A through **6**F, description will be made about a method of manufacturing a semiconductor device according to a first embodiment of this invention.

The surface of the semiconductor substrate **101** is thermally oxidized to a thickness of 5 nm to thereby form the gate oxide film **102**, as illustrated in FIGS. **5**A and **6**A. Thereafter, a polysilicon film including phosphorus is grown to a thickness of 100 nm by CVD (Chemical Vapor Deposition), and successively, the tungsten silicide **104** is grown by the use of CVD or sputtering.

Subsequently, the first silicon nitride film **105** is deposited to a thickness of 100 nm by the CVD. Unnecessary portions of the first silicon nitride film **105**, the tungsten silicide **104** and polysilicon film **103** are removed to thereby form the gate electrode.

Next, the polysilicon film **103** patterned by the thermal oxidation and the tungsten silicide patterned are oxidized on the side surface to thereby form the silicon oxide film **106** to a thickness of about 10 nm, as illustrated in FIGS. **5**B and **6**B.

Successively, the gate oxide film **102** formed on the silicon substrate between the gate electrodes is etched-back by the use of the anisotropic etching to thereby expose the surface of the silicon substrate **101**. Thereafter, phosphorus ions are implanted with 1E13/cm^2 under energy of 30 keV to thereby form the impurity region as the drain region.

Subsequently, the silicon layer **108** including phosphorus with 1E20/cm^3 is grown to a thickness of about 50 nm on the impurity region **107** by using selective epitaxial silicon growth, as illustrated in FIGS. **5**C and **6**C.

Successively, the second silicon nitride film **109** is deposited on the whole surface by the CVD, as illustrated in FIGS. **3**D and **4**D. The film thickness of the second silicon nitride film **109** is preferably adjusted such that the second silicon nitride film **109** does not bury between the gate electrodes. For example, if the space between the gate electrodes is equal to 150 nm, the second silicon nitride film **109** has the thickness of about 50 nm. Next, the second silicon nitride film **109**

selectively grown on the silicon **108** is etched-back by the use of the anisotropic etching to thereby expose out the surface of the silicon layer **108**.

Thereafter, the silicon oxide film **110** is deposited thereon to a thickness of 500 nm by the CVD, and the surface thereof is flattened by the use of CMP (Chemical Mechanical Polishing), as illustrated in FIGS. **5**E and **6**E. Next, the contact hole **111** is opened by removing an unnecessary portion of the silicon oxide film **110** by the lithography and the anisotropic dry etching.

In such anisotropic etching, the silicon oxide film has an etching rate slower than that of the silicon nitride film. Thereby, even if the dimension of the upper portion of the contact hole **111** is larger than the space between the gate electrodes, the gate electrode is not partially exposed inside the contact hole **111** because the gate electrode is covered with the first silicon nitride film **105** and the second silicon nitride film **109**, as illustrated in FIGS. **6**E and **6**E.

Subsequently, titanium and titanium nitride are grown to 10 nm by the CVD or the sputtering, respectively, and thereby, the titanium/titanium nitride lamination film **112** is formed, as illustrated in FIGS. **5**F and **6**F. Thereafter, a thermal treatment is carried out at 700° C. for 30 seconds, and as a result, the titanium reacts with the silicon to thereby form a titanium silicide layer **113**. Next, the conductive layer **114** made of tungsten is deposited to 300 nm by the CVD, and successively, unnecessary portions of the conductive layer **114** and the titanium/titanium nitride lamination film **112** are removed by the CMP.

Referring to FIGS. **7**A through **7**G and FIG. **8**A through **8**G, description will be made about a method of manufacturing a semiconductor device according to a second embodiment of this invention.

The surface of the semiconductor substrate **101** is thermally oxidized to a thickness of 5 nm to thereby form the gate oxide film **102**, as illustrated in FIGS. **7**A and **8**A. Thereafter, the polysilicon film including phosphorus is grown to a thickness of 100 nm by the CVD, and successively, the tungsten silicide **104** is grown by the use of the CVD or the sputtering.

Subsequently, the first silicon nitride film **105** is deposited to a thickness of 100 nm by the CVD. Unnecessary portions of the first silicon nitride film **105**, the tungsten silicide **104** and polysilicon film **103** are removed to thereby form the gate electrode.

Next, the polysilicon film **103** patterned by the thermal oxidation and the tungsten silicide **104** patterned are oxidized on the side surface to thereby form the silicon oxide film **106** to a thickness of about 10 nm, as illustrated in FIGS. **7**B and **8**B.

Successively, the gate oxide film **102** formed on the silicon substrate **101** between the gate electrodes is etched-back by the use of the anisotropic etching to thereby expose out the surface of the silicon substrate **101**. Thereafter, phosphorus ions are implanted with 1E13/cm^2 under energy of 30 keV to thereby form the impurity regions as the source/drain regions.

Subsequently, the silicon layer **108** including phosphorus with 1E20/cm^3 is grown to a thickness of about 50 nm on the impurity region **107** by using the selective epitaxial silicon growth, as illustrated in FIGS. **7**C and **8**C.

Successively, the second silicon nitride film **109** is deposited on the whole surface by the CVD, as illustrated in FIGS. **7**D and **8**D. The film thickness of the second silicon nitride film **109** is preferably selected such that the second silicon nitride film **109** does not bury between the gate electrodes. For example, if the space of the gate electrodes is equal to 150 nm, the second silicon nitride film **109** has the thickness of about 50 nm. Next, a silicon oxide film **110** is deposited to 500 nm by the CVD, and the surface is flattened by the CMP.

Next, an unnecessary portion of the silicon oxide film **110** is removed by the lithography and the anisotropic dry-etching, as illustrated in FIGS. **7**E and **8**E.

In such anisotropic etching, the silicon oxide film **110** has an etching rate slower than that of the silicon nitride film. Thereby, even if the dimension of the upper portion of the contact hole **111** is larger than the space between the gate electrodes, the gate electrode is not partially exposed out because the gate electrode is covered with the first silicon nitride film **105** and the second silicon nitride film **109**, as illustrated in FIGS. **7**E and **8**E.

Successively, the second silicon nitride film **109** on the silicon layer **108** grown selectively by the anisotropic dry-etching is etched-back to thereby expose out the surface of the silicon layer **108**, as illustrated in FIGS. **7**F and **8**F.

Subsequently, titanium and titanium nitride are grown to 10 nm by the CVD or the sputtering, respectively, and thereby, a titanium/titanium nitride lamination film **112** is formed, as illustrated in FIGS. **7**G and **8**G. Thereafter, a thermal treatment is carried out at 700° C. for 30 seconds, and as a result, the titanium reacts with the silicon to thereby form the titanium silicide layer **113**. Next, the conductive layer **114** made of tungsten is deposited to 300 nm by the CVD, and successively, unnecessary portion of the conductive layer **114** and the titanium/titanium nitride lamination film **112** are removed by the use of the CMR

While this invention has thus far been disclosed in conjunction with several embodiments thereof, it will be readily possible for those skilled in the art to put this invention into practice in various other manners.

For example, according to the above-described embodiments, the gate electrode is made of the polysilicon **103** and the tungsten silicide **104**. However, this invention is not restricted to such a structure, and the gate electrode may be made of other materials as long as the polysilicon layer and the metal layer or the metal silicide layer are employed. For example, the tungsten may be employed as the metal layer while the titanium silicide may be used as the other silicide layer.

What is claimed is:

1. A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a gate insulating film on the semiconductor substrate;

(b) forming a gate electrode on the gate insulating film;

(c) forming a first silicon nitride film on the gate electrode;

(d) forming a sidewall which is formed only by a silicon oxide film so as to reach to a surface of the semiconductor substrate and which is formed at a side surface of the gate electrode;

(e) forming impurity regions at both sides of the gate electrode in the semiconductor substrate;

(f) forming a silicon layer selectively on the impurity region so as to contact with a surface of the sidewall;

(g) forming a second silicon nitride film partially on the silicon layer and partially at a side surface of the silicon oxide film;

(h) forming a conductive layer on the silicon layer, the first silicon nitride film, and the second silicon nitride film;

wherein steps (c) and (d) are performed in sequence.

2. A method as claimed in claim **1**, wherein:

the gate electrode is formed of a polysilicon layer and a metal layer or a metal silicide layer.

3. A method as claimed in claim 1, wherein:
the silicon layer is selectively grown on the impurity region by selective epitaxial growth.

4. A method as claimed in claim 1, further comprising the following steps of:
forming a titanium/titanium nitride lamination film on the silicon layer; and forming a titanium silicide layer on the silicon layer by thermal treatment.

5. A method as claimed in claim 1, wherein:
the silicon oxide film and the second silicon nitride film constitute a double sidewall spacer.

6. A method as claimed in claim 1, further comprising:
forming a conductive film between said conductive layer and said first silicon nitride film.

7. A method as claimed in claim 4, wherein:
a depletion layer is formed near the impurity region, and the silicon layer serves so as to prevent the depletion layer from reaching the titanium silicide layer.

8. A method as claimed in claim 5, wherein:
a hot carrier is generated at an edge of the impurity region, and a distance between the edge of the impurity region and the second silicon nitride film is selected such that the hot carrier is not trapped in the second silicon nitride film.

9. A method of manufacturing a semiconductor device, comprising the steps of:
(a) forming a gate insulating film on the semiconductor substrate;
(b) sequentially forming a polysilicon film and a metal film or a metal silicide film and a first silicon nitride film on the semiconductor substrate;
(c) forming a gate electrode by removing an unnecessary portion by lithography and anisotropic dry-etching;
(d) oxidizing at least a side surface of the polysilicon film in oxidation atmosphere;
(e) exposing a surface of the silicon substrate by etching-back an oxide film by anisotropic dry etching;
(f) forming source/drain regions by ion-implantation;
(g) growing silicon layers on the source/drain regions by a silicon selective growth;
(h) entirely growing a second silicon nitride film;
(i) exposing the silicon layer by etching-back the second silicon nitride film by anisotropic dry-etching;
(j) forming an interlayer insulating film made of a silicon oxide film;
(k) opening a contact hole by lithography and dry-etching; and
(l) forming a conductive layer on the silicon layer, the first silicon nitride film, and the second silicon nitride film;
wherein steps (e), (f), and (g) are performed sequentially.

10. A method as claimed in claim 9, further comprising:
forming a conductive film between said conductive layer and said first silicon nitride film.

11. A method as claimed in claim 9, wherein:
the gate electrode is formed of the polysilicon film and the metal layer or the metal silicide layer.

12. A method as claimed in claim 9, wherein:
impurity regions are formed at both sides of the gate electrode in the semiconductor substrate; and
the silicon layer is selectively grown on the impurity region by selective epitaxial growth.

13. A method as claimed in claim 9, further comprising the following steps of:
forming a titanium/titanium nitride lamination film on the silicon layer; and forming a titanium silicide layer on the silicon layer by thermal treatment.

14. A method as claimed in claim 9, wherein:
the silicon oxide film and the second silicon nitride film constitute a double sidewall spacer.

15. A method as claimed in claim 12, wherein:
a depletion layer is formed near the impurity region, and the silicon layer serves so as to prevent the depletion layer from reaching a titanium silicide layer.

16. A method as claimed in claim 12, wherein:
a hot carrier is generated at an edge of the impurity region, and a distance between the edge of the impurity region and the second silicon nitride film is selected such that the hot carrier is not trapped in the second silicon nitride film.

17. A method of forming a semiconductor device, the method comprising:
(a) forming first and second gate structures over a semiconductor substrate to make a space between the first and second gate structures, the space being defined by side surfaces of the first and second gate electrode structures facing with each other, each of the first and second gate electrode structures having an upper surface;
(b) forming first and second sidewalls respectively on the side surfaces of the first and second gate structures, each of the first and second side walls including a first part on a side of the semiconductor substrate and a second part on a side of the upper surface thereof;
(c) forming a silicon layer in the space over the semiconductor substrate and in contact respectively with the first parts of the first and second side walls;
(d) forming third and fourth sidewalls in contact respectively with the second parts of the first and second side walls and with the silicon layer with leaving a portion of the silicon layer between the third and fourth sidewalls;
(e) forming a conductive film to cover respective surfaces of the third and fourth sidewalls and the portion of the silicon layer; and
(f) forming a conductive layer on the conductive film to fill the space.

18. The method of forming a semiconductor device as claimed in claim 17, wherein each of the first and second sidewalls is different in material from each of the third and fourth sidewalls.

19. The method of forming a semiconductor device as claimed in claim 17, wherein each of the first and second sidewalls includes a silicon oxide film and each of the third and fourth sidewalls includes a silicon nitride film.

20. The method of forming a semiconductor device as claimed in claim 17, wherein the conductor film includes lamination of a titanium film and a titanium nitride film.

21. The method of forming a semiconductor device as claimed in claim 17, wherein the silicon layer is formed by selective epitaxial growth.

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